To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M35012-XXXSP, M35013-XXXSP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DESCRIPTION

The M35012-XXXSP and M35013-XXXSP are TV screen display control IC which can be used to display information such as program schedules, the date and messages on the TV screen.

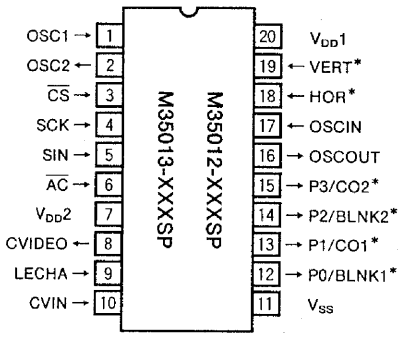
The differences among M35012-XXXSP and M35013-XXXSP are noted below.

The descriptions that follow describe the M35013-XXXSP unless otherwise noted.

Type name	M35012-XXXSP	M35013-XXXSP
Characters available	256	128
Data input	16 bits serial input	8 bits serial input
Exclusion function	Exclusion 1 and 2 function	Exclusion 1 function
CONT7F function	Normal/FF_{16} writing mode	Normal/$7F_{16}$ writing mode

For M35013-001SP and M35012-001SP that are standard ROM version of M35013-XXXSP and M35012-XXXSP respectively, the I/O polarity of pin and the character pattern are also mentioned.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4B

Note : The pins remarked "*" are selectabled the input or output polarity when the character ROM masked.

FEATURES

- Screen composition ..... 24 columns × 10 lines
- Number of characters displayed ..... 240 (Max.)
- Character composition ..... 12 × 18 dot matrix
- Characters available
  - M35013-XXXSP ..... 128 characters
  - M35012-XXXSP ..... 256 characters
- Character sizes available ... 4 (horizontal) × 4 (vertical)
- Display locations available
  - Horizontal direction ..... 62 locations
  - Vertical direction ..... 64 locations
- Blinking ..... Character units
  - Cycle : approximately 1 second, or approximately 0.5 seconds
  - Duty : 25%, 50%, or 75%
- Data input
  - M35013-XXXSP ..... By the 8-bit serial input function
  - M35012-XXXSP ..... By the 16-bit serial input function
- Coloring
  - Background coloring (composite video signal)
- Blanking
  - Total blanking (14 × 18 dots)
  - Border size blanking
  - Character size blanking
- Synchronization signal
  - Composite synchronization signal generation (PAL, NTSC, M-PAL)
- Synchronized separation circuit ..... Built-in
- 4 output ports (2 digital lines)
- Oscillation stop function
  - Be possible to stop the oscillation for display and for synchronized signal generation
- Exclusion function
  - M35013-XXXSP 1
  - M35012-XXXSP 2
- Reversed character display function

APPLICATION

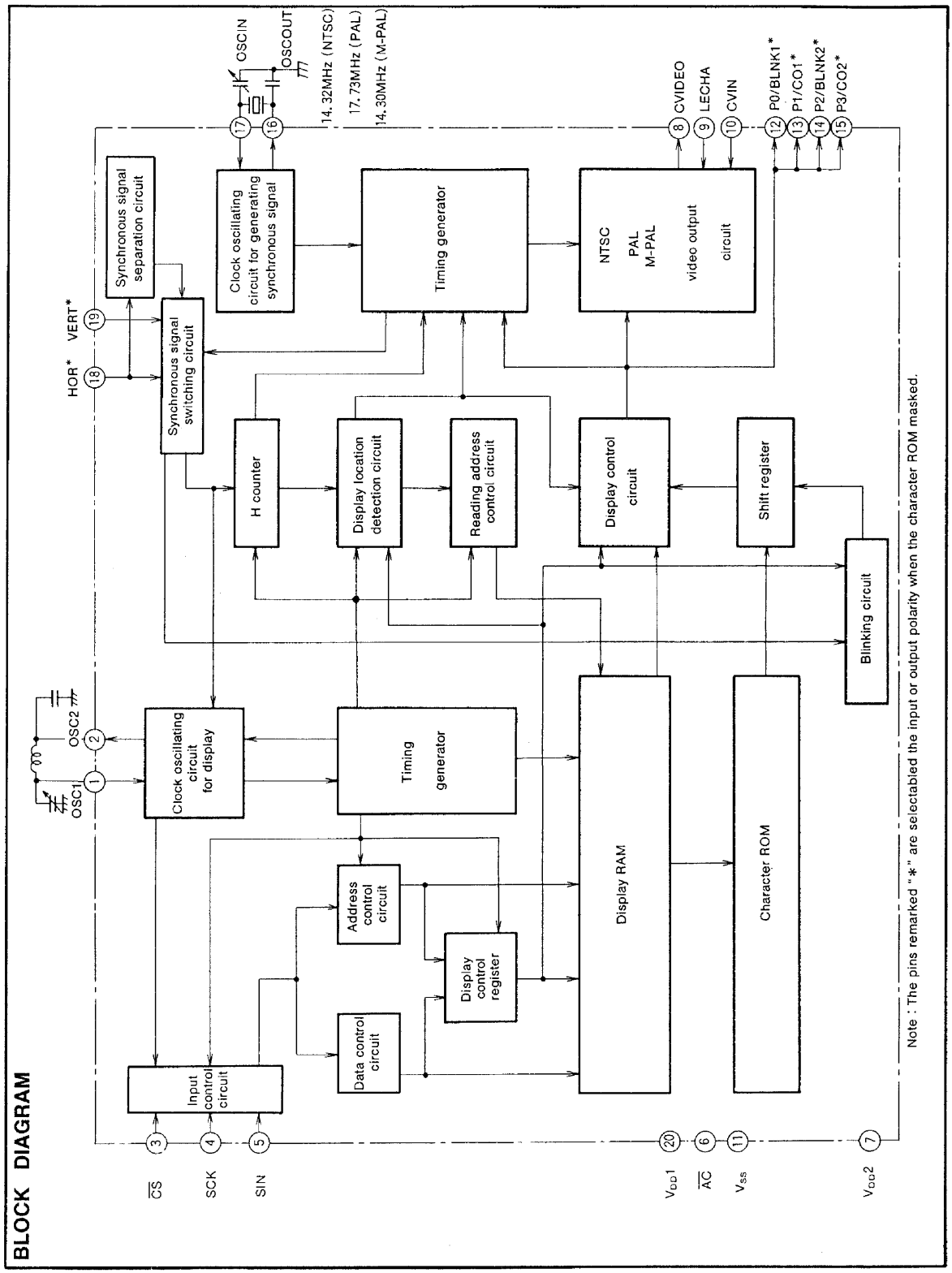
TV, VCR, Camcorder

PIN DESCRIPTION

Pin Number	Symbol	Pin name	Input /Output	Function
1	OSC1	Pins for attachment of external oscillator circuit	Input	There are the pins for attaching an external display oscillator circuit. The standard oscillation frequency is approximately 7MHz. This oscillation frequency determines the horizontal position of the display on the TV screen and the width of the characters.
2	OSC2		Output	
3	$\overline{CS}$	Chip select input	Input	This is the chip select pin, and when serial data transmission is being carried out, it goes to "L". Hysteresis input. Includes built-in pull-up resistor.
4	SCK	Serial clock input	Input	When $\overline{CS}$ pin is "L", SIN serial data is taken in when SCK rises. Hysteresis input. Built-in pull-up resistor is included.
5	SIN	Serial data input	Input	This is the pin for serial input of data and addresses for the display control register and the display data memory. Hysteresis input. Inculdes built-in pull-up resistor.
6	$\overline{AC}$	Auto-clear input	Input	When "L", this pin resets the internal IC circuit. Hysteresis input. Includes built-in pull-up resistor.
7	$V_{DD}2$	Power pin	—	Please connect to +5V with the analog circuit power pin.
8	CVIDEO	Composite video signal output	Output	This is the output pin for composite video signals. It outputs $2V_{P-P}$ composite video signals. In superimpose mode, character output etc. is superimposed on the external composite video signals from CVIN.
9	LECHA	Character level input	Input	This is the input pin which determines the "white" character color level in the composite video signal.
10	CVIN	Composite video signal input	Input	This is the input pin for external composite video signals. In superimpose mode, character output etc. is superimposed on these external composite video signals.
11	V_{SS}	Earthing pin	—	Please connect to GND using circuit earthing pin.
12	P0	Port P0 output	Output	This pin can be toggled between port pin output and BLNK1* (character background) signal output. Polarity can be selected when the character ROM is masked.
13	P1	Port P1 output	Output	This pin can be toggled between port pin output and CO1* (character) signal output. Polarity can be selected when the character ROM is masked.
14	P2	Port P2 output	Output	This pin can be toggled between port pin output and BLNK2* (character background) signal output. Polarity can be selected when the character ROM is masked.
15	P3	Port P3 output	Output	This pin can be toggled between port pin output and CO2* (character) signal output. Polarity can be selected when the character ROM is masked.
16	OSCOUT	Pins for attachment of external oscillator circuit for synchronization signal generation	Output	These are the pins for attaching an external oscillator circuit for generating the synchronization signal. An oscillation of 14.32MHz is needed for NTSC, 17.73MHz is needed for PAL and 14.30MHz is needed for M-PAL.
17	OSCIN		Input	
18	HOR*	Horizontal synchronization signal input	Input	This pin inputs the horizontal synchronization signal. Hysteresis input. Polarity can be selected when the character ROM is masked.
19	VERT*	Vertical synchronization signal input	Input	This pin inputs the vertical synchronization signal. Hysteresis input. Polarity can be selected when the character ROM is masked.
20	$V_{DD}1$	Power pin	—	Please connect to +5V with the digital circuit power pin.

Note : The pins remarked "*" are selectabled the input or output polarity when the character ROM masked.

BLOCK DIAGRAM



MEMORY CONSTITUTION

Address 00_{16} to EF_{16} are assigned to the display RAM, address $F0_{16}$ to $F8_{16}$ are assigned to the display control registers.

Bit / Address	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Remarks
00_{16}	EXP	C_6	C_5	C_4	C_3	C_2	C_1	C_0	Display RAM
⋮	Expansion bit	Character code							
EF_{16}	EXP	C_6	C_5	C_4	C_3	C_2	C_1	C_0	
$F0_{16}$	PTD 3	PTD 2	PTD 1	PTD 0	PTC 3	PTC 2	PTC 1	PTC 0	Port output specify
$F1_{16}$	TBASE 1	TBASE 0	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0	Horizontal display start position specify
$F2_{16}$	$\overline{INT}$/NON	SEPV	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0	Vertical display start position specify
$F3_{16}$	VSZ 21	VSZ 20	VSZ 11	VSZ 10	HSZ 21	HSZ 20	HSZ 11	HSZ 10	Character size specify
$F4_{16}$	DSP 7	DSP 6	DSP 5	DSP 4	DSP 3	DSP 2	DSP 1	DSP 0	Display mode specify
$F5_{16}$	$\overline{N}$/P	TEST 2	TEST 1	TEST 0	EXP 1	EXP 0	DSP 9	DSP 8	Expansion
$F6_{16}$	EQP	PAL H	MPAL	ALL 24	FSC	BLINK 2	BLINK 1	BLINK 0	Blinking specify and so on
$F7_{16}$	BLKHF	BB	BG	BR	LEVEL 0	PHASE 2	PHASE 1	PHASE 0	Raster color specify
$F8_{16}$	DSP ON	CONT7F	STOP 1	STOP IN	RAM ERS	EX	BLK 1	BLK 0	Control display

Fig. 1 Memory constitution (M35013-XXXSP)

At the M35013-XXXSP
The internal circuit is reset and all display control registers (address $F0_{16}$ to $F8_{16}$) are set to "0" and display RAM (address 00_{16} to EF_{16}) are set to "$7F_{16}$" when the $\overline{AC}$ pin level is "L". The memory constitution is shown in Figure 1.

At the M35012-XXXSP
The internal circuit is reset and all display control registers (address $F0_{16}$ to $F8_{16}$) are set to "0" and display RAM (address 00_{16} to EF_{16}) are set to "FF_{16}" when the $\overline{AC}$ pin level is "L". The memory constitution is shown in Figure 2.

Address \ Bit	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Remarks
00_{16}	0	0	0	0	0	REV	BLINK	0	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0	Display RAM
⋮	⋮	⋮	⋮	⋮	⋮	Reversed character	Blinking	⋮	Character code								
EF_{16}	0	0	0	0	0	REV	BLINK	0	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0	
$F0_{16}$	0	0	0	0	0	0	0	0	PTD3	PTD2	PTD1	PTD0	PTC3	PTC2	PTC1	PTC0	Port output specify
$F1_{16}$	0	0	0	0	0	0	0	0	TBAS1	TBAS0	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display start position specify
$F2_{16}$	0	0	0	0	0	0	0	0	$\overline{INT}$/ NON	SEPV	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display start position specify
$F3_{16}$	0	0	0	0	0	0	0	0	VSZ 21	VSZ 20	VSZ 11	VSZ 10	HSZ 21	HSZ 20	HSZ 11	HSZ 10	Character size specify
$F4_{16}$	0	0	0	0	0	0	0	0	DSP7	DSP6	DSP5	DSP4	DSP3	DSP2	DSP1	DSP0	Display mode specify
$F5_{16}$	0	0	0	0	0	0	0	0	$\overline{N}$/P	TEST 2	TEST 1	TEST 0	EXP1	EXP0	DSP9	DSP8	Expansion
$F6_{16}$	0	0	0	0	0	0	0	0	EQP	PALH	MPAL	ALL 24	FSC	BLINK 2	BLINK 1	BLINK 0	Blinking specify and so on
$F7_{16}$	0	0	0	0	0	0	0	0	BLKHF	BB	BG	BR	LEVEL 0	PHASE 2	PHASE 1	PHASE 0	Raster color specify
$F8_{16}$	0	0	0	0	0	0	0	0	DSPON	CONT 7F	STOP 1	STOP IN	RAMERS	EX	BLK1	BLK0	Control display

Fig. 2 Memory constitution (M35012-XXXSP)
※DA8 to DAF of the display control registers (addresses $F0_{16}$ to $F8_{16}$) are set to "0".

SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM. The screen consitution is shown in Figure 3.

Line \ Row	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	00_{16}	01_{16}	02_{16}	03_{16}	04_{16}	05_{16}	06_{16}	07_{16}	08_{16}	09_{16}	$0A_{16}$	$0B_{16}$	$0C_{16}$	$0D_{16}$	$0E_{16}$	$0F_{16}$	10_{16}	11_{16}	12_{16}	13_{16}	14_{16}	15_{16}	16_{16}	17_{16}
2	18_{16}	19_{16}	$1A_{16}$	$1B_{16}$	$1C_{16}$	$1D_{16}$	$1E_{16}$	$1F_{16}$	20_{16}	21_{16}	22_{16}	23_{16}	24_{16}	25_{16}	26_{16}	27_{16}	28_{16}	29_{16}	$2A_{16}$	$2B_{16}$	$2C_{16}$	$2D_{16}$	$2E_{16}$	$2F_{16}$
3	30_{16}	31_{16}	32_{16}	33_{16}	34_{16}	35_{16}	36_{16}	37_{16}	38_{16}	39_{16}	$3A_{16}$	$3B_{16}$	$3C_{16}$	$3D_{16}$	$3E_{16}$	$3F_{16}$	40_{16}	41_{16}	42_{16}	43_{16}	44_{16}	45_{16}	46_{16}	47_{16}
4	48_{16}	49_{16}	$4A_{16}$	$4B_{16}$	$4C_{16}$	$4D_{16}$	$4E_{16}$	$4F_{16}$	50_{16}	51_{16}	52_{16}	53_{16}	54_{16}	55_{16}	56_{16}	57_{16}	58_{16}	59_{16}	$5A_{16}$	$5B_{16}$	$5C_{16}$	$5D_{16}$	$5E_{16}$	$5F_{16}$
5	60_{16}	61_{16}	62_{16}	63_{16}	64_{16}	65_{16}	66_{16}	67_{16}	68_{16}	69_{16}	$6A_{16}$	$6B_{16}$	$6C_{16}$	$6D_{16}$	$6E_{16}$	$6F_{16}$	70_{16}	71_{16}	72_{16}	73_{16}	74_{16}	75_{16}	76_{16}	77_{16}
6	78_{16}	79_{16}	$7A_{16}$	$7B_{16}$	$7C_{16}$	$7D_{16}$	$7E_{16}$	$7F_{16}$	80_{16}	81_{16}	82_{16}	83_{16}	84_{16}	85_{16}	86_{16}	87_{16}	88_{16}	89_{16}	$8A_{16}$	$8B_{16}$	$8C_{16}$	$8D_{16}$	$8E_{16}$	$8F_{16}$
7	90_{16}	91_{16}	92_{16}	93_{16}	94_{16}	95_{16}	96_{16}	97_{16}	98_{16}	99_{16}	$9A_{16}$	$9B_{16}$	$9C_{16}$	$9D_{16}$	$9E_{16}$	$9F_{16}$	$A0_{16}$	$A1_{16}$	$A2_{16}$	$A3_{16}$	$A4_{16}$	$A5_{16}$	$A6_{16}$	$A7_{16}$
8	$A8_{16}$	$A9_{16}$	AA_{16}	AB_{16}	AC_{16}	AD_{16}	AE_{16}	AF_{16}	$B0_{16}$	$B1_{16}$	$B2_{16}$	$B3_{16}$	$B4_{16}$	$B5_{16}$	$B6_{16}$	$B7_{16}$	$B8_{16}$	$B9_{16}$	BA_{16}	BB_{16}	BC_{16}	BD_{16}	BE_{16}	BF_{16}
9	$C0_{16}$	$C1_{16}$	$C2_{16}$	$C3_{16}$	$C4_{16}$	$C5_{16}$	$C6_{16}$	$C7_{16}$	$C8_{16}$	$C9_{16}$	CA_{16}	CB_{16}	CC_{16}	CD_{16}	CE_{16}	CF_{16}	$D0_{16}$	$D1_{16}$	$D2_{16}$	$D3_{16}$	$D4_{16}$	$D5_{16}$	$D6_{16}$	$D7_{16}$
10	$D8_{16}$	$D9_{16}$	DA_{16}	DB_{16}	DC_{16}	DD_{16}	DE_{16}	DF_{16}	$E0_{16}$	$E1_{16}$	$E2_{16}$	$E3_{16}$	$E4_{16}$	$E5_{16}$	$E6_{16}$	$E7_{16}$	$E8_{16}$	$E9_{16}$	EA_{16}	EB_{16}	EC_{16}	ED_{16}	EE_{16}	EF_{16}

The hexadecimal numbers in the boxes show the display RAM address.

Fig. 3 Screen constitution

REGISTERS DESCRIPTION

(1) Address $F0_{16}$

DA	Register	Contents		Remarks
		Status	Function	
0	PTC0	⓪	P0 output (port P0)	Port output control
		1	BLNK1* output	
1	PTC1	⓪	P1 output (port P1)	
		1	CO1* output	
2	PTC2	⓪	P2 output (port P2)	
		1	BLNK2* output	
3	PTC3	⓪	P3 output (port P3)	
		1	CO2* output	
4	PTD0	⓪	P0 output "L"	Port data control
		1	P0 output "H"	
5	PTD1	⓪	P1 output "L"	
		1	P1 output "H"	
6	PTD2	⓪	P2 output "L"	
		1	P2 output "H"	
7	PTD3	⓪	P3 output "L"	
		1	P3 output "H"	

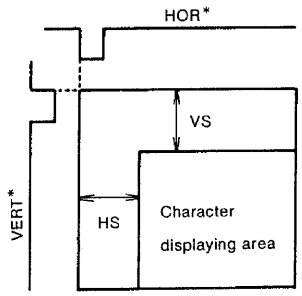
Note : The mark ○ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(2) Address $F1_{16}$

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">HP0
(LSB)</td><td>⓪</td><td rowspan="11">If HS is the horizontal display start location,
$HS = T \times (4 \sum_{n=0}^{5} 2^n HP_n + N)$.
T : The oscillation cycle of oscillator OSC1, OSC2
<table><tr><th>HSZ11</th><th>HSZ10</th><th rowspan="2">N</th></tr><tr><th>HSZ21</th><th>HSZ20</th></tr><tr><td>0</td><td>0</td><td>9</td></tr><tr><td>0</td><td>1</td><td>10</td></tr><tr><td>1</td><td>0</td><td>11</td></tr><tr><td>1</td><td>1</td><td>12</td></tr></table></td><td rowspan="11">Horizontal display start location is specified using the 6 bits from HP5 to HP0.
Note : HP5 to 0 = (000000_2) and (000001_2) setting is forbidden.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">HP1</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">HP2</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">HP3</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">HP4</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">HP5
(MSB)</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">TBASE0</td><td>⓪</td><td>No correction for the synchronous error by a noise.</td><td rowspan="4">The synchronized signal correction setting.</td></tr>
<tr><td>1</td><td>Correction for the synchronous error by a noise.</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">TBASE1</td><td>⓪</td><td>No correction for a lack of the synchronized signal.</td></tr>
<tr><td>1</td><td>Correction for a lack of the synchronized signal.</td></tr>
</table>

Note : The mark ○ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(3) Address $F2_{16}$

DA	Register	Contents		Remarks
		Status	Function	
0	VP0 (LSB)	⓪	If VS is the vertical display start location, $VS = H \times (4 \sum_{n=0}^{5} 2^n VP_n + 3)$. H : Cycle with the horizontal synchronizing pulse  	The vertical start location is specified using the 6 bits from VP5 to VP0.
		1		
1	VP1	⓪		
		1		
2	VP2	⓪		
		1		
3	VP3	⓪		
		1		
4	VP4	⓪		
		1		
5	VP5 (MSB)	⓪		
		1		
6	SEPV	⓪	Input both horizontal synchronization signal and vertical synchronization signal.	The contents of synchronization signal input in superimpose display is altered.
		1	Input the horizontal (composite) synchronization signal only.	
7	$\overline{INT}$/NON	⓪	Interlace	Scanning lines control (only in internal synchronization)
		1	Non-interlace	

Note : The mark ○ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(4) Address $F3_{16}$

DA	Register	Contents		Remarks
		Status	Function	
0	HSZ10	⓪	HSZ10 / HSZ11: 0 → 1T/1dot, 1 → 3T/1dot	Character size setting in the horizontal direction for the first line.
		1	HSZ10 / HSZ11: 0 → 2T/1dot, 1 → 4T/1dot	
1	HSZ11	⓪		
		1		
2	HSZ20	⓪	HSZ20 / HSZ21: 0 → 1T/1dot, 1 → 3T/1dot	Character size setting in the horizontal direction for the 2nd line to 10th line.
		1	HSZ20 / HSZ21: 0 → 2T/1dot, 1 → 4T/1dot	
3	HSZ21	⓪		
		1		
4	VSZ10	⓪	VSZ10 / VSZ11: 0 → 1H/1dot, 1 → 3H/1dot	Character size setting in the vertical direction for the first line.
		1	VSZ10 / VSZ11: 0 → 2H/1dot, 1 → 4H/1dot	
5	VSZ11	⓪		
		1		
6	VSZ20	⓪	VSZ20 / VSZ21: 0 → 1H/1dot, 1 → 3H/1dot	Character size setting in the vertical direction for the 2nd line to 10th line.
		1	VSZ20 / VSZ21: 0 → 2H/1dot, 1 → 4H/1dot	
7	VSZ21	⓪		
		1		

Note : The mark ○ arround the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(5) Address $F4_{16}$

DA	Register	Contents		Remarks
		Status	Function	
0	DSP0	⓪	Line 1 is in the display mode specified by BLK0 and BLK1.	DSP0 to DSP9 are each controlled independently.
		1	Line 1 is in a different display mode.	
1	DSP1	⓪	Line 2 is in the display mode specified by BLK0 and BLK1.	
		1	Line 2 is in a different display mode.	
2	DSP2	⓪	Line 3 is in the display mode specified by BLK0 and BLK1.	
		1	Line 3 is in a different display mode.	
3	DSP3	⓪	Line 4 is in the display mode specified by BLK0 and BLK1.	
		1	Line 4 is in a different display mode.	
4	DSP4	⓪	Line 5 is in the display mode specified by BLK0 and BLK1.	
		1	Line 5 is in a different display mode.	
5	DSP5	⓪	Line 6 is in the display mode specified by BLK0 and BLK1.	
		1	Line 6 is in a different display mode.	
6	DSP6	⓪	Line 7 is in the display mode specified by BLK0 and BLK1.	
		1	Line 7 is in a different display mode.	
7	DSP7	⓪	Line 8 is in the display mode specified by BLK0 and BLK1.	
		1	Line 8 is in a different display mode.	

BLK1	BLK0	DSPn	Display mode for line n
0	0	0	Border (Note1)
		1	Character
0	1	0	Character
		1	Border
1	0	0	Border
		1	Matrix-outline
1	1	0	Matrix-outline
		1	Character

DSPn in the generic name for DSP0 to DSP9

Note 1 : The display mode for line n is the border size, and for the other lines, the display mode is the character size.
If all DSPn (n : 0 to 9) are "0", the display mode is all line blanking OFF.
Note 2 : DSP8 and DSP9 are assigned to address $F5_{16}$.

Note : The mark ○ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(6) Address $F5_{16}$

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">DSP8</td><td>⓪</td><td>Line 9 is in the display mode specified by BLK0 and BLK1.</td><td rowspan="4">See the remarks of address $F4_{16}$.</td></tr>
<tr><td>1</td><td>Line 9 is in the different display mode.</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">DSP9</td><td>⓪</td><td>Line 10 is in the display mode specified by BLK0 and BLK1.</td></tr>
<tr><td>1</td><td>Line 10 is in the different display mode.</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">EXP0</td><td>⓪</td><td rowspan="4"><table><tr><th>EXP1 \ EXP0</th><th>0</th><th>1</th></tr><tr><td>0</td><td>Normal character + Blinking</td><td>Reversed character (No blinking)</td></tr><tr><td>1</td><td>Normal character + Exclusion</td><td>Reversed character + Exclusion</td></tr></table></td><td rowspan="4">For M35013-XXXSP, these registers are used to extend the function of the EXP bits in the addresses 0_{16} to EF_{16} of the display RAM.
For M35012-XXXSP, these registers are used to extend the function of the REV bits and BLINK bits in the addresses 0_{16} to EF_{16} of the display RAM.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">EXP1</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">TEST0</td><td>⓪</td><td rowspan="6">TEST0 to TEST2=(000_2)→Normal display
(010_2)→Space display</td><td rowspan="6"></td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">TEST1</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">TEST2</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">$\overline{N}/P$</td><td>⓪</td><td rowspan="2"><table><tr><th>$\overline{N}/P$ \ MPAL</th><th>0</th><th>1</th></tr><tr><td>0</td><td>NTSC</td><td>M-PAL</td></tr><tr><td>1</td><td>PAL</td><td>Do not use</td></tr></table></td><td rowspan="2">Synchronization signal is selected with this register and MPAL register (address $F6_{16}$).</td></tr>
<tr><td>1</td></tr>
</table>

Note : The mark ○ around the status value means the reset status by "L" level is input to $\overline{AC}$ pin.

(7) Address $F6_{16}$

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="4">0
1</td><td rowspan="4">BLINK0
BLINK1</td><td>0</td><td rowspan="4"><table><tr><th>BLINK1 \ BLINK0</th><th>0</th><th>1</th></tr><tr><td>0</td><td>Blinking OFF</td><td>Duty 25%</td></tr><tr><td>1</td><td>Duty 50%</td><td>Duty 75%</td></tr></table></td><td rowspan="4">Blinking duty ratio can be altered.</td></tr>
<tr><td>1</td></tr>
<tr><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td>2</td><td>BLINK2</td><td>0</td><td>Division of vertical synchronization signal into 1/64.
Cycle approximately 1 second.</td><td rowspan="2">Blinking cycle can be altered.</td></tr>
<tr><td></td><td></td><td>1</td><td>Division of vertical synchronization signal into 1/32.
Cycle approximately 0.5 second.</td></tr>
<tr><td>3</td><td>FSC</td><td>0</td><td>OSCIN oscillation frequency 4 × fsc</td><td rowspan="2">Oscillation frequency setting for OSCIN terminal (only effective with NTSC).</td></tr>
<tr><td></td><td></td><td>1</td><td>OSCIN oscillation frequency 2 × fsc</td></tr>
<tr><td>4</td><td>ALL24</td><td>0</td><td>Blanking with all 24 characters in matrix-outline size.</td><td rowspan="2">Horizontal display range can be altered when all characters are in matrix-outline size (Note 2).</td></tr>
<tr><td></td><td></td><td>1</td><td>Horizontal display period blanked.</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">MPAL</td><td>0</td><td rowspan="2"><table><tr><th>$\overline{N/P}$ \ MPAL</th><th>0</th><th>1</th></tr><tr><td>0</td><td>NTSC</td><td>M-PAL</td></tr><tr><td>1</td><td>PAL</td><td>Do not use</td></tr></table></td><td rowspan="2">Synchronization signal is selected with this register and $\overline{N/P}$ register (address $F5_{16}$).</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>6</td><td>PALH</td><td>0</td><td>Interlace 1
Noninterlace 1</td><td rowspan="2">In NTSC mode, status is "0".</td></tr>
<tr><td></td><td></td><td>1</td><td>Interlace 2
Noninterlace 2</td></tr>
<tr><td>7</td><td>EQP</td><td>0</td><td>Not include the equivalent pulse</td><td rowspan="2">Setting the contents of composite synchronized signal at non-interlace.</td></tr>
<tr><td></td><td></td><td>1</td><td>Include the equivalent pulse</td></tr>
</table>

Notes 1. The mark ○ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.
2. Fix to "0" this register at external synchronous.

(8) Address $F7_{16}$

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">PHASE0</td><td>⓪</td><td rowspan="8">
<table>
<tr><th>PHASE2</th><th>PHASE1</th><th>PHASE0</th><th>NTSC Phase angle(color)</th><th>PAL phase angle(color)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>(Black)</td><td>(Black)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>π /2 [rad.]</td><td>±π /2 [rad.]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>7π /4 [rad.]</td><td>∓π /4 [rad.]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>same phase</td><td>same phase</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>π [rad.]</td><td>±π [rad.]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3π /4 [rad.]</td><td>±3π /4 [rad.]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>3π /2 [rad.]</td><td>∓π /2 [rad.]</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>(White)</td><td>(White)</td></tr>
</table>
</td><td rowspan="8">Raster color setting. Coloring by composite video signals means that the phase angle of the background color signals for the color burst signals can be varied. The angle can be varied in units of π /4 rad.
This differs from coloring by RGB output.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">PHASE1</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">PHASE2</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">LEVEL0</td><td>⓪</td><td>Internal bias OFF</td><td rowspan="2">Generation of composite video signal bias potential</td></tr>
<tr><td>1</td><td>Internal bias ON</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">BR</td><td>⓪</td><td rowspan="6">
<table>
<tr><th>BB</th><th>BG</th><th>BR</th><th>NTSC phase angle(color)</th><th>PAL phase angle(color)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>(Black)</td><td>(Black)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>π /2 [rad]</td><td>±π /2 [rad.]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>7π /4 [rad.]</td><td>∓π /4 [rad.]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>same phase</td><td>same phase</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>π [rad.]</td><td>±π [rad.]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3π /4 [rad.]</td><td>±3π /4 [rad.]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>3π /2 [rad.]</td><td>∓π /2 [rad]</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>(White)</td><td>(White)</td></tr>
</table>
</td><td rowspan="6">Character background color setting.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">BG</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">BB</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">BLKHF</td><td>⓪</td><td>The halftone displaying "OFF" in superimpose</td><td rowspan="2">This register is available in the superimpose displaying only.</td></tr>
<tr><td>1</td><td>The halftone displaying "ON" in superimpose</td></tr>
</table>

Note : The mark ○ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(9) Address $F8_{16}$

DA	Register	Contents		Remarks
		Status	Function	
0	BLK0	⓪		Display mode variable
		1		
1	BLK1	⓪		
		1		

BLK1 \ BLK0	0	1
0	Blanking OFF	Character size
1	Border size	Matrix-outline size

DA	Register	Status	Function	Remarks
2	EX	⓪	External synchronization	Synchronization signal switching
		1	Internal synchronization	
3	RAMERS	⓪	RAM not erased	This register does not have the function as register. If RAM is erase continuously, set DSPON (address $F8_{16}$) to "0".
		1	RAM erased	
4	STOPIN	⓪	Oscillaion of OSCIN, OSCOUT for synchronization signals.	OSCIN oscillation stop (Note 1)
		1	Stop oscillation of OSCIN, OSCOUT, for synchronization signals.	
5	STOP1	⓪	Oscillation of OSC1, OSC2 for display.	OSC1 and OSC2 oscillation switching. To stop the oscillation, set $\overline{CS}$ pin to "H" level and DSPON (address $F8_{16}$) to "0".
		1	Stop the oscillation OSC1, OSC2 for display.	
6	CONT7F	⓪	Normal write mode.	Usually "0" fix. Writing mode of the serial data input switching. (Note 2) For M35012-XXXSP, continuously writing mode (character code FF_{16}).
		1	Continuously writing mode (character code $7F_{16}$)*	
7	DSPON	⓪	Display OFF	Display can be altered.
		1	Display ON	

Notes 1. When crystal oscillation move from external synchronous to internal synchronous at stop state (STOPIN=1), leave the crystal oscillation state (STOPIN=0) before 1V (vertical synchronous NTSC, M-PAL about 16.7ms, PAL 20ms) or more.
2. The mark ○ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

DISPLAY FORMS

M35013-XXXSP has the following five display forms as the blanking function, when CO1 *, BLNK1 *, CO2 *, and BLNK2* are output.

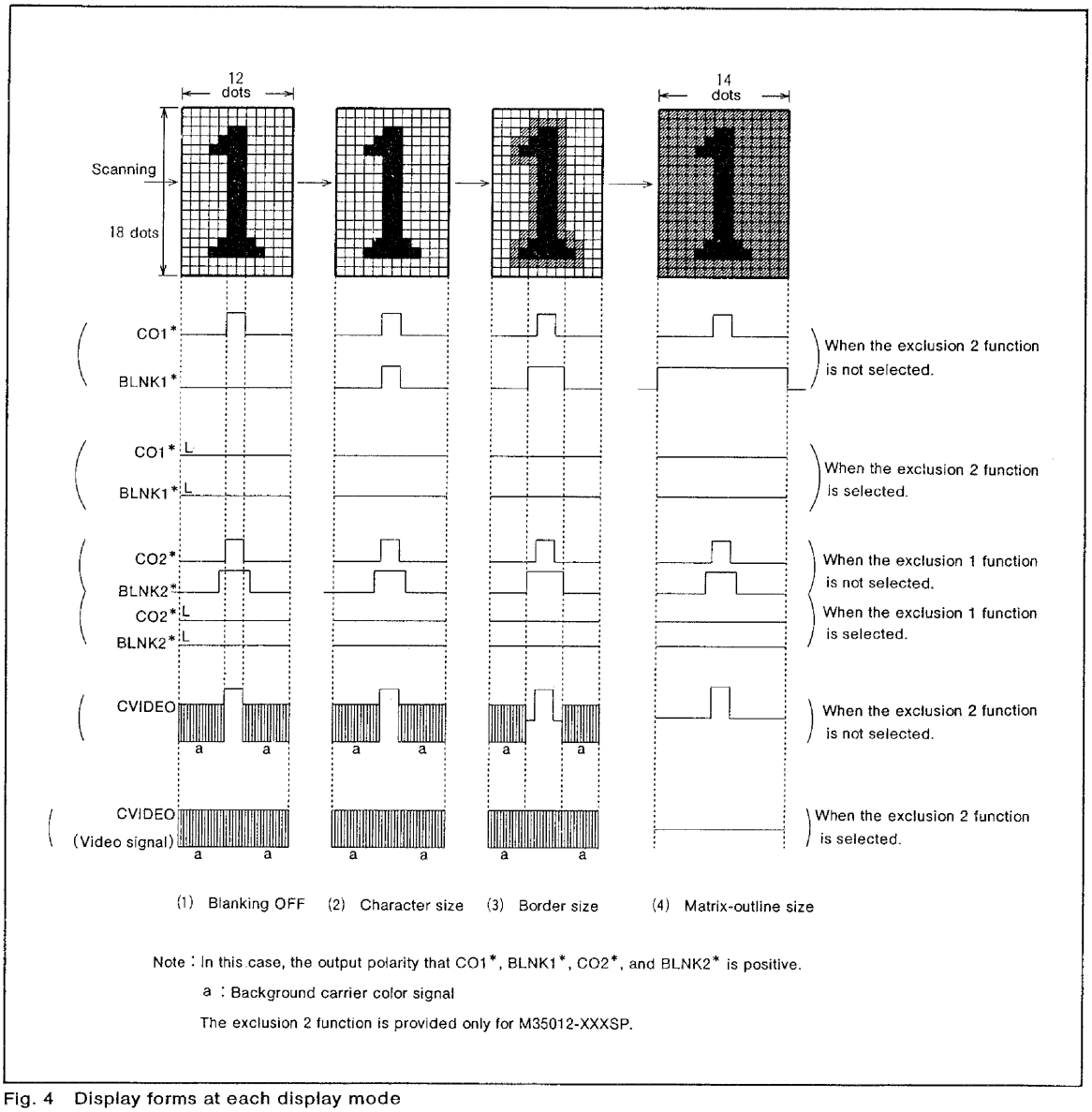
(1) Blanking OFF : Blanking output signal (BLNK*) is cut off.

(2) Character size : Blanking same as the character size.

(3) Border size : Blanking the background as a size from character.

(4) Matrix-outline size : Blanking the background as a size from all character font size.

This display format allows each line (from the first line to the tenth line) to be controlled independently, so that two kinds of display formats can be combined on the same screen.



Note : In this case, the output polarity that CO1*, BLNK1*, CO2*, and BLNK2* is positive.

a : Background carrier color signal

The exclusion 2 function is provided only for M35012-XXXSP.

Fig. 4 Display forms at each display mode

EXCLUSION FUNCTION

For M35013-XXXSP, the function expansion that is set with the EXP1 and EXP0 registers (DA3 and DA2 of address $F5_{16}$) is performed when "1" is set to DA7 of display RAM (EXP bit).

Table 1 Display form of M35013-XXXSP

Register		Display form
EXP1	EXP0	
0	0	Normal character + Blinking
0	1	Reversed character (no blinking)
1	0	Normal character + Exclusion 1
1	1	Reversed character + Exclusion 1

For M35012-XXXSP, the displays shown in table 2 are available with the combination of DA9 (BLINK bit), DAA (REV bit) of display RAM and EXP1, EXP0 register (DA3 and DA2 of address $F5_{16}$).

When the exclusion 1 function is selected, CO2 * and BLNK2* side are not displayed.

When the exclusion 2 function is selected, CO1*, BLNK1*, and video signal side are not displayed.

The character of exclusion 2 and exclusion 1 are prohibited to be next to each other horizontally. Insert "FF_{16}" of character between the character of exclusion 2 and that of exclusion 1.

Table 2 Display form of M35012-XXXSP

Register		RAM		Display form
EXP1	EXP0	REV	BLINK	
0	0	0	0	Normal character
		0	1	Normal character + Blinking
		1	0	Reversed character
		1	1	Reversed character + Blinking
0	1	0	0	Normal character + Exclusion 2
		0	1	Normal character + Blinking + Exclusion 1
		1	0	Reversed character + Exclusion 2
		1	1	Reversed character + Blinking + Exclusion 1
1	0	0	0	Normal character
		0	1	Normal character + Exclusion 1
		1	0	Reversed character
		1	1	Reversed character + Exclusion 1
1	1	0	0	Normal character
		0	1	Normal character + Blinking
		1	0	Normal character + Exclusion 1
		1	1	Normal character + Blinking + Exclusion 1

The figure 5 and 6 show the display examples using ports P0 to P3 (digital output).

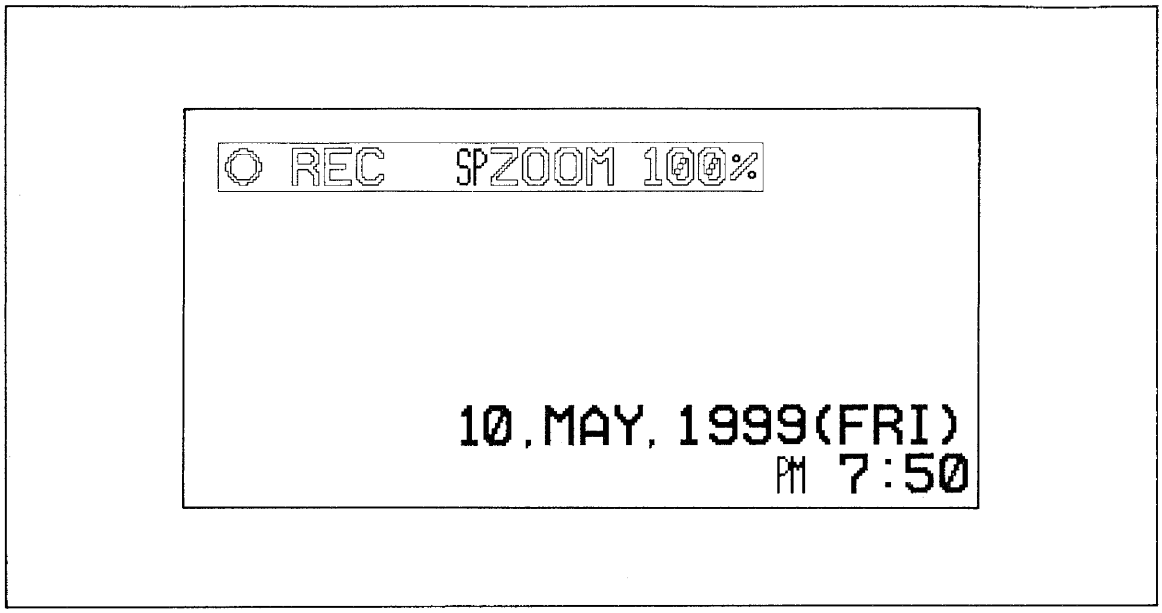


Fig. 5 Display example using ports P0(BLNK1*) and P1(CO1*) (display line)

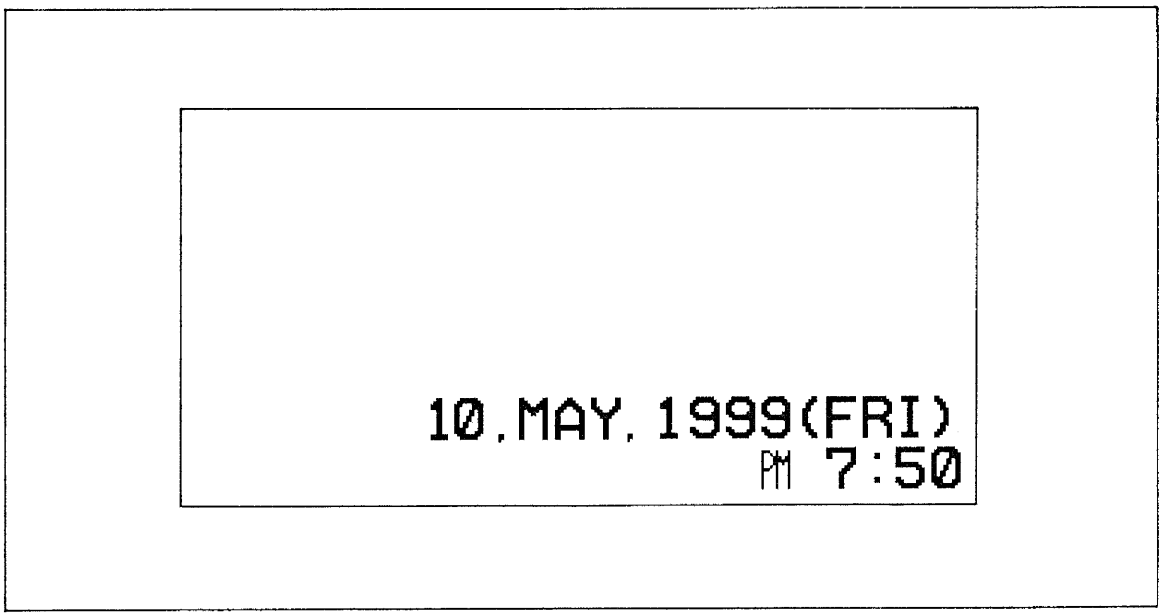


Fig. 6 Display example using ports P2(BLNK2*) and P3(CO2*) (record line)

DATA INPUT EXAMPLE

Data of display RAM and display control registers can be set by the serial input function. Example of data setting at M35013-XXXSP is shown in Figure 7, and example of data setting at M35012-XXXSP is shown in Figure 8.

No.	Memory Contents		DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0
	Address/Data	Addition								
1	Address $F8_{16}$	Display OFF	1	1	1	1	1	0	0	0
2	Data ($F8_{16}$)		0	0	0	0	1	×	×	×
3	Data (00_{16})	Setting to display RAM (address 00_{16} to EF_{16}) and registers (addresses $F0_{16}$ to $F8_{16}$)	EXP	C_6	C_5	C_4	C_3	C_2	C_1	C_0
4	Data (01_{16})		EXP	C_6	C_5	C_4	C_3	C_2	C_1	C_0
	⋮						⋮			
242	Data (EF_{16})		EXP	C_6	C_5	C_4	C_3	C_2	C_1	C_0
243	Data ($F0_{16}$)		PTD 3	PTD 2	PTD 1	PTD 0	PTC 3	PTC 2	PTC 1	PTC 0
244	Data ($F1_{16}$)		0	0	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
245	Data ($F2_{16}$)		0	0	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
246	Data ($F3_{16}$)		VSZ 21	VSZ 20	VSZ 11	VSZ 10	HSZ 21	HSZ 20	HSZ 11	HSZ 10
247	Data ($F4_{16}$)		DSP 7	DSP 6	DSP 5	DSP 4	DSP 3	DSP 2	DSP 1	DSP 0
248	Data ($F5_{16}$)		$\overline{N}$/P	0	0	0	EXP 1	EXP 0	DSP 9	DSP 8
249	Data ($F6_{16}$)		EQP	PAL H	MPAL	ALL 24	FSC	BLINK 2	BLINK 1	BLINK 0
250	Data ($F7_{16}$)		BLKHF	BB	BG	BR	1	PHASE 2	PHASE 1	PHASE 0
251	Data ($F8_{16}$)	Display ON	1	0	0	0	0	EX	BLK 1	BLK 0

Fig. 7 Example of data setting by the serial input function (M35013-XXXSP)

No.	Memory Contents		DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
	Address/Data	Addition																
1	Address $F8_{16}$	Display OFF	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0
2	Data ($F8_{16}$)		0	0	0	0	0	0	0	0	0	0	0	0	1	×	×	×
3	Data (00_{16})		0	0	0	0	0	REV	BLINK	0	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
4	Data (01_{16})		0	0	0	0	0	REV	BLINK	0	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
	⋮										⋮							
242	Data (EF_{16})	Setting to display RAM (address 00_{16} to EF_{16}) and registers (addresses $F0_{16}$ to $F8_{16}$)	0	0	0	0	0	REV	BLINK	0	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
243	Data ($F0_{16}$)		0	0	0	0	0	0	0	0	PTD 3	PTD 2	PTD 1	PTD 0	PTC 3	PTC 2	PTC 1	PTC 0
244	Data ($F1_{16}$)		0	0	0	0	0	0	0	0	0	0	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
245	Data ($F2_{16}$)		0	0	0	0	0	0	0	0	0	0	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
246	Data ($F3_{16}$)		0	0	0	0	0	0	0	0	VSZ 21	VSZ 20	VSZ 11	VSZ 10	HSZ 21	HSZ 20	HSZ 11	HSZ 10
247	Data ($F4_{16}$)		0	0	0	0	0	0	0	0	DSP 7	DSP 6	DSP 5	DSP 4	DSP 3	DSP 2	DSP 1	DSP 0
248	Data ($F5_{16}$)		0	0	0	0	0	0	0	0	$\overline{N}$/P	0	0	0	EXP 1	EXP 0	DSP 9	DSP 8
249	Data ($F6_{16}$)		0	0	0	0	0	0	0	0	EQP	PALH	MPAL	ALL 24	FSC	BLINK 2	BLINK 1	BLINK 0
250	Data ($F7_{16}$)		0	0	0	0	0	0	0	0	BLKHF	BB	BG	BR	1	PHASE 2	PHASE 1	PHASE 0
251	Data ($F8_{16}$)	Display ON	0	0	0	0	0	0	0	0	1	0	0	0	0	EX	BLK 1	BLK 0

Fig. 8 Example of data setting by the serial input function (M35012-XXXSP)

SERIAL DATA INPUT TIMING

At the M35013-XXXSP

(1) Serial data should be input with the LSB first.
(2) The address consists of 8 bits.
(3) The data consists of 8 bits.
(4) The 8 bits in the SCK after the $\overline{CS}$ signal has fallen are the address, and for succeeding input data, the address is incremented every 8 bits.

At the M35012-XXXSP

(1) Serial data should be input with the LSB first.
(2) The address consists of 16 bits.
(3) The data consists of 16 bits.
(4) The 16 bits in the SCK after the $\overline{CS}$ signal has fallen are the address, and for succeeding input data, the address is incremented every 16 bits.

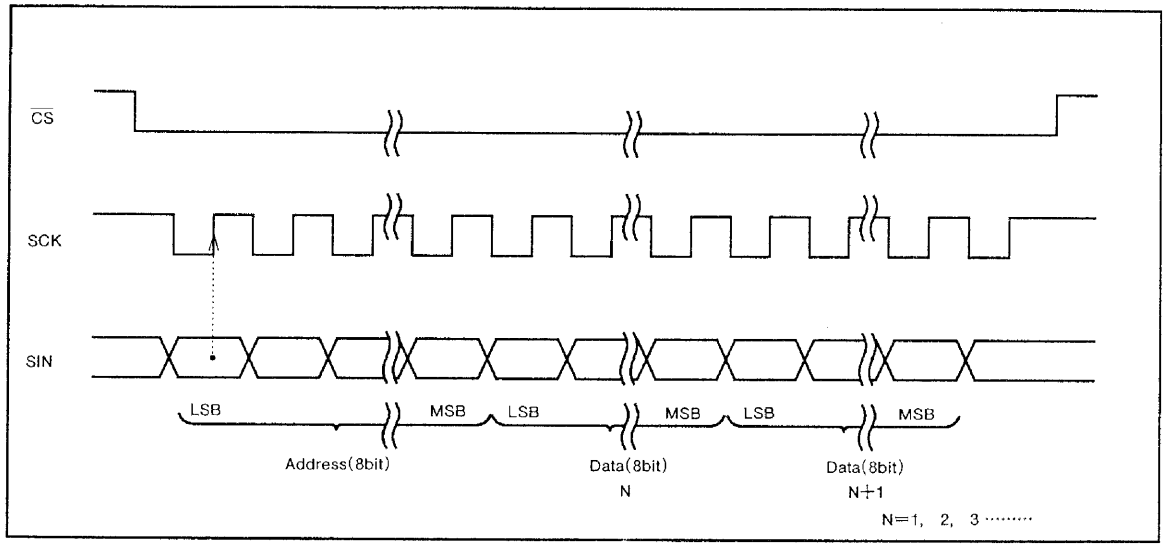


Fig. 9 Serial input timing (M35013-XXXSP)

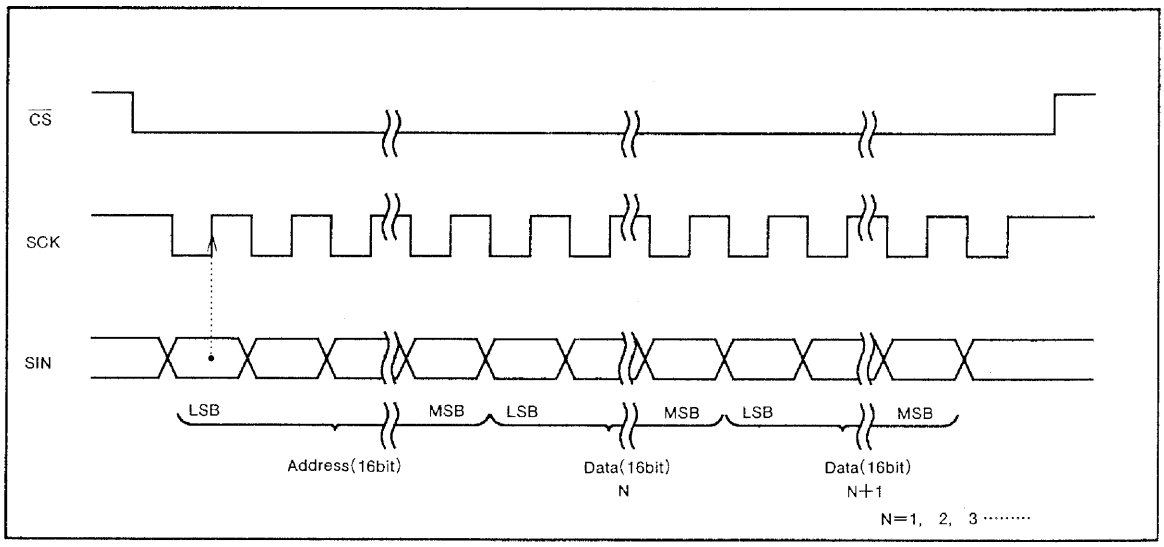


Fig. 10 Serial input timing (M35012-XXXSP)

CONT7F FUNCTION

When the register CONT7F (DA6 of address $F8_{16}$) is set to "1" and data input as the timing shown in Figure 11, the character code $7F_{16}$* (blank) can be set to display RAM automatically. However, be necessary to set the hold time. While this function is operating, never stop the display oscillation OSC1 and OSC2, and set the register STOP1 (DA5 of address $F8_{16}$) to "0".

* For M35012-XXXSP, the character code FF_{16} (blank) can be set to display RAM automatically.

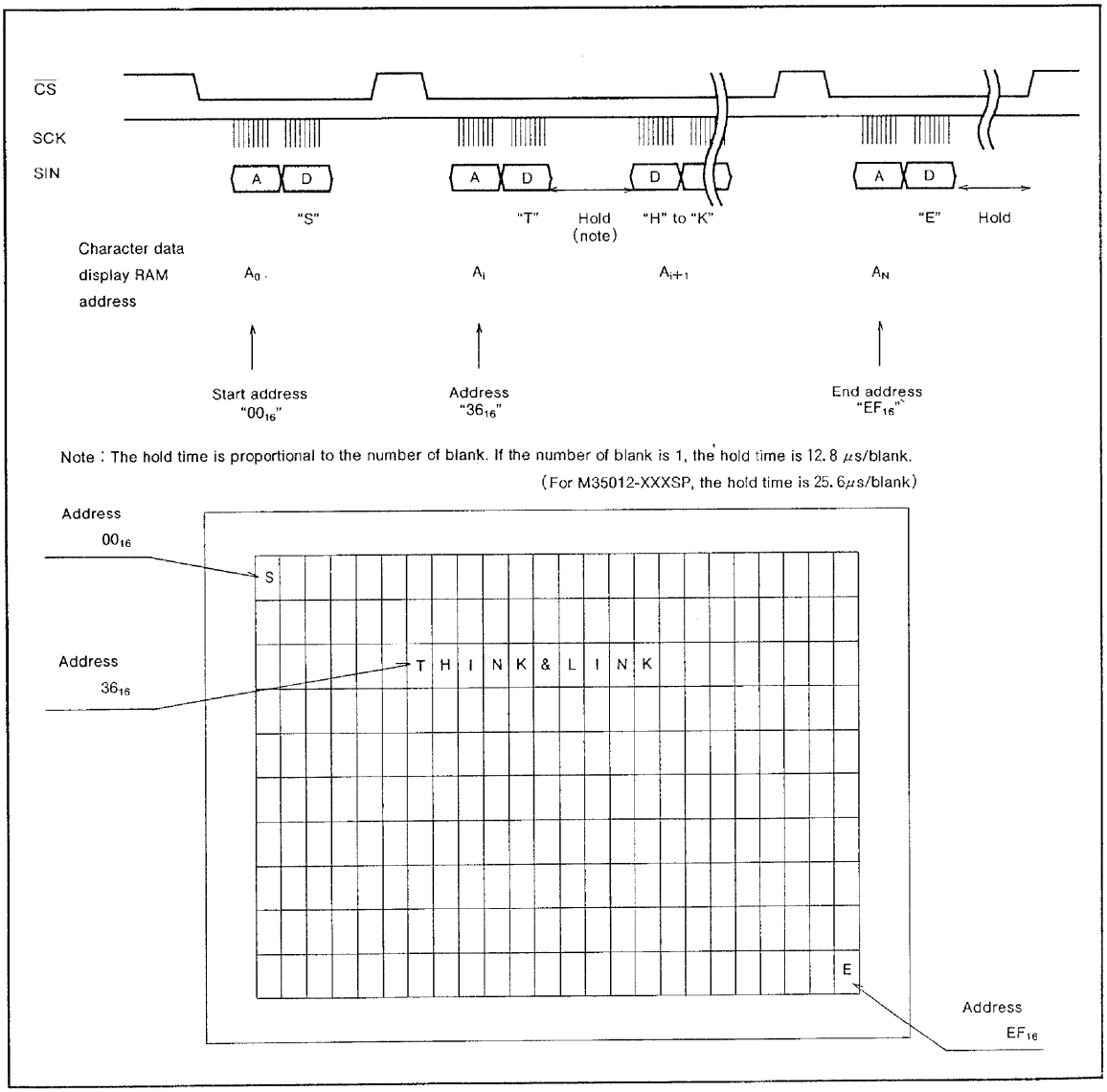


Fig. 11 CONT7F functional timing

TIME BASE (SYNCHRONOUS SIGNAL CORRECTION) FUNCTION

Time base function can correct the errors from the lost synchronous signal or disordered synchronization by a noise, using the reference clock fosc1.

The following are the correction method.

(1) Time base 0—TBASE0 (DA6 of address $F1_{16}$)="1".
- Cut-off a noise effect to synchronous signal.
- Cut-off a noise during D period of Figure 12.

(2) Time base 1—TBASE1 (DA7 of address $F1_{16}$)="1"
- Correct the lost synchronous signal.
- Generate the pulse if the synchronous signal has not input during C period of Figure 12. And stop to display the character till the next synchronous signal is input.

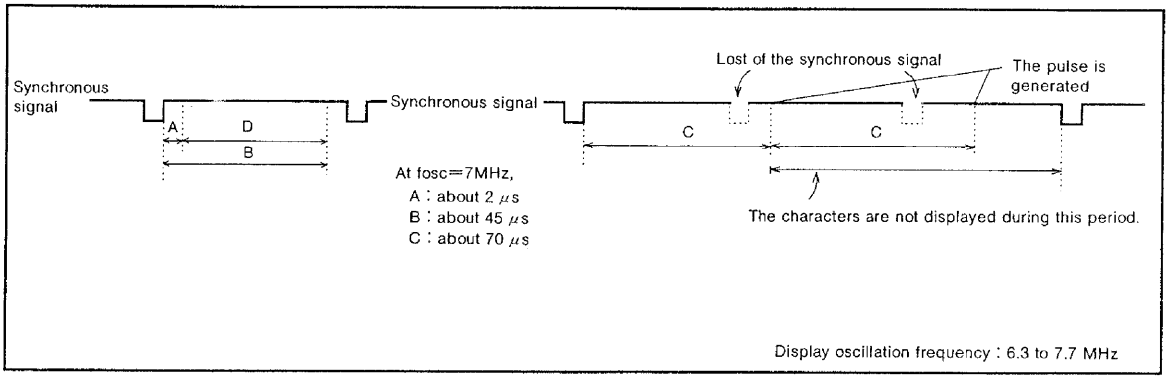


Fig. 12 Example of time base function

CHARACTER FONT

Images are composed on a 12 × 18 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

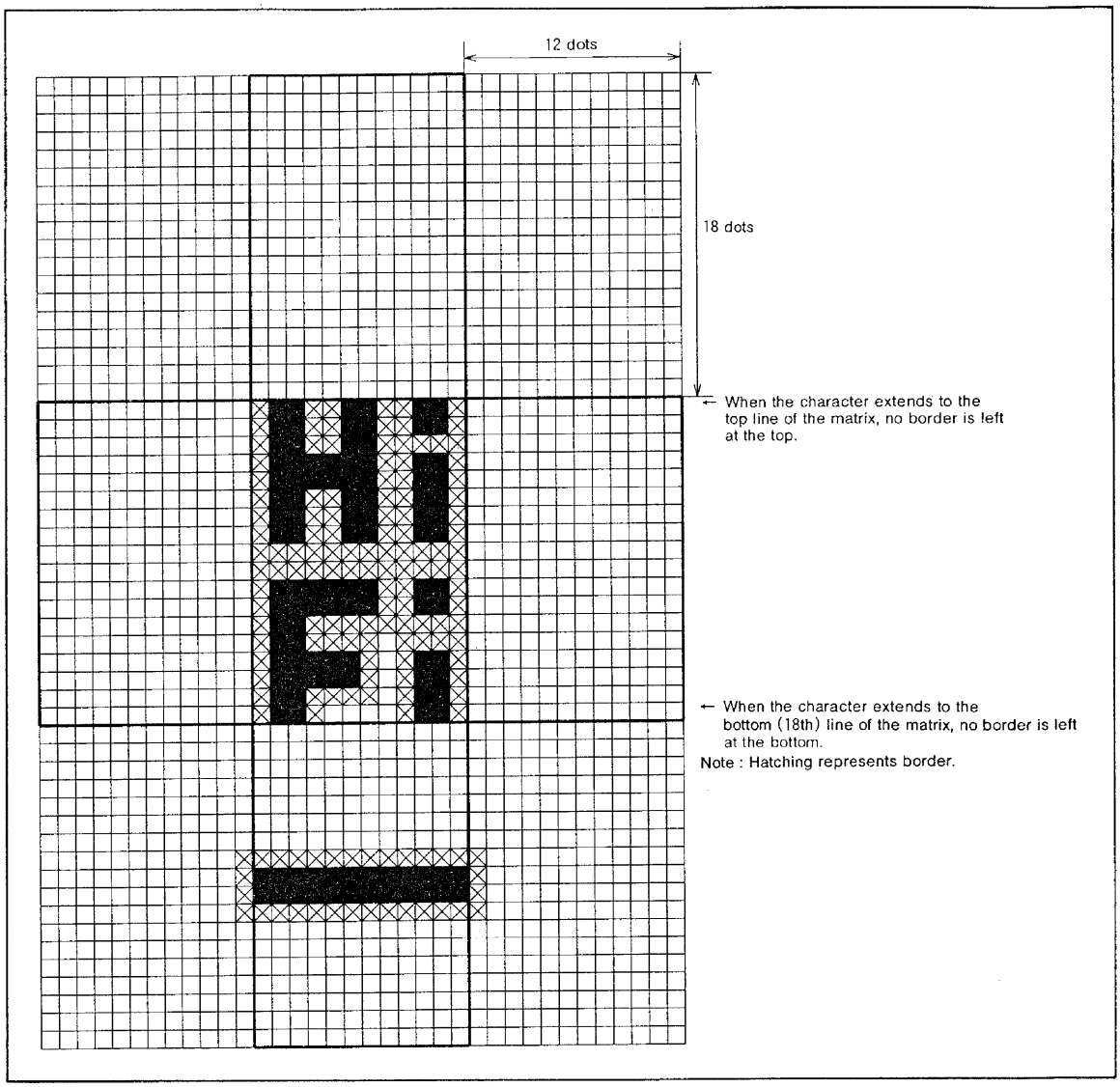


Fig. 13 Character font and border

Character code $7F_{16}$ is fixed as blank, without a background at the M35013-XXXSP.
Character code FF_{16} is fixed as blank, without a background at the M35012-XXXSP.

TIMING REQUIREMENTS (T_a=−20°C to +70°C, V_{DD}=5±0.5V, unless otherwise noted)

Serial data input at the M35013-XXXSP

Symbol	Parameter	Limits			Unit	Remarks
		Min.	Typ.	Max.		
$t_{w(SCK)}$	SCK width	200	—	—	ns	See Figure 14
$t_{su(\overline{CS})}$	$\overline{CS}$ setup time	200	—	—	ns	
$t_{h(\overline{CS})}$	$\overline{CS}$ hold time	2	—	—	μs	
$t_{su(SIN)}$	SIN setup time	200	—	—	ns	
$t_{h(SIN)}$	SIN hold time	200	—	—	ns	
t_{word}	1 word writing time	5	—	—	μs	

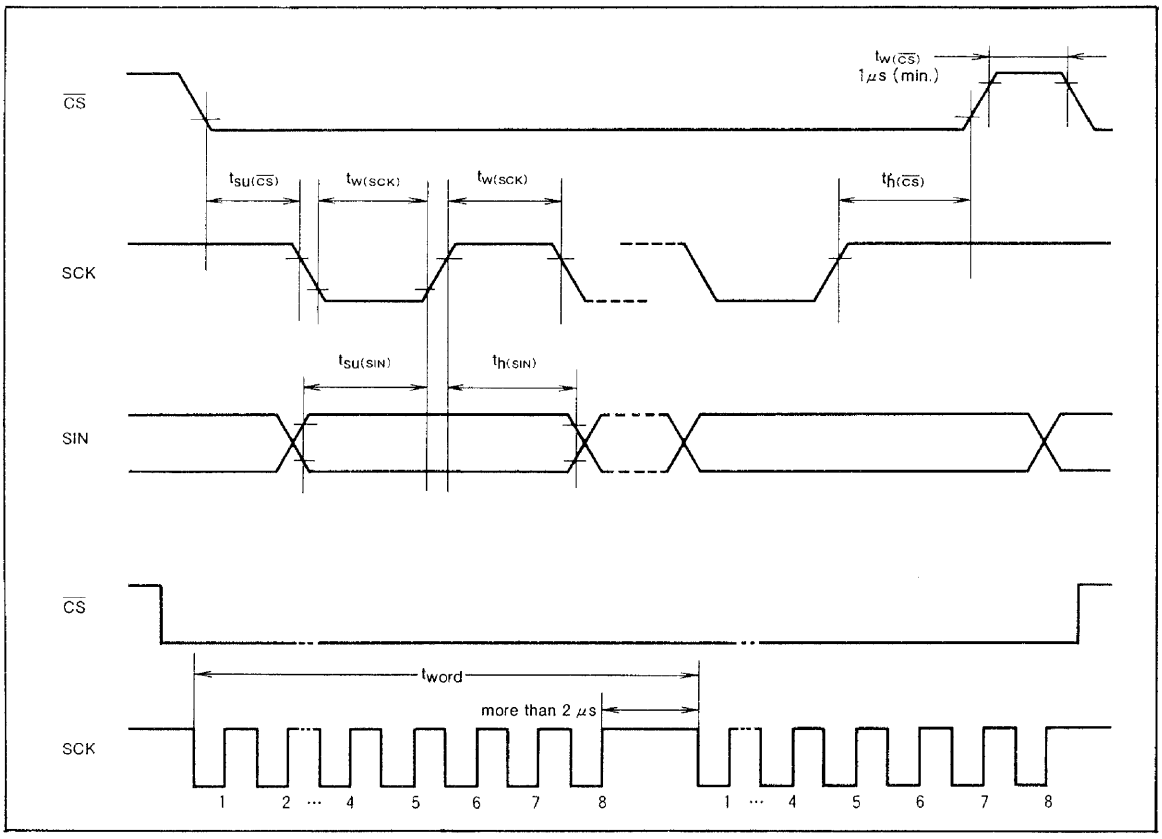


Fig. 14 Serial input timing requirements (M35013-XXXSP)

TIMING REQUIREMENTS (T_a=−20℃ to +70℃, V_{DD}=5±0.5V, unless otherwise noted)

Serial data input at the M35012-XXXSP

Symbol	Parameter	Limits			Unit	Remarks
		Min.	Typ.	Max.		
t_w(SCK)	SCK width	200	—	—	ns	See Figure 15
$t_{su(\overline{CS})}$	$\overline{CS}$ setup time	200	—	—	ns	
$t_{h(\overline{CS})}$	$\overline{CS}$ hold time	2	—	—	μs	
$t_{su(SIN)}$	SIN setup time	200	—	—	ns	
$t_{h(SIN)}$	SIN hold time	200	—	—	ns	
t_{word}	1 word writing time	10	—	—	μs	

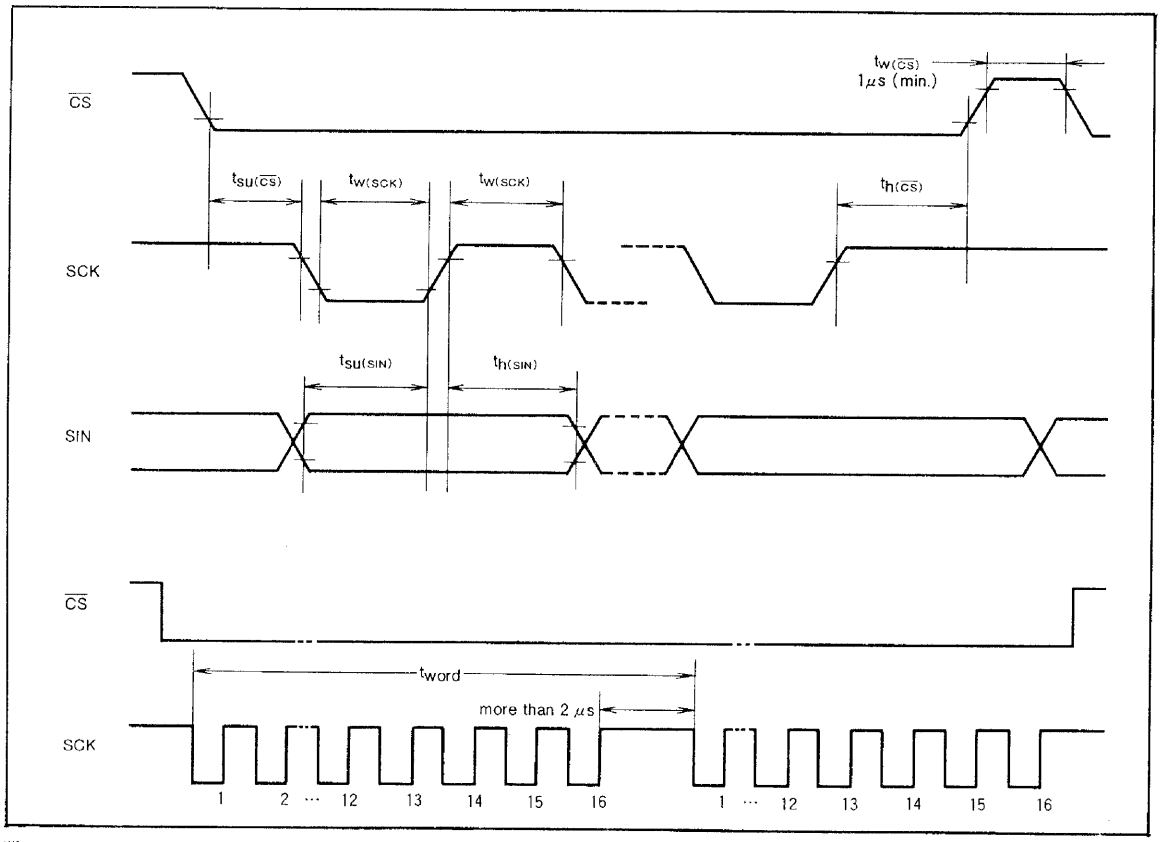


Fig. 15 Serial input timing requirements (M35012-XXXSP)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage	With respect to V_{SS}.	−0.3 to 6.0	V
V_I	Input voltage		$V_{SS}-0.3 \leqq V_I \leqq V_{DD}+0.3$	V
V_O	Output voltage		$V_{SS} \leqq V_O \leqq V_{DD}$	V
P_d	Power dissipation	T_a=25℃	300	mW
T_{opr}	Operating temperature		−20 to 70	℃
T_{stg}	Storage temperature		−40 to 125	℃

RECOMMENDED OPERATING CONDITIONS (V_{DD}=5V, T_a=−20 to 70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{DD}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	"H" level input voltage SIN, SCK, $\overline{CS}$, $\overline{AC}$, HOR*, VERT*	0.8V_{DD}	V_{DD}	V_{DD}	V
V_{IL}	"L" level input voltage SIN, SCK, $\overline{CS}$, $\overline{AC}$, HOR*, VERT*	0	0	0.2V_{DD}	V
VCVIN	Composite-video signal input voltage CVIN	—	2V_{P-P}	—	V
f_{OSC1}	Oscillating frequency for display	6.3	7.0	7.7	MHz
f_{OSCIN}	Oscillating frequency for synchronized signal	—	14.30 14.32 17.73	—	MHz

ELECTRICAL CHARACTERISTICS (V_{DD}= 5 V, f_{OSC1}=7.0MHz, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	T_a=−20 to 70℃	4.5	5.0	5.5	V
I_{DD}	Supply current		—	—	20	mA
V_{OH}	"H" level output voltage, P0 to P3	V_{DD}=4.5V, I_{OH}=0.4mA	3.5	—	—	V
V_{OL}	"L" level output voltage, P0 to P3	V_{DD}=4.5V, I_{OL}=0.4mA	—	—	0.4	V
R_I	Pull-up resistance SCK, $\overline{AC}$, $\overline{CS}$, SIN,		10	30	100	kΩ

VIDEO SIGNAL INPUT CONDITIONS (V_{DD}=5V, T_a=−20 to 70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{IN-SC}	Composite-video signal input clamp voltage	Sync-chip voltage	—	1.5	—	V

Note for Supplying Power

Timing of power supplying to $\overline{AC}$ pin

The internal circuit of M35012-XXXSP/M35013-XXXSP is reset when the level of the auto clear input pin $\overline{AC}$ is "L". This pin is hysteresis input with the pull-up resistor. The timing about power supplying of $\overline{AC}$ pin is shown in Figure 16.

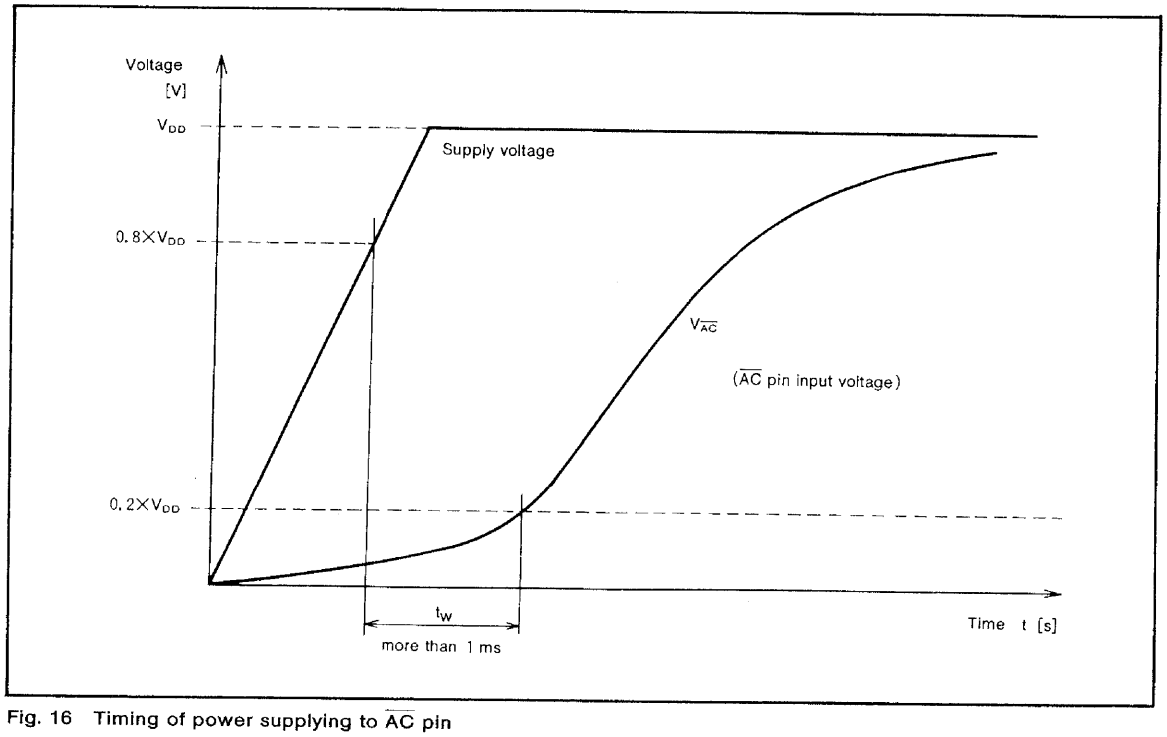


Fig. 16 Timing of power supplying to $\overline{AC}$ pin

After supplying the power (V_{DD} and V_{SS}) to M35012-XXXSP/ M35013-XXXSP and the supply voltage becomes more than 0.8 × V_{DD}, it needs to keep V_{IL} time; tw of the $\overline{AC}$ pin for more than 1ms.

Power supply timing about $V_{DD}1$ pin and $V_{DD}2$ pin.

The power need to supply to $V_{DD}1$ and $V_{DD}2$ at a time, though it is separated perfectly between the $V_{DD}1$ as the digital line and the $V_{DD}2$ as the analog line.

PRECAUTION FOR USE

Notes on noise and latch-up

In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{DD} pin and V_{SS} pin using a heavy wire.

Ask your crystal oscillator manufacture to examine the matching conditions between this device and the crystal oscillator.

STANDARD ROM TYPE : M35013-001SP

M35013-001SP is a standard ROM type of M35013-XXXSP. The input/output polarity and character patterns are fixed to the contents of Table 3 and Figure 17 to 19.

Table 3 Input/output polarity of pins

Pin name	I/O	Polarity
HOR*	Input	Negative
VERT*	Input	Negative
P3(CO2*)	Output	Positive
P2(BLNK2*)	Output	Positive
P1(CO1*)	Output	Positive
P0(BLNK1*)	Output	Positive

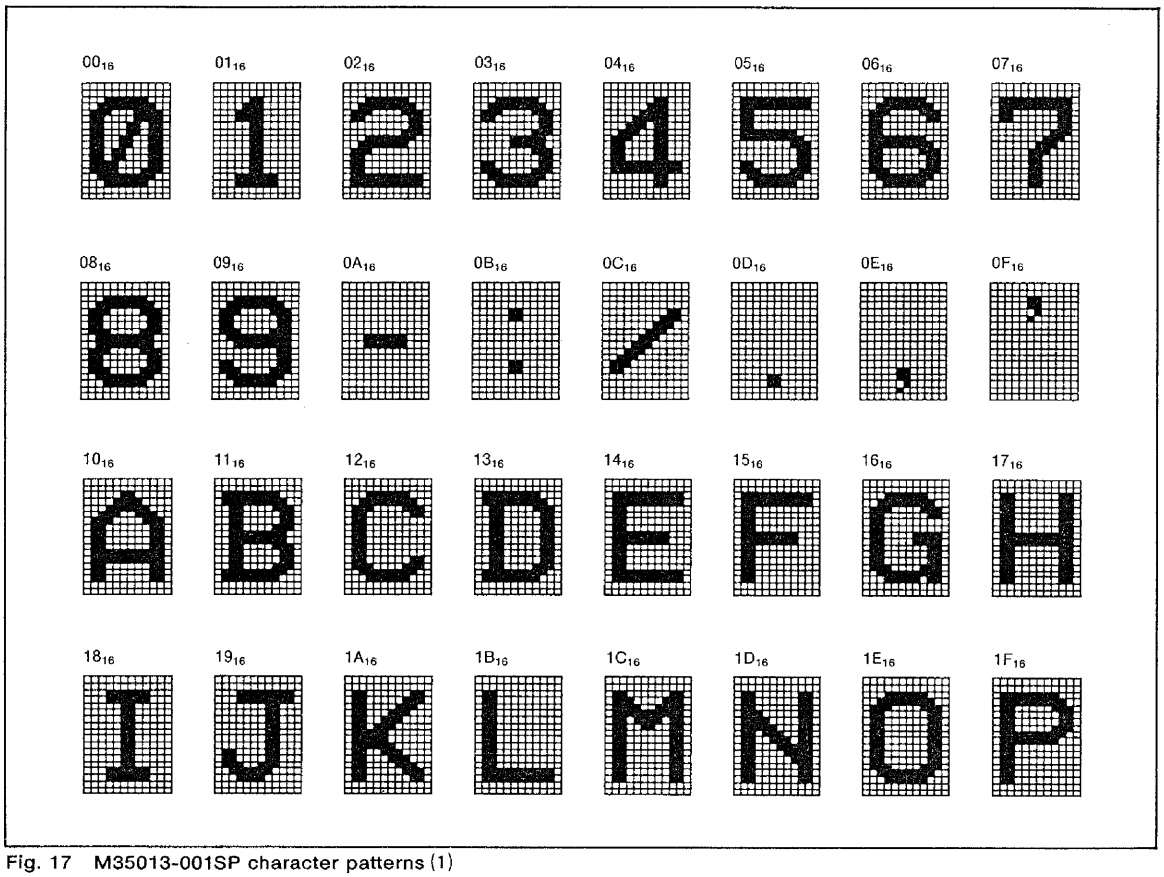


Fig. 17 M35013-001SP character patterns (1)

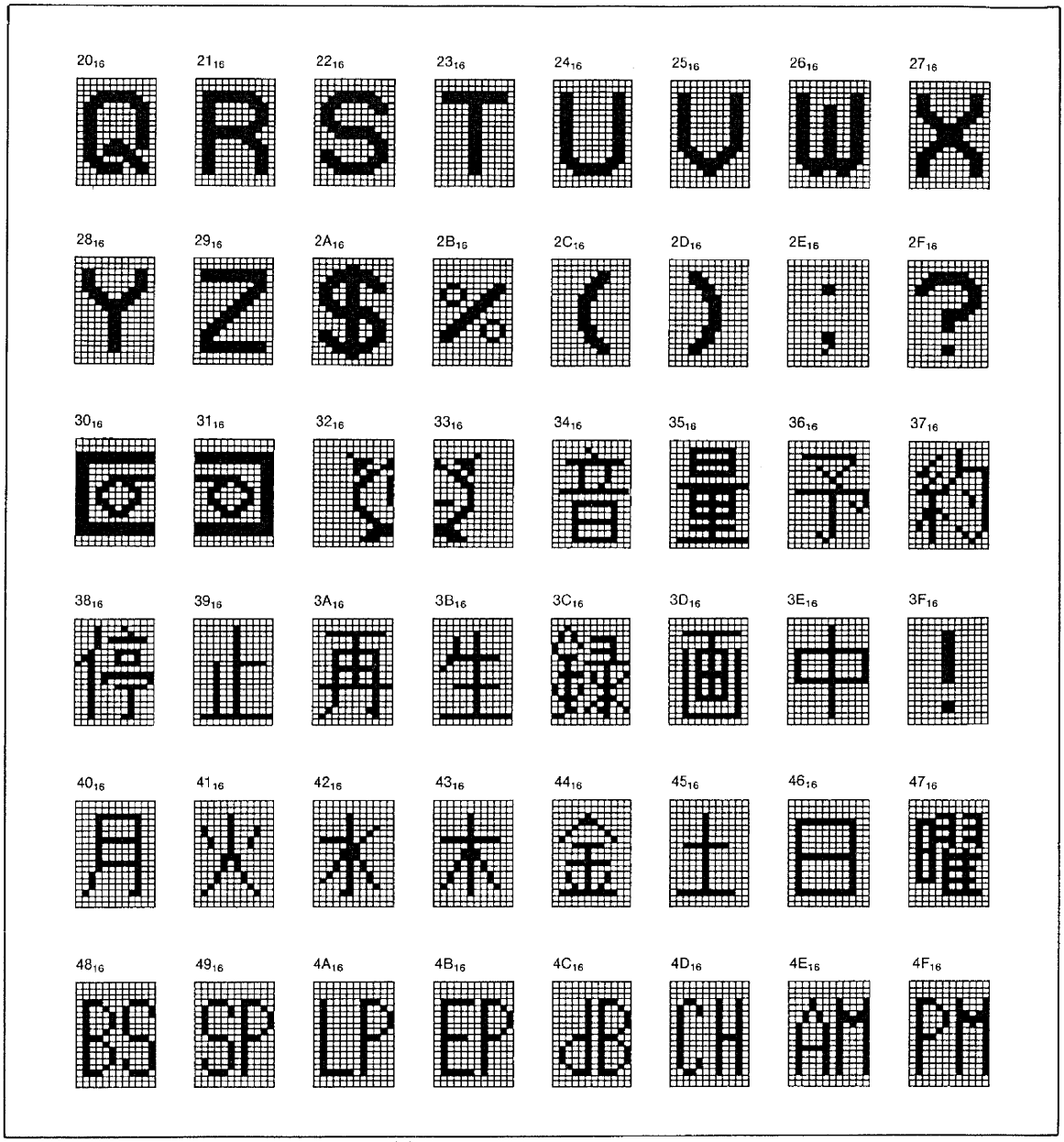


Fig. 18 M35013-001SP character patterns (2)

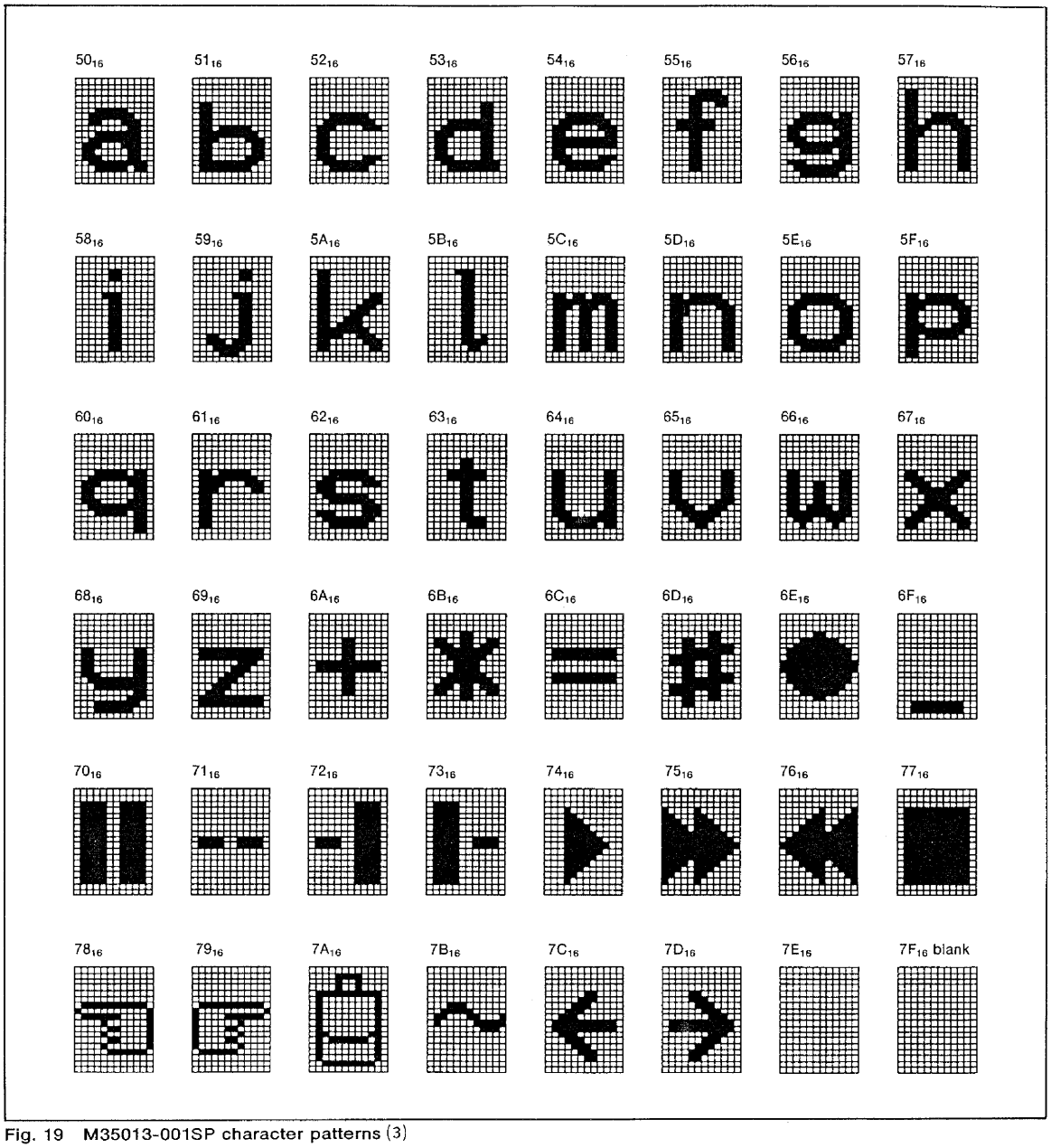


Fig. 19 M35013-001SP character patterns (3)

STANDARD ROM TYPE : M35012-001SP

M35012-001SP is a standard ROM type of M35012-XXXSP. The input/output polarity and character patterns are fixed to the contents of Table 4 and Figure 20 to 25.

Table 4 Input/output polarity of pins

Pin name	I/O	Polarity
HOR*	Input	Negative
VERT*	Input	Negative
P3(CO2*)	Output	Positive
P2(BLNK2*)	Output	Positive
P1(CO1*)	Output	Positive
P0(BLNK1*)	Output	Positive

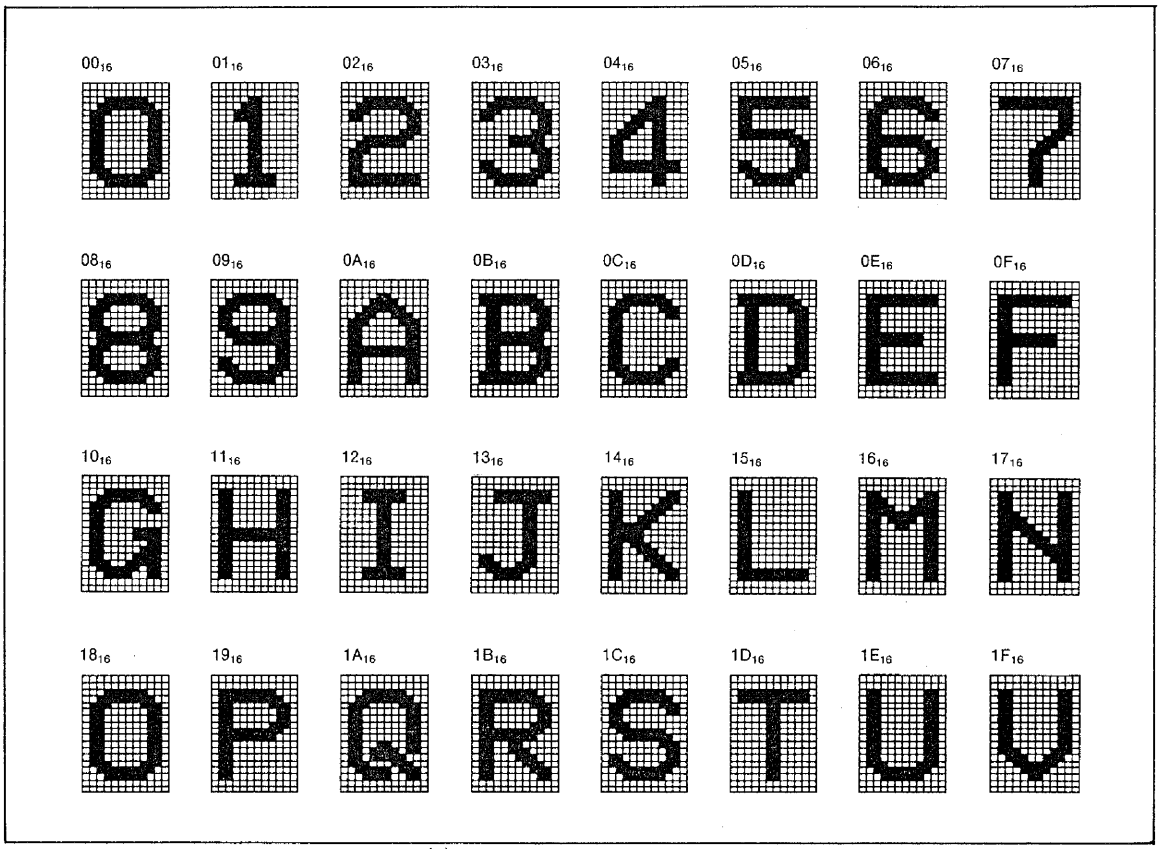


Fig. 20 M35012-001SP character patterns (1)

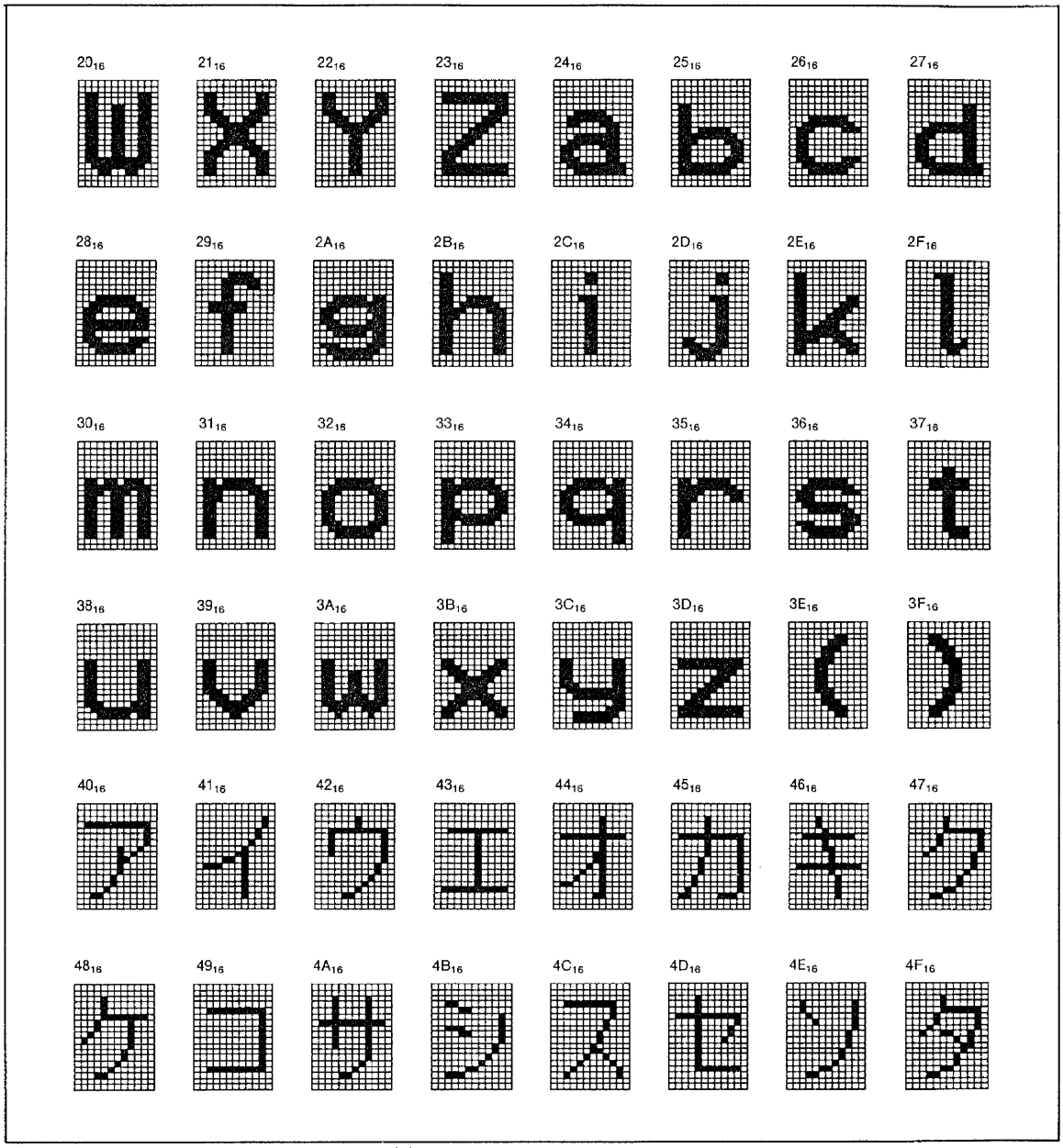


Fig. 21 M35012-001SP character patterns (2)

Fig. 22 M35012-001SP character patterns (3)

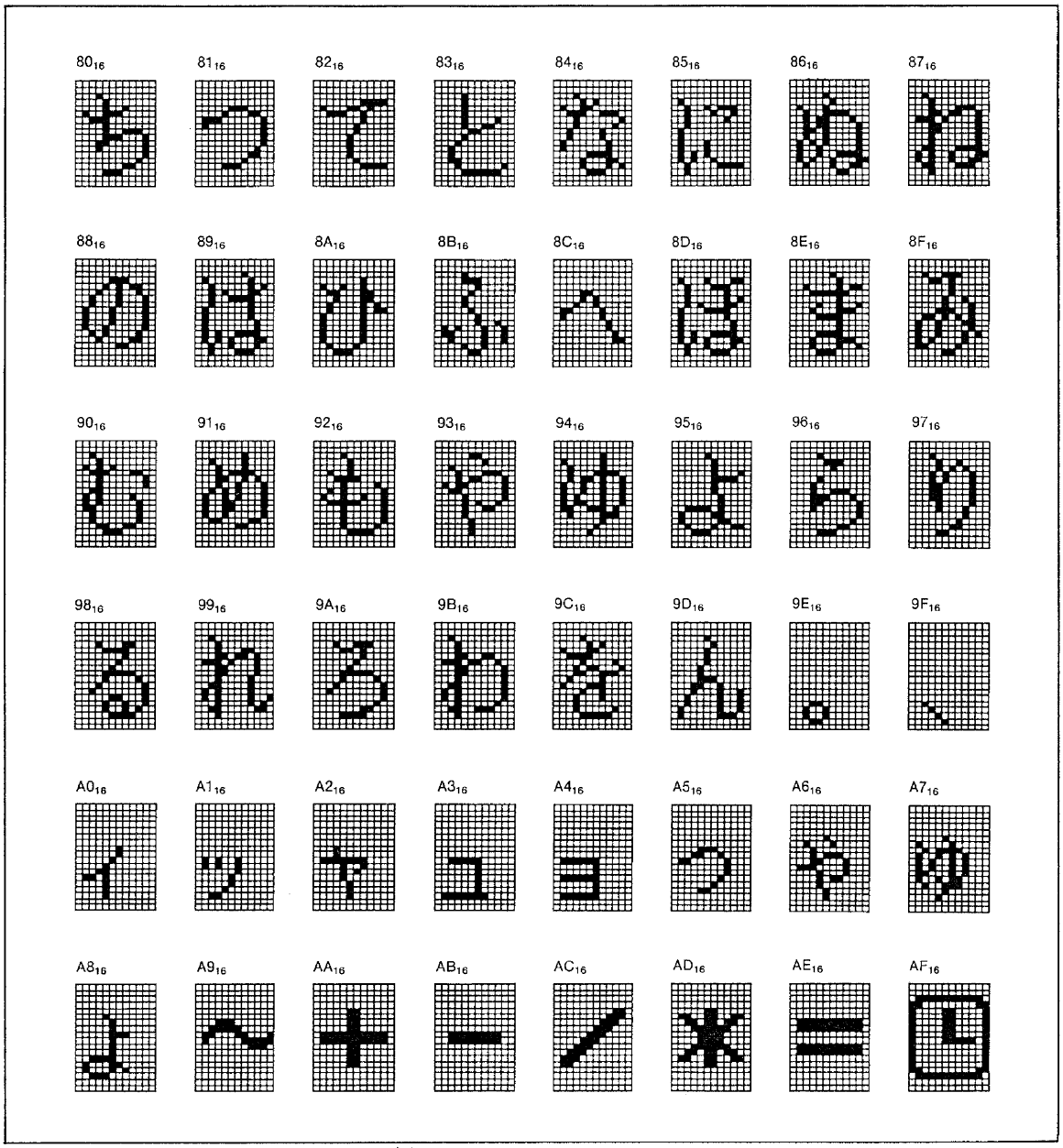


Fig. 23 M35012-001SP character patterns (4)

Fig. 24 M35012-001SP character patterns (5)

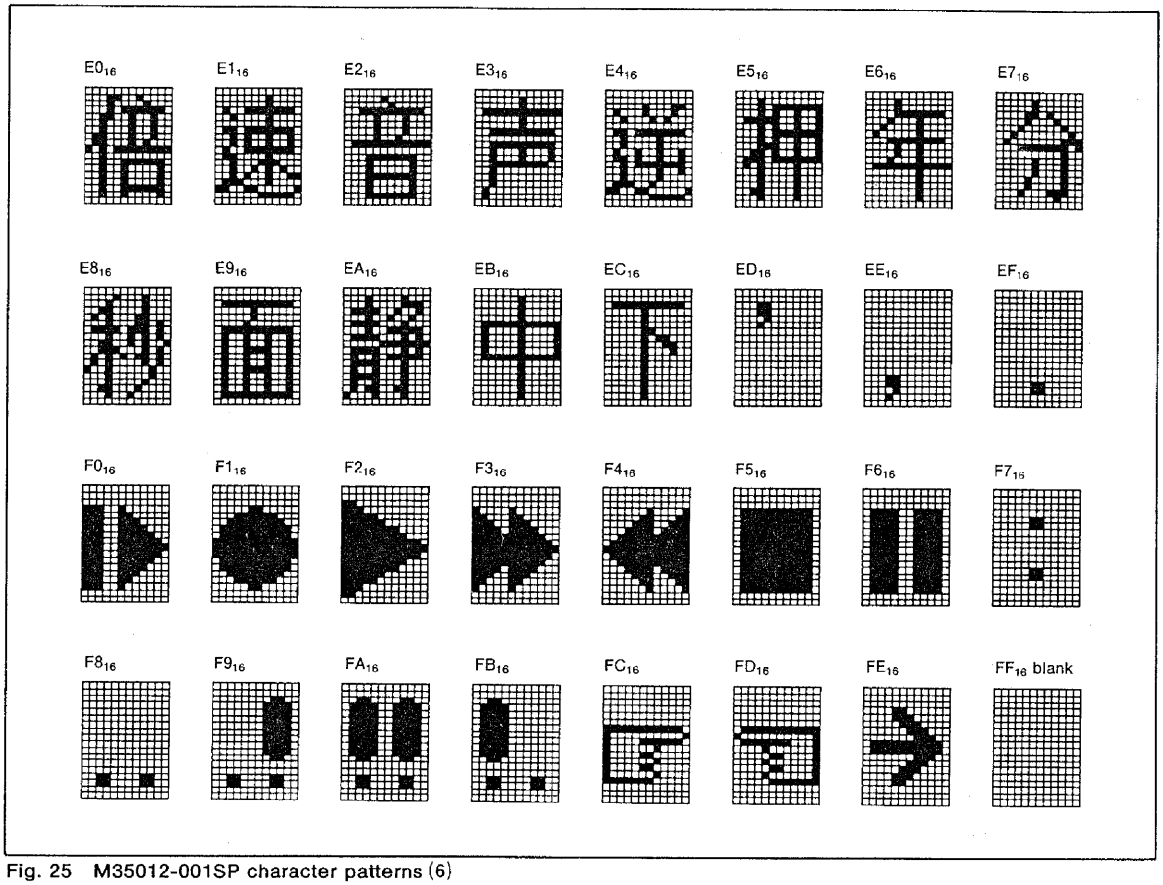


Fig. 25 M35012-001SP character patterns (6)