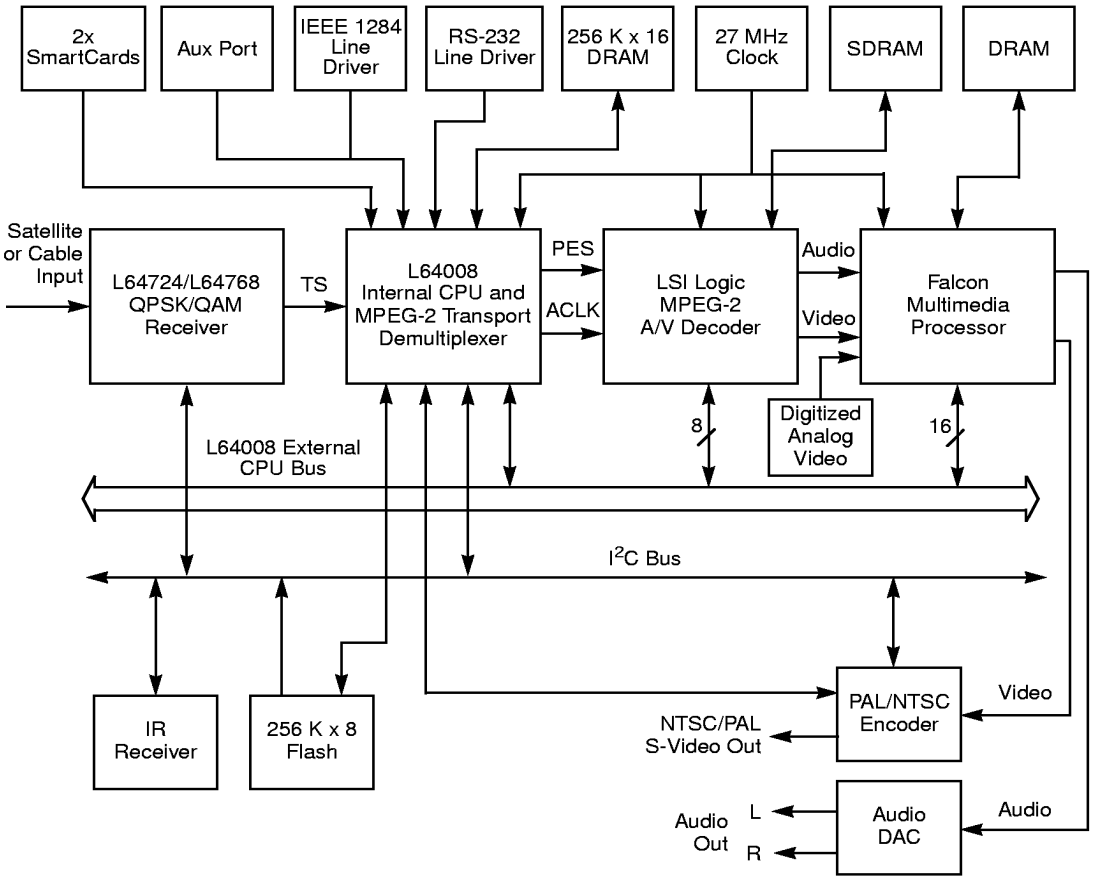
Falcon™ Multimedia Processor

Preliminary Datasheet

LSI Logic's Falcon is an advanced multimedia processor for high-performance set-top box (STB) applications. Figure 1 illustrates how Falcon integrates into an LSI Logic Integra™ MPEG-2 system.

Figure 1 Falcon System Block Diagram



Falcon overlays captured video and animated bitmapped graphics with live motion video using advanced chroma keying and alpha blending functions. Its other video functions include color space conversion, anti-flutter filtering, dithering, video capture, and scaling. Falcon supports both NTSC (525 lines/60 Hz) and PAL (625 lines/50 Hz) compatible displays with square pixel and ITU-R 601 pixel sampling.

Falcon supports three independent physical video planes, which include an on-screen display (OSD) plane, a 4:2:0 graphics plane, and a passthrough video plane. The OSD and 4:2:0 planes are stored in external DRAM. The passthrough video plane is live video from an MPEG-2 decoder or an auxiliary digital video source. Falcon mixes these planes to produce a single output display plane by using chroma keying and alpha blending.

Falcon contains a bit block transfer function (blitter) that fast copies rectangular pixel blocks. The blitter implements multiple logical planes within the OSD and 4:2:0 physical planes. For example, Falcon can efficiently generate logical planes that simulate a background color plane, a still picture plane, and decimated video in the 4:2:0 plane. The flexibility of these blitter functions enables Falcon to meet the requirements of a variety of applications.

Falcon includes an auxiliary video input port which can receive 8-bit or 16-bit digitized analog YCbCr video data from a digital decoder such as the SAA7110.

Falcon mixes PCM audio data (stored in DRAM), such as beeps and other sounds, with real time audio streams.

Falcon interfaces with LSI Logic's L64008 CPU/MPEG-2 Transport Demultiplexer via the external CPU bus (EBus). Falcon also interfaces with Intel and Motorola PowerPC style CPUs.

Falcon interfaces with standard and EDO DRAMs (512 kbyte, 1 Mbyte, or 2 Mbyte). Falcon addresses up to 16 Mbits of memory anywhere within a 64 Mbit DRAM address range.

Falcon is a low-power, 3.3-V device in a 208-pin plastic quad flat package (PQFP). It is manufactured using a 0.35 micron CMOS process.

Features

Video Overlay

- Overlay of captured video and bitmapped animated graphics with live motion video using chroma keying and alpha blending functions
- Seamless interface with LSI Logic's L64005/L64105 MPEG-2 decoders for digital video input
- YCbCr 4:2:2 video input with square pixel or ITU-R601 pixel sampling
- Auxilary 8-bit or 16-bit YCbCr video interface for digitized analog signals
- Three optimized physical display planes (an OSD plane, a 4:2:0 graphics plane, and a passthrough video plane), which support multiple logical planes
- RGB16, CLUT8, and ACLUT16 color formats
- Anti-flutter filter
- Video capture control with scaling (sample rate decimation) and dithering
- Programmable CRT controller (CRTC)
- High and medium display resolutions: 640 x 480, 768 x 576, 720 x 480, 720 x 576, 320 x 240, 384 x 288, 352 x 240 (or 360), 352 x 288 (or 360)
- Video output compatible with commodity NTSC and PAL digital encoders
- Display clocks: 27 MHz ITU-R601 pixel clock, 24.54 MHz (NTSC) and 29.5 MHz (PAL) square pixel clocks, digital video input clock, and digitized analog video input clock

Audio Mixing

- Seamless interface with LSI Logic's L64005/L64105 MPEG-2 decoders
- PCM (pulse code modulation) audio playback of sound samples and synthesized audio (8-bit or 16-bit stereo and mono)
- Mixing of PCM audio, stored in DRAM, with live digital audio

- 16-bit stereo PCM output with direct connection to a commodity digital-to-analog converter (DAC)

Graphics Acceleration

- High-speed blitter processes at speeds up to one pixel per memory clock cycle (54 MHz maximum)
- Linked-list blitter operations
- Blitter may be paced to match display rates
- Blitter can be triggered by video events, for example, line numbers

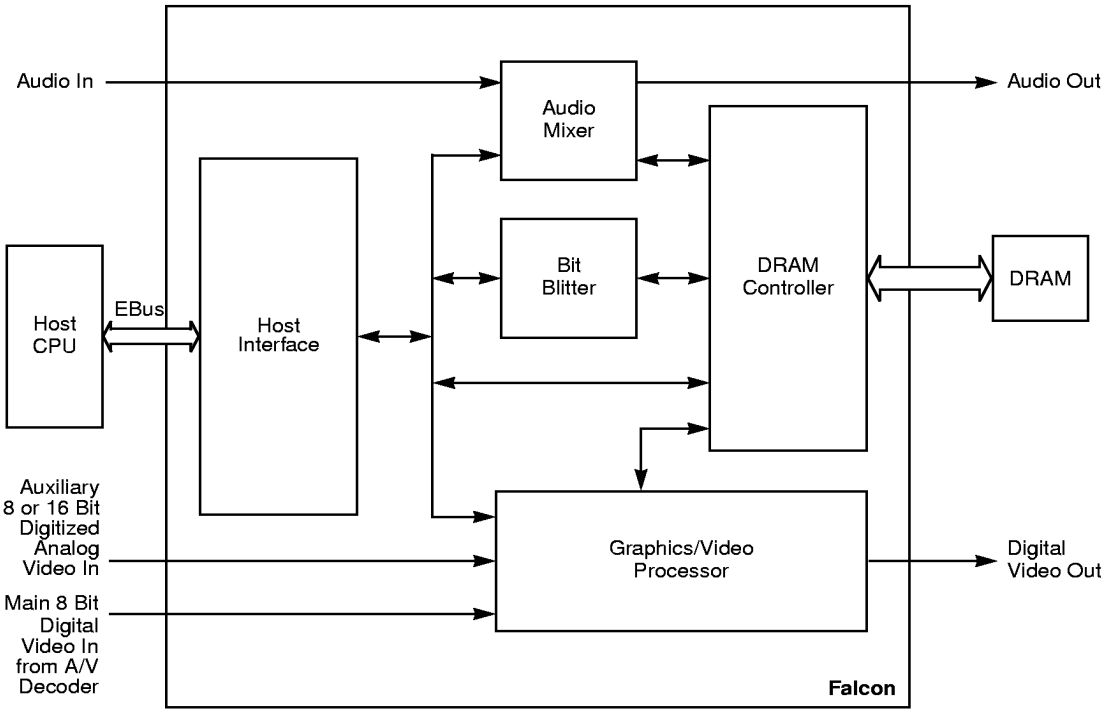
General Features

- EBus interface to LSI Logic's L64008 CPU/MPEG-2 Transport Demultiplexer
- Interfaces with Intel and Motorola style PowerPCs
- Compatible with standard or EDO DRAMs (512 kbyte, 1 Mbyte, or 2 Mbyte)
- Programmable DRAM controller supports 16-bit and 32-bit data widths
- Uses 16 Mbits of memory address space for normal operation
- 54 MHz system clock from the L64008
- 208-pin PQFP
- 0.35 micron, 3.3-V CMOS process

Functional Description

This section describes the main functional components of the Falcon Multimedia Processor. Figure 2 shows the Falcon block diagram.

Figure 2 Falcon Block Diagram



The following subsections describe these functional components:

- EBus Interface
- DRAM Controller
- Video/Graphics Processor
- Blitter
- Audio Mixer

EBus Interface

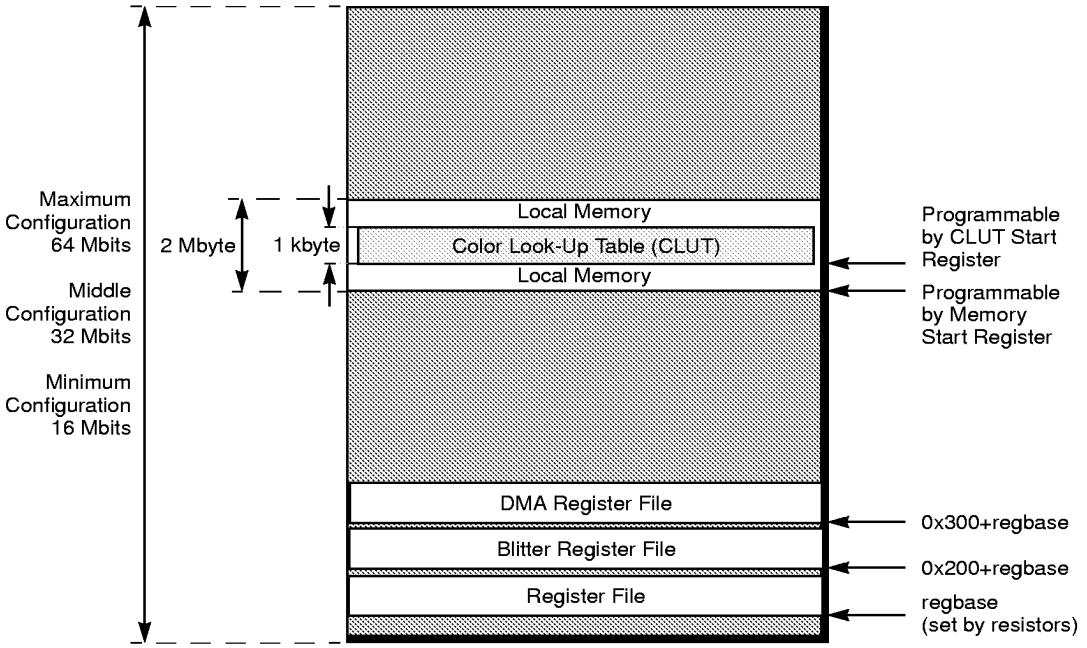
Falcon connects directly with LSI Logic's L64008 CPU/MPEG-2 Transport Demultiplexer via the EBus interface. The Falcon also interfaces with Intel and Motorola PowerPC style CPUs. In order to increase host access speeds, Falcon's EBus interface uses a 4-word write FIFO and a 1-word read cache with a single address tag for latency reduction. Other programmable features of the EBus interface include interrupt polarity selection and the insertion of optional wait states in the bus cycle.

DRAM Controller

Falcon's high performance DRAM controller directly controls standard or EDO DRAMs of various capacities: 512 kbyte, 1 Mbyte, and 2 Mbyte. The DRAM controller supports both 16-bit (512 kbyte DRAM) and 32-bit (1 or 2 Mbyte DRAMs) data widths. In order to maximize performance, the DRAM controller utilizes an independent memory clock (MCLK), which supports frequencies of up to 54 MHz.

Falcon optimizes memory space according to the memory map shown in Figure 3. Falcon utilizes up to 16 Mbits of address space anywhere within the maximum 64 Mbits of address space in DRAM. Falcon divides memory space into the following regions: local memory and register files. The register files include subregions allocated to the DMA register files and the blitter register files.

Figure 3 Memory Map



Video/Graphics Processor

Falcon's video/graphics processor performs all video interfacing, video/graphics overlay, and video capture.

Video Interface

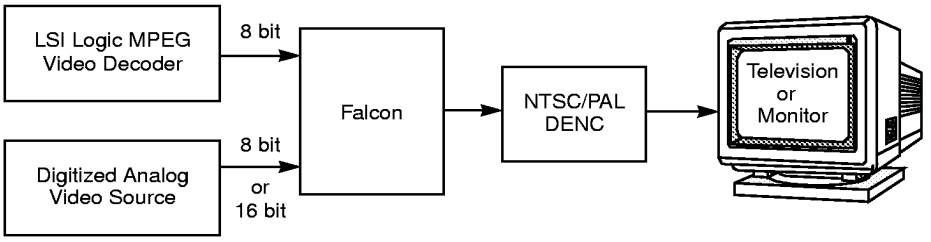
Falcon receives YCbCr 4:2:2 video input from both main and auxiliary sources. LSI Logic's MPEG-2 decoders, such as the L64005 and the L64105, serve Falcon as main sources for digital video input. Digitized analog video input may be supplied through the auxiliary input.

The video/graphics processor features a CRTC that generates the horizontal and vertical sync CRT display signals. The CRTC also scans interlaced and non-interlaced display fields.

To help eliminate "flutter" in medium resolution displays such as televisions, Falcon filters interlaced display fields by means of display line interpolation.

Figure 4 shows the basic video interface configuration for Falcon. Falcon supports a variety of both high and medium resolution displays.

Figure 4 Falcon Video Interfaces



Video/Graphics Overlay

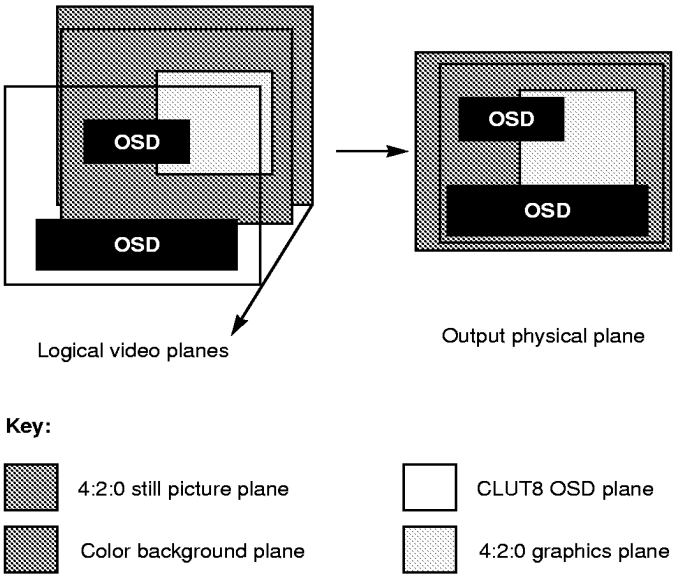
Falcon can overlay captured video and bitmapped graphics with passthrough motion video. Falcon accomplishes this by chroma keying and alpha blending video images on three physical display planes, which support a combination of multiple logical display planes. These are the three physical planes:

- OSD plane
- 4:2:0 graphics plane
- Passthrough video plane

Figure 5 shows an example with four logical planes and their resulting physical display. The visibility of each plane is determined by the translucency and transparency parameters of the plane itself and of the plane(s) residing in front of it. The video/graphics processor controls these parameters by means of chroma keying and alpha blending,

In this example, the front plane is the 8-bit CLUT OSD plane. This is the plane through which live passthrough video is displayed. Falcon uses the 4:2:0 graphics plane to display captured motion video and animated bitmapped graphics stored in DRAM. The 4:2:0 still picture plane displays bitmapped graphic images and still video frames also stored in DRAM. The color background plane displays an opaque, user-defined color background.

Figure 5 Logical Display Planes



Falcon converts incoming YCbCr signals to one of four color spaces: RGB16, CLUT8, 4:2:0, or ACLUT16. Before video data is output from Falcon, the video/graphics processor converts the color space of the video signal back into YCbCr format.

Video Capture

Falcon captures both digital and digitized analog video signals in a continuous or single shot. Prior to video capture, Falcon can optionally filter incoming video data with horizontal low pass filtering (dithering). Once captured, the video data is decimated. The horizontal and vertical scaling parameters are host programmable. Falcon captures the decimated video data in DRAM.

Blitter

Falcon's blitter accelerates video/graphics processing by performing high-speed linked list operations on two-dimensional pixel arrays. The blitter can execute the following operations:

- Copy a display image from one location to another
- Blend two source images and copy the resulting image to another location (only in designated modes)
- Flood fill a display area with a specified color

The blitter functions at maximum speeds of up to one pixel per memory clock cycle (MCLK = 54 MHz maximum) for read/write operations. Optionally, its speed may be paced to match that of the current display rate.

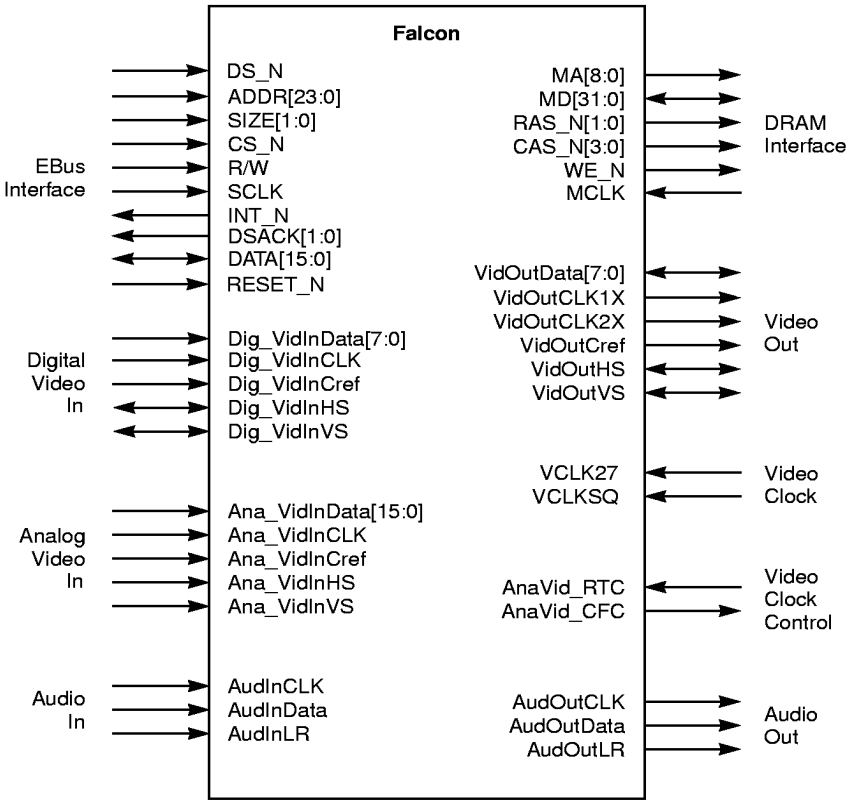
Audio Mixer

The audio mixer accepts external digital audio signals. Its interface is compatible with LSI Logic's L64005/L64105 line of MPEG-2 decoders. The audio mixer either passes live audio through Falcon unmixed or mixes it with PCM audio data stored in DRAM. The stored PCM audio data (8-bit or 16-bit stereo and mono) is typically in the form of sound samples (beeps, etc.) and synthesized audio. Falcon outputs 16-bit stereo PCM audio to standard DACs.

Signal Description

This section describes the interface signals shown in Figure 6. This section concludes with a pinout diagram in Figure 7.

Figure 6 Falcon Signal Interface



The following tables provide signal descriptions which correspond to the interfaces illustrated in Figure 6.

Table 1 EBus Interface Signals

Pin Name	Pin Type	Pin No.	Description
DS_N	I	2	Data Strobe
ADDR[23:19]	I	4–8	Host Address
ADDR[18:12]	I	10–16	Host Address
ADDR[11:5]	I	18–24	Host Address
ADDR[4:2]	I	26–28	Host Address
SIZE[1:0]	I	29–30	Transfer Size
ADDR[1:0]	I	31–32	Host Address
CS_N	I	34	Chip Select
R/W	I	35	Read/Write
SCLK	I	39	CPU Clock (27 MHz)
INT_N	O	42	Interrupt (open drain)
DSACK[0:1]	3-state	43–44	Data/Size Acknowledge
Reserved	Pull-down to VSS via a 10 k resistor	46–52	Reserved
Reserved		54–60	Reserved
Reserved		62–63	Reserved
DATA[15:11]	I/O	64–68	Host Data
DATA[10:4]	I/O	70–76	Host Data
DATA[3:0]	I/O	78–81	Host Data
RESET_N	I	208	Reset

Table 2 Digital Video Input Signals

Pin Name	Pin Type	Pin No.	Description
Dig_VidInData[0:7]	I	83–90	4:2:0 Data In
Dig_VidInCLK	I	92	2x Pixel Clock
Dig_VidInHS	I/O	94	Digital Video Horizontal Sync
Dig_VidInVS	I/O	95	Digital Video Vertical Sync
Dig_VidInCref	I	96	Digital Video Chroma Phase (Cr_Ref)

Table 3 Digitized Analog Video Input Signals

Pin Name	Pin Type	Pin No.	Description
Ana_VidInHS	I	97	Analog Video Horizontal Sync
Ana_VidInVS	I	98	Analog Video Vertical Sync
Ana_VidInCref	I	99	Analog Video Chroma Phase (Cr_Ref)
Ana_VidInCLK	I	101	Analog Video 2x Pixel Clock
Ana_VidInData[0:7]	I	103–110	Analog Video Data In
Ana_VidInData[8:15]	I	112–119	Analog Video Data In

Table 4 Video Clock Signals

Pin Name	Pin Type	Pin No.	Description
VCLK27	I	121	27 MHz Clock
VCLKSQ	I	123	2x Pixel Clock for Square Pixel Mode

Table 5 Video Output Signals

Pin Name	Pin Type	Pin No.	Description
VidOutData[0:4]	I/O	125–129	4:2:0 Data Out (Pull-up/Pull-down)
VidOutData[5:7]	I/O	130–132	4:2:0 Data Out (Pull-down)
VidOutCLK1x	O	134	1x Pixel Clock
VidOutCLK2x	O	135	2x Pixel Clock
VidOutHS	I/O	137	Horizontal Sync
VidOutVS	I/O	138	Vertical Sync or Odd/Even Indicator
VidOutCref	I/O	139	Chroma Phase (Pull-up)

Table 6 Video Clock Control Signals

Pin Name	Pin Type	Pin No.	Description
AnaVid_CFC	O	140	Chroma Frequency Control
AnaVid_RTC	I	141	Real Time Clock Input

Table 7 Audio Input Signals

Pin Name	Pin Type	Pin No.	Description
AudInCLK	I	143	Audio Clock
AudInData	I	144	Audio Data In
AudInLR	I	145	Audio LR Clock

Table 8 Audio Output Signals

Pin Name	Pin Type	Pin No.	Description
AudOutCLK	O	146	Audio Clock Out
AudOutData	O	147	Audio Data Out
AudOutLR	O	148	Audio LR Clock

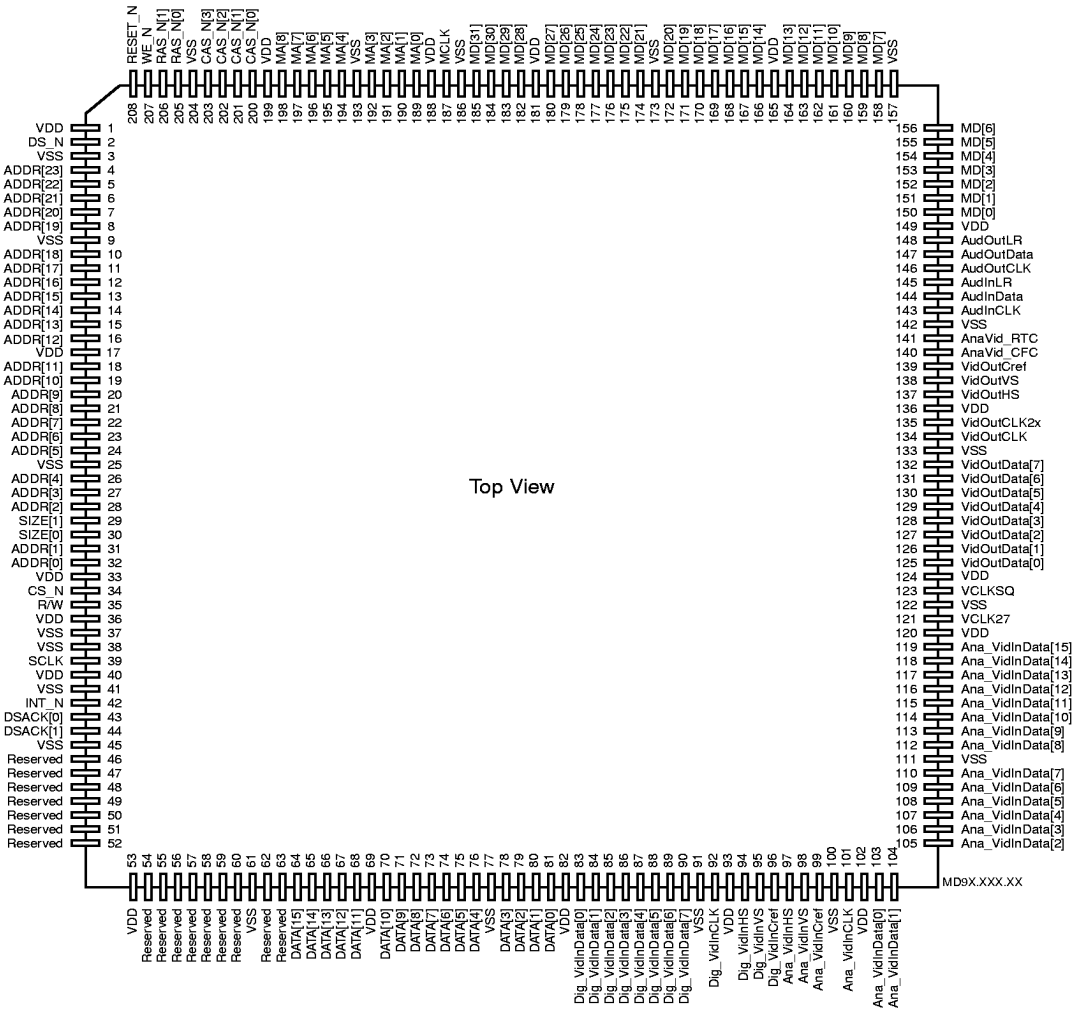
Table 9 DRAM Interface Signals

Pin Name	Pin Type	Pin No.	Description
MD[0:6]	I/O	150–156	DRAM Data
MD[7:13]	I/O	158–164	DRAM Data
MD[14:20]	I/O	166–172	DRAM Data
MD[21:27]	I/O	174–180	DRAM Data
MD[28:31]	I/O	182–185	DRAM Data
MCLK	I	187	Memory Clock
MA[0:3]	O	189–192	DRAM Address
MA[4:8]	O	194–198	DRAM Address
CAS_N[0:3]	O	200–203	Column Address Strobe
RAS_N[0:1]	O	205–206	Row Address Strobe
WE_N	O	207	Write Enable

Table 10 Power/Ground Pins

Pin Name	Pin Type	Pin Numbers
VDD	Power	1, 17, 33, 36, 40, 53, 69, 82, 93, 102, 120, 124, 136, 149, 181, 188, 199
VSS	Ground	3, 9, 25, 37, 38, 41, 45, 61, 77, 91, 100, 111, 122, 133, 142, 157, 173, 186, 193, 204

Figure 7 Falcon Pinout



Register Map

Table 11 provides Falcon's register map.

Table 11 Register Map

Register Type	Address	Bit Field Description
Video output	0x00	Horizontal Total
	0x04	Horizontal Sync Width
	0x08	Horizontal Display Start
	0x0C	Horizontal Display End
	0x10	Vertical Total
	0x14	Vertical Sync Width
	0x18	Vertical Display Start
	0x1C	Vertical Display End
	0x20	
	0x24	
	0x28	Raster Compare
	0x2C	Field Counter (19) / CRTC Line Counter (10–0)
	0x30	CRTC Vertical Counter Preset (25–16) / CRTC Horizontal Counter Preset (10–0)
	0x34	CRT Control
	0x38	
	0x3C	
	0x40	Graphics Layer Gain Ctrl.
	0x44	Graphics Layer Chroma Key (max) (31–16) / Graphics Layer Chroma Key (min) (15–0)
	0x48	Display Controls
	0x4C	*

* DMA Bank Control.

Table 11 Register Map (Cont.)

Register Type	Address	Bit Field Description
		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Video Input	0x50	Digital Video Input Control
	0x54	Analog Video Input Control
	0x58	
	0x5C	
	0x60	Video Capture Vertical Start Location / Video Capture Horizontal Start Location
	0x64	Video In Vertical Capture Size / Video In Horizontal Capture Size
	0x68	Vertical Scaling Control / Horizontal Scaling Control
	0x6C	Video In Capture Control
Graphics Accel-erator	0x70	
	0x74	
	0x78	
	0x7C	
	0x80	Blitter Control
	0x84	Blitter Status (read only)
Unused	0x88	
	0x8C	
System Control	0x90	Falcon Revision Number (read only) / Falcon ID Number (read only)
	0x94	Falcon System Control
	0x98	Falcon Memory Control
	0x9C	
	0xA0	Memory Map
	0xA4	
	0xA8	
	0xAC	Test Mode
	0xB0	Timer Counter
	0xB4	Timer Compare
	0xB8	Watchdog Timer
	0xBC	
	0xC0	Interrupt Enable
	0xC4	Interrupt Status (read only)
	0xC8	Interrupt Clear
	0xCC	
	0xD0	CLUT Memory Location
Unused	0xD4	
	0xD8	
	0xDC	

Table 11 Register Map (Cont.)

Register Type	Address	Bit Field Description
		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Audio	0xE0	Audio Sample Start Address
	0xE4	Audio Sample End Address
	0xE8	Audio Sample Write Pointer
	0xEC	Audio Sample Read Pointer
	0xF0	Audio Reference Pointer
	0xF4	Audio Control
	0xF8	Audio Time Stamp
Unused	0xFC	
Blitter	0x200	Blitter Register File Base Address
	0x200	Blitter Alpha Blend Value / Blitter Mode
	0x204	Blitter Source 1 Pixel Map Pointer
	0x208	Blitter Source 2 Pixel Map Pointer
	0x20C	Blitter Destination Pixel Map Pointer
	0x210	Blitter Source 2 Pixel Map Pitch / Blitter Source 1 Pixel Map Pitch
	0x214	Blitter Destination Pixel Map Pitch
	0x218	Blitter Height / Blitter Width
	0x21C	Minimum Blitter Chroma Value / Maximum Blitter Chroma Value
	0x220	Blitter Link List Pointer
Unused	0x224	
	0x228	
	0x22C	
DMA	0x300	DMA Register File Base Address
	0x300	Display Height / Display Pixel Map Pitch
	0x304	Display Pixel Map Start Address
	0x308	Display Alpha Channel Start Address
	0x30C	Display Link List Pointer
	0x310	Video Capture Pixel Map Pitch
	0x314	Video Capture Channel Odd Field Start Address
	0x318	Video Capture Channel Even Field Start Address
	0x31C	Capture Link List Pointer

Specifications

This section contains the electrical specifications for Falcon.

Table 12 Absolute Maximum Ratings

Symbol	Parameter	Limits[1]	Units
V_{DD}	DC Supply	−0.3 to +3.9	V
V_{IN}	5-V Compatible Input Voltage	−1.0 to +6.5	V
I_{IN}	DC Input Current	±10	mA
T_{STGP}	Storage Temperature Range (PQFP Package)	−40 to +125	°C

1. Referenced to V_{SS}.

Table 13 Recommended Operating Conditions

Symbol	Parameter	Limits	Units
V_{DD}	DC Supply	+3.14 to +3.46	V
T_A	Ambient Temperature	0 to +70	°C

Table 14 Pin Capacitance

Symbol	Parameter[1]	Min	Units
C_{IN}	Input Capacitance	2.5	pF
C_{OUT}	Output Capacitance	2.0	pF

1. Measurement conditions are V_{IN} = 3.3 V (V_{IN} = 5.0 V for 5-V tolerant buffers), T_A = 25 °C, and clock frequency = 1 MHz.

Table 15 DC Characteristics

Symbol	Parameter	Condition[1]	Min	Typ	Max	Units
V_{IL}	Voltage Input Low TTL CMOS		 — —	 — —	 0.8 $0.2V_{DD}$	 V V
V_{IH}	Voltage Input High TTL CMOS 5-V Compatible		 2.0 $0.7V_{DD}$ 2.0	 — —	 — 5.5	 V V V
V_{OL}	Voltage Output Low 4-mA Output Buffers 8-mA Output Buffers	 I_{OL} = 4.0 mA I_{OL} = 8.0 mA	 — —	 0.2 0.2	 0.4 0.4	 V V
V_{OH}	Voltage Output High 4-mA Output Buffers 8-mA Output Buffers	 I_{OH} = –4.0 mA I_{OH} = –8.0 mA	 2.4 2.4	 — —	 — —	 V V
I_{IL}	Current Input Leakage[2] with Pulldown with Pullup	$V_{IN} = V_{DD}$ or V_{SS} $V_{IN} = V_{DD}$ $V_{IN} = V_{SS}$	–10 35 –214	±10 115 –115	 222 –35	µA µA µA
I_{OZ}	Current 3-State Output Leakage	V_{DD} = Max $V_{OUT} = V_{SS}$ or V_{DD}	–10	±1	+10	µA
I_{DD}	Quiescent Supply Current	$V_{IN} = V_{DD}$ or V_{SS}	—	TBD	—	mA
I_{CC}	Dynamic Supply Current	V_{DD} = Max f = 27 MHz	—	TBD	—	mA

1. Specified at V_{DD} equals 3.3 V ±5% at ambient temperature over the specified range.
2. For CMOS and TLL inputs.

AC Timing

This section describes Falcon's AC timing characteristics. The Falcon EBus timing is described first, followed by descriptions of DRAM interface timing and video input/output timing.

EBus Timing

Figure 8 shows the Falcon EBus read/write cycle timing, which is compatible with the L64008 EBus timing. Table 16 provides the associated AC timing specifications.

Figure 8 EBus Read/Write Cycle

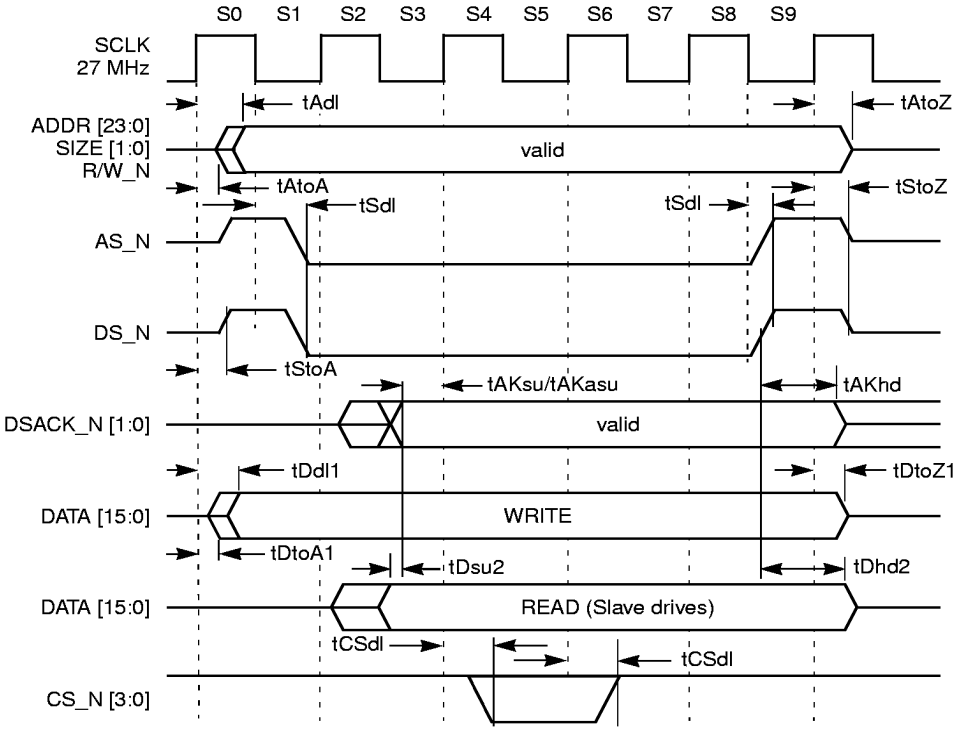


Table 16 L64008 EBus Timing

Symbol	Parameter	Time (ns)	
		Min	Max
tDsu2	DATA[15:0] setup time to DSACK[1:0] falling when external slave returns data	0	
tAKsu/tAKasu	DSACK[1:0] Sync[1]/Async[2] setup time during L64008 master cycle	0	
tADsu	ADDR[23:0], SIZE[1:0] setup time	0	
tRWsu	R/W setup time	5	
tDSsu	DS setup time	10	
tAKhd	DS rising to DSACK[1:0] hold time	0	37
tASsu	AS setup time	7	
tDhd2	DATA[15:0] hold time when external slave returns data to L64008	0	
tADhd	ADDR[23:0], SIZE [1:0] hold time	5	
tRWhd	R/W hold time	5	
tDShd	DS hold time[3]	5	
tAShd	AS hold time	5	
tDhd3[4]	DATA [15:0] hold time when external slave returns data to L64008 in self acknowledgement mode	0	
tDsu3[4]	DATA[15:0] setup time to CS[3:0] rising when external slave returns data to L64008	50	
tAtoA	ADDR[23:0], R/W, SIZE [1:0] Hi-z to active	3	16
tAdl	ADDR[23:0], R/W, SIZE[1:0] delay		0
tAtoZ	ADDR[23:0], R/W, SIZE [1:0] active to Hi-z		16
tDtoA1	DATA[15:0] Hi-z to active when L64008 writes	3	16

Table 16 L64008 EBus Timing (Cont.)

Symbol	Parameter	Time (ns)	
		Min	Max
tDdl1	DATA[15:0] delay when L64008 writes		0
tDtoZ1	DATA[15:0] active to Hi-z when L64008 writes		16
tDtoA2	DATA[15:0] Hi-z to active when L64008 is in slave read cycle	3	16
tDdl2	DATA[15:0] delay when L64008 is in slave read cycle		16
tDtoZ2	DATA[15:0] active to Hi-z when L64008 is slave read cycle	3	16
tStoA	AS, DS Hi-z to active	3	16
tSdl	AS, DS fall/rise delay		13
tStoZ	AS, DS active to Hi-z		16
tAKtoA	DSACK[1:0] Hi-z to active when L64008 is slave read cycle		16
tAKdl	DSACK[1:0] delay when L64008 is slave read cycle		13
tAKtoZ	DSACK[1:0] active to Hi-z when L64008 is slave read cycle	3	6
tCSdl	CS[3:0] fall/rise delay	3	13

1. The pseudo 32-bit device always has to satisfy this synchronous setup time (tAKsu at any time slot).
2. tAKasu indicates the asynchronous setup time (tAKasu at S3- time slot) that qualifies for the fastest transaction of 5 SCLK cycles (latency of 2.5 SCLK cycles to DS negation after DSACK has been sampled).
3. DS negation is required by next rising edge of SCLK when the external master samples assertion of DSACK[1:0] during his write data transaction cycle for L64008 internal resources.
4. This parameter only applies to read cycles in L64008 master self acknowledgement mode.

DRAM Interface Timing

The DRAM interface timing parameters are programmable. Table 17 gives the DRAM timing parameter specifications. Figures 9 and 10 show page-mode write cycle timing (for EDO and non-EDO DRAMs) when the CAS_N pulse width is set for two MCLK cycles and one MCLK cycle, respectively. Figures 11 and 12 show page-mode read cycle timing for non-EDO and EDO DRAMs, respectively.

Table 17 DRAM Interface Timing

Symbol	Parameter	Time (ns)	
		Min	Max
T	MCLK period	20	
tRC	Cycle time	5T	32T
tRP	RAS_N Precharge time	1.5T	5T
tRCD	RAS_N to CAS_N delay	1.5T	2.5T
tRASP	RAS_N Pulse Width	3T	27T
tCP	CAS_N Precharge time	0.5T	T
tCASP	CAS_N Pulse Width	T	2.5T–3.5T
tASR	Row Address Setup time	0.5T	T
tRAH	Row Address Hold time	T	T
tASC	Column Address Setup time	0.5T	T
tCAH	Column Address Hold time	T	2.5T–3.5T
tDS	Data In Setup time	0.5T	T
tDH	Data In Hold time	T	2.5T–3.5T

Figure 9 Page-Mode Write Cycle Timing when CAS_N Pulse Width Is Two MCLK Cycles

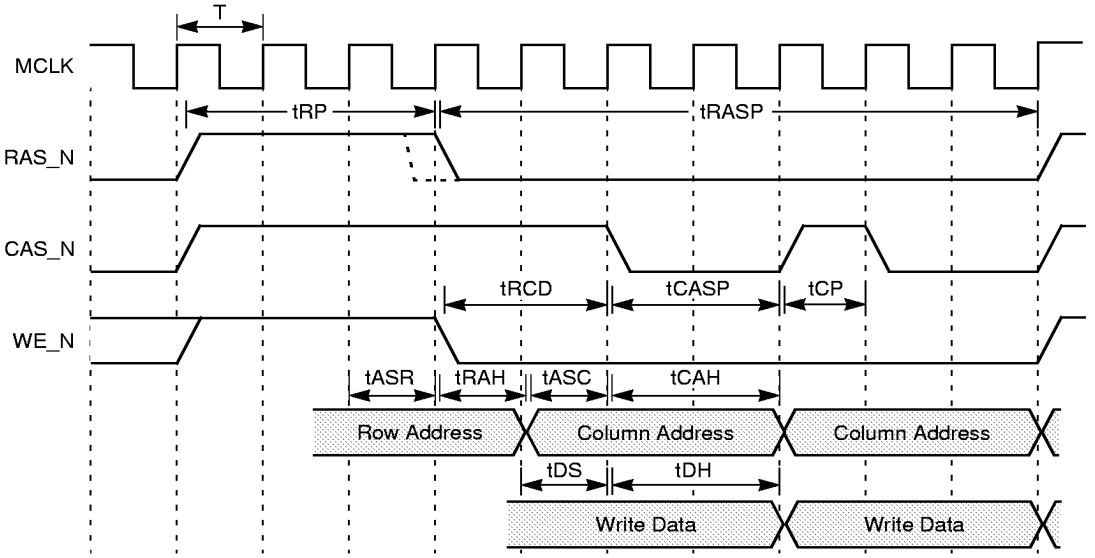


Figure 10 Page-Mode Write Cycle Timing when CAS_N Pulse Width Is One MCLK Cycle

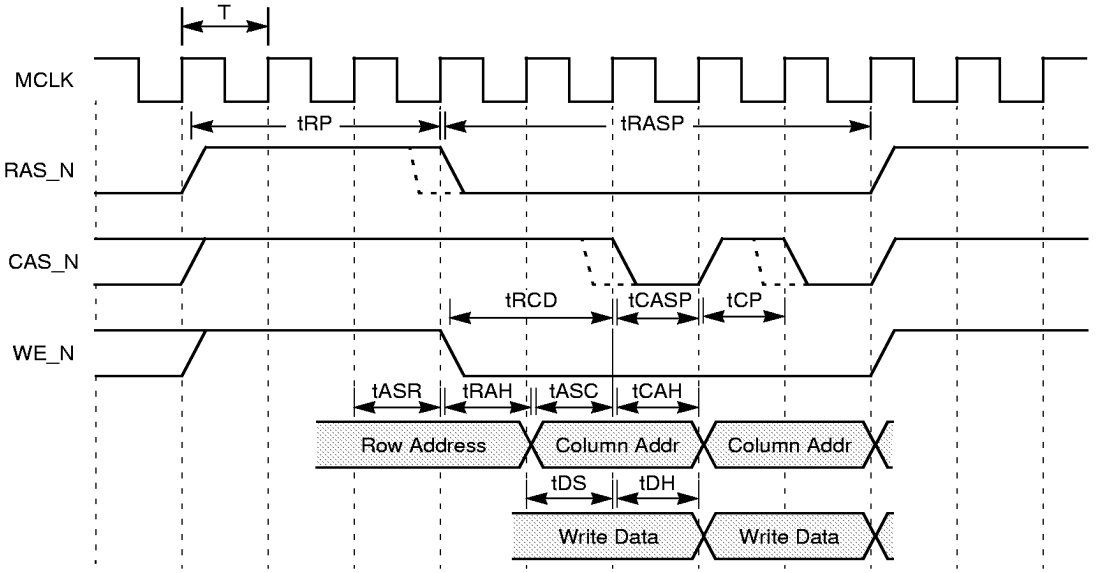


Figure 11 Page-Mode Read Cycle Timing (non-EDO)

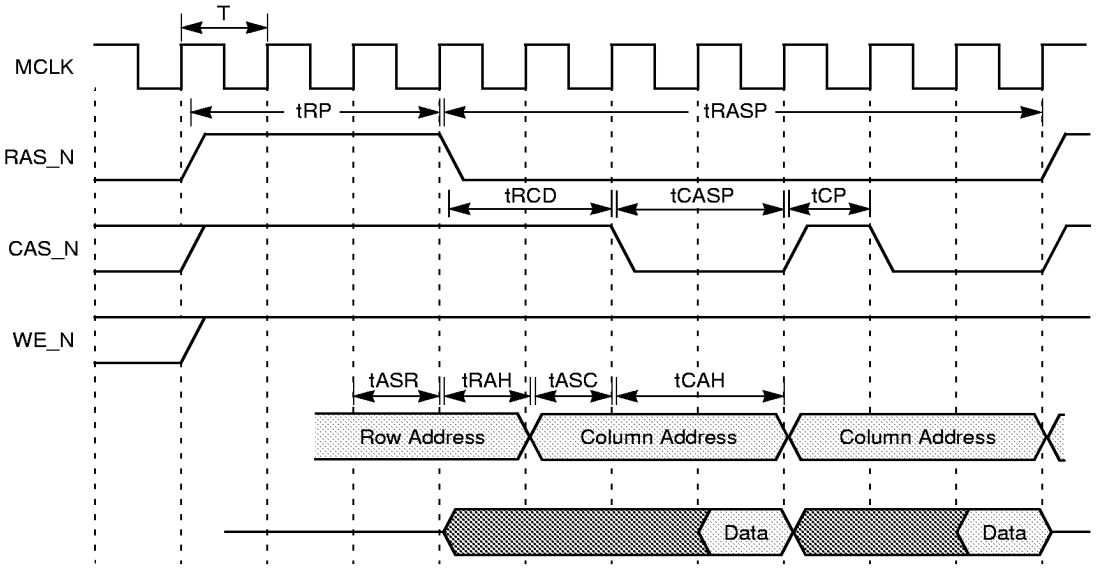
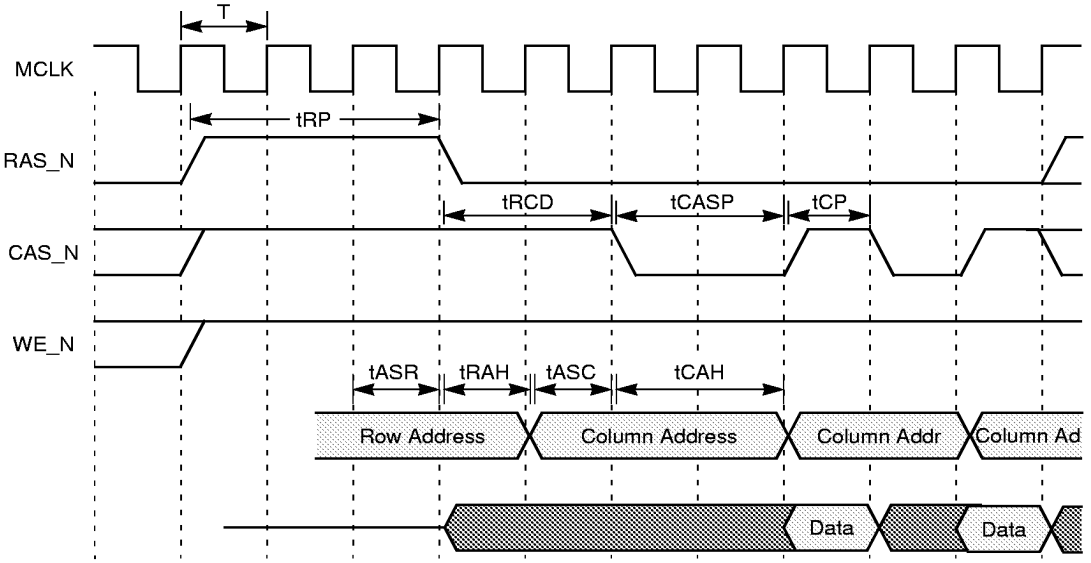


Figure 12 Page-Mode Read Cycle Timing (EDO)



Video Input/Output Timing

This section includes Falcon's video input/output interface timing specifications. In Figures 13–15, tPIX represents a 13-MHz pixel clock cycle.

Figure 13 16-bit Digitized Analog Video Input Pixel Timing

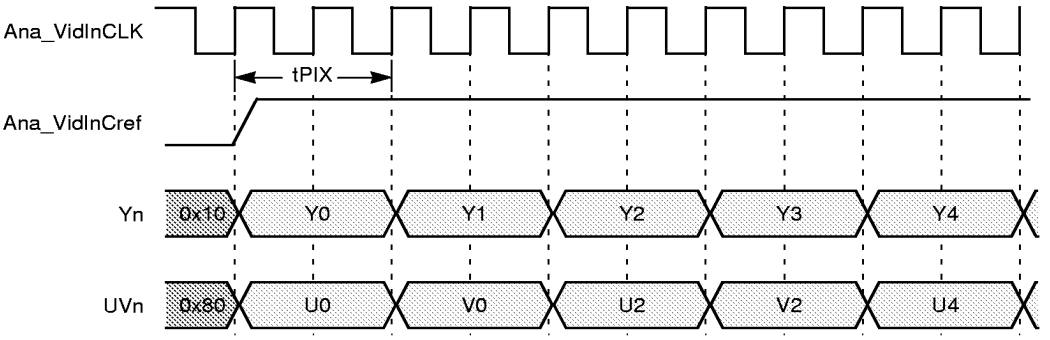


Figure 14 shows the digital video input pixel timing. The 8-bit digitized analog video input pixel timing is identical to the timing shown in Figure 14.

Figure 14 8-bit Digital MPEG-2 Video Input Pixel Timing

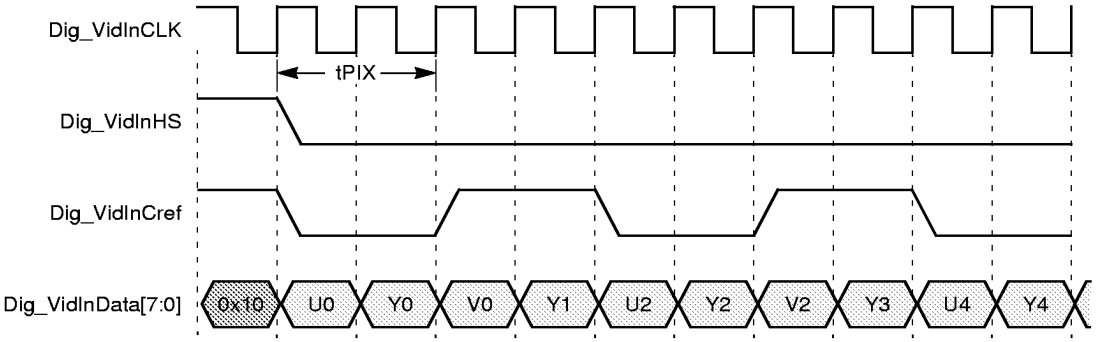
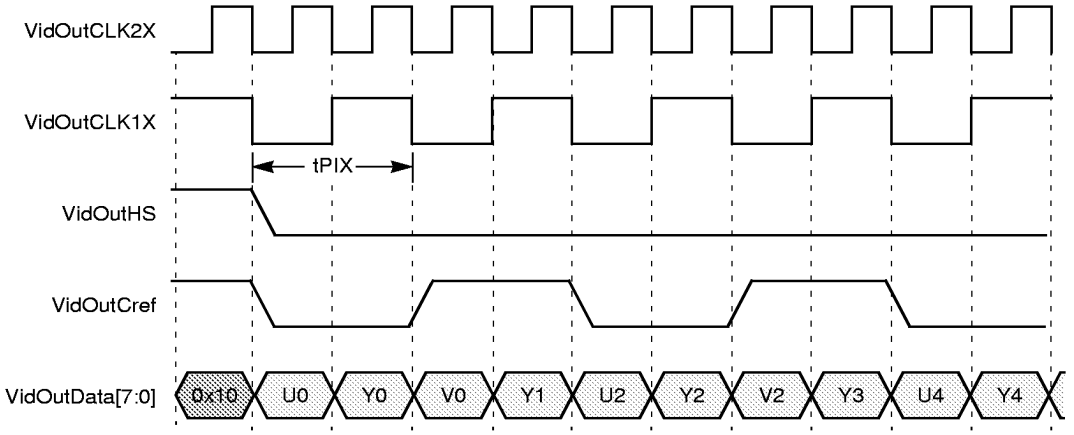


Figure 15 Falcon Video Output Pixel Timing



Package Dimensions

This section contains the mechanical drawings for Falcon's 208-pin plastic quad flat package (PQFP).

Figure 16 208-pin Plastic Quad Flat Package (Sheet 1 of 2)

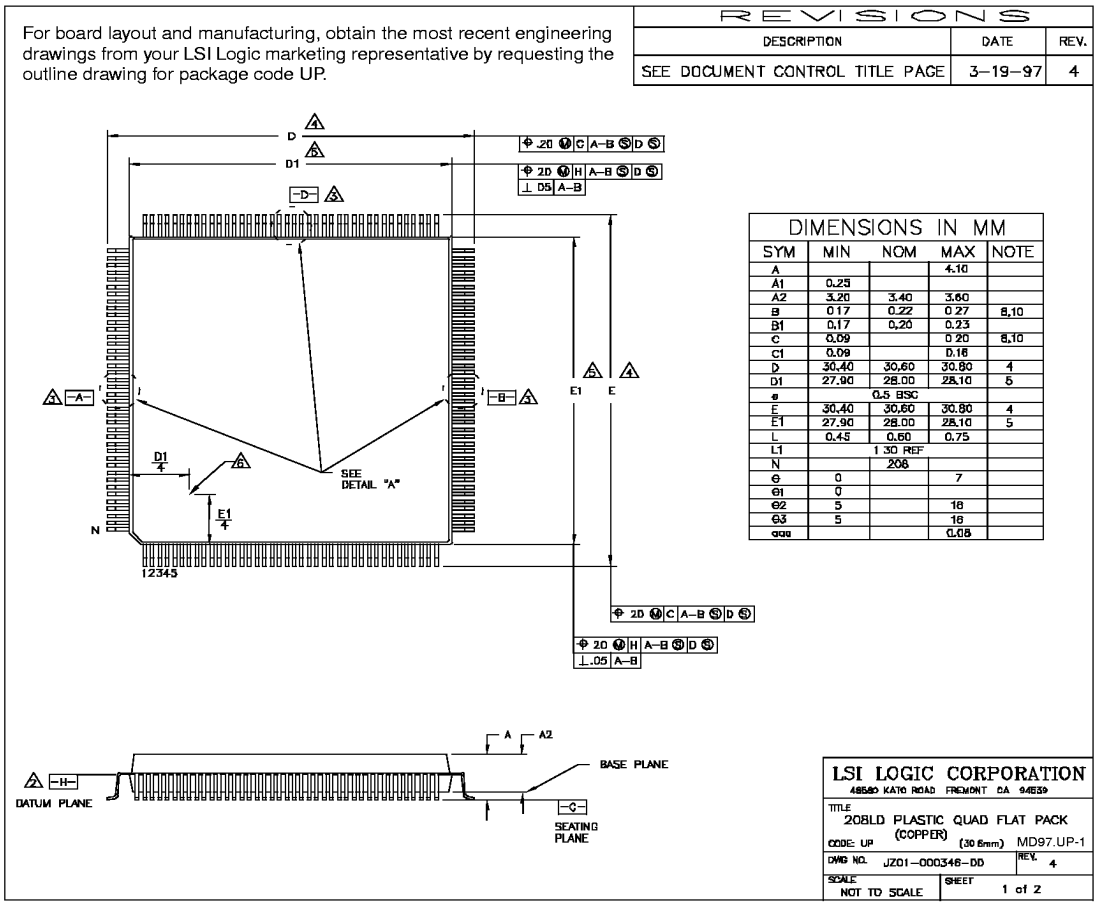
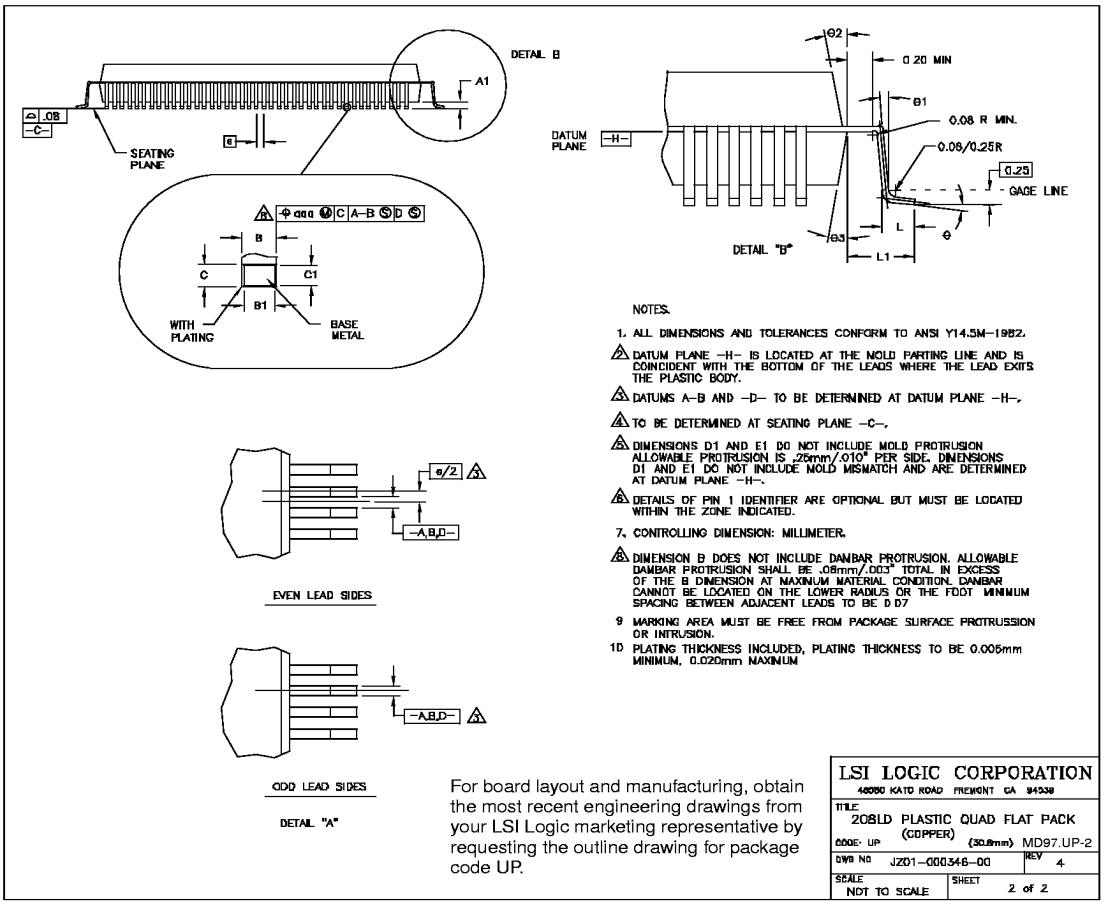


Figure 16 (Cont.) 208-pin Plastic Quad Flat Package (Sheet 2 of 2)



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