AN397
APPLICATION NOTE

Timing Specifications for Memory Products

STMicroelectronics has, for many years, committed itself to the JEDEC naming convention for the timing parameters of its memory products. Historically, timing parameter names had tended towards describing the function that was being performed during the time interval, for example:

– t_{AH} to represent the Address Hold time
– t_{DH} to represent the Data Hold time
– t_{ACC} to represent the Access time

However, these names are ambiguous. They do not specify which signals are used to indicate the start and end events, and they do not specify which transitions are involved. For example, t_{ACC} does not specify, whether this is the time from addresses becoming valid, or from the Chip Enable becoming enabled, or from the Chip Enable ceasing to be disabled.

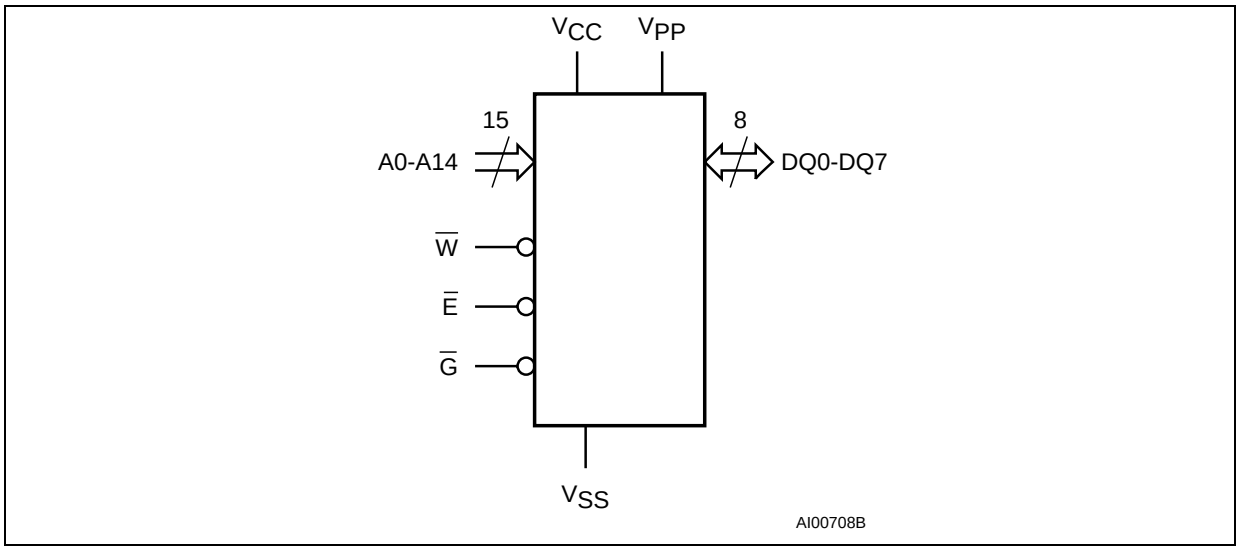
Under the JEDEC system, timing parameter names are composed from the names of the signals involved, and their corresponding logic transitions. They take the general form, t_{1234}, where 1 and 3 specify two signal names, and 2 and 4 specify the logic transitions. Each timing period consists of a start event, as specified by a given logic transition-2 on signal-1, and an end event, as specified by a given logic transition-4 on signal-3.

To help in keeping the names of the timing periods consistent between designers, there are conventions on how the signal names, 1 and 3, should be chosen, and on how the transition names, 2 and 4, should be specified. The core of the signal naming system is as follows:

– Q to represent a Data Output
– D to represent a Data Input
– A to represent an Address Line
– E to represent a Chip Enable Input
– G to represent a, Output Enable Input
– W to represent a Write Enable Input

These are shown in use for the example memory device in Figure 1.

Figure 1. Signal Names on an Example Memory Device



The naming convention for the transitions is as follows:

– H indicates the earliest moment at which the signal can be considered to be driven in the high logic state (for example, as a result of a low-to-high transition).

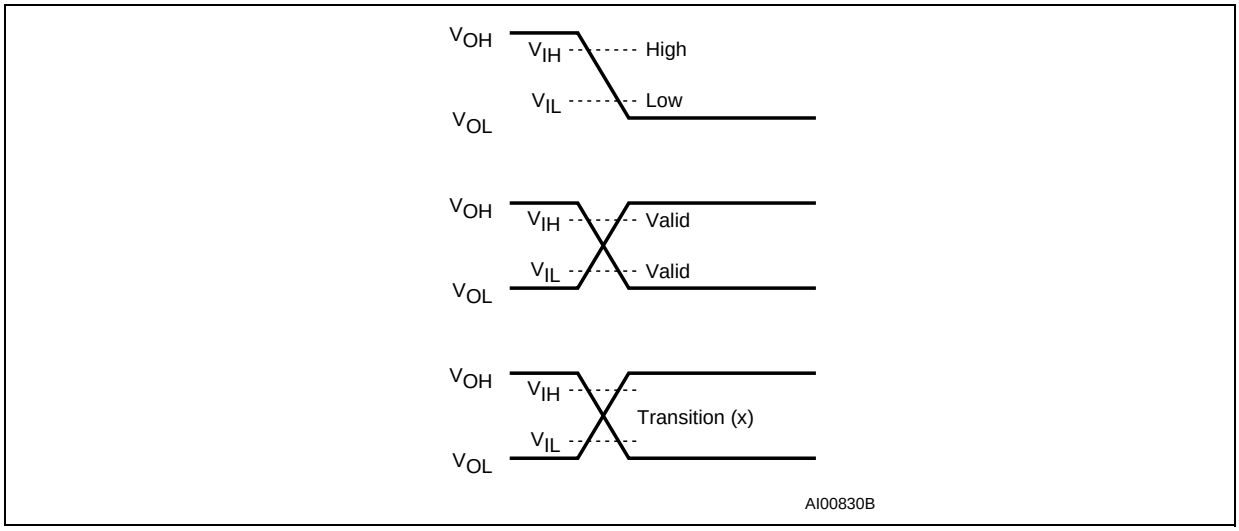
– L indicates the earliest moment at which the signal can be considered to be driven in the low logic state (for example, as a result of a high-to-low transition).

– V indicates the earliest moment at which the signal can be considered to be driven in a valid logic state, either high or low (for example, as a result of coming out of a high-to-low, or low-to-high transition, passing through the invalid state in between).

– X indicates the earliest moment at which the signal can be considered to be driven in the invalid logic state (between V_{IL} and V_{IH} in Figure 2), neither high nor low (for example, as a result of going into a high-to-low, or low-to-high transition, passing through the invalid state in between).

– Z indicates earliest moment at which the signal can be considered to be undriven, and left floating in its high impedance state.

Figure 2. Logic State Transitions on Example Input and Output Waveforms



EXAMPLES

The parameter t_{AVQV} specifies a time interval: starting from the instant when the address lines are below V_{IL} (for signals at, or going to a logic Low level) *or* above V_{IH} (for those at, or going to a High logic level); and ending at the instant when the data output signals are all below V_{IL} or above V_{IH}.

The parameter t_{EHQZ} specifies a time interval: starting from the instant when the Chip Enable input goes above V_{IH}; and ending at the instant when the data output is no longer driven.

The parameter t_{AXQX} specifies a time interval: starting from the instant when any single address line goes outside its stable, valid level; and ending at the instant when any data output line transition passes these levels, and is consequently no longer valid.

Some further examples are shown in the first column of Table 1. The second column indicates the old style of name for the same parameter. As can be seen in some of the names, the inversion bar is always omitted from signals that use negative logic. For example, $\overline{E}$ from Figure 1 appears as E in t_{ELQX} in Table 1.

Table 1. Timing Characteristics Example

Symbol	Alt.	Parameter
tAVAV	tRC	Read Cycle Time
tAVQV	tACC	Address Valid to Output Valid
tELQX	tLZ	Chip Enable Low to Output Transition
tELQV	tCE	Chip Enable Low to Output Valid
tGLQX	tOLZ	Output Enable Low to Output Transition
tGLQV	tOE	Output Enable Low to Output Valid
tEHQZ		Chip Enable High to Output Hi-Z
tGHQZ	tDF	Output Enable High to Output Hi-Z
tAXQX	tOH	Address Transition to Output Transition

Notes: 1. These are taken from the FLASH Memory data sheets.

MEASUREMENT CONDITIONS

There are a few other parameters that need to be included in the data sheets, to make the specification complete. Firstly, the limits on the output levels, as used in Figure 2, need specifying:

$V_{OH} \geq 0.8\ V_{CC}$

$V_{OL} \leq 0.2\ V_{CC}$

Next, the thresholds recognized by the input buffers, again as used in Figure 2, need specifying:

$V_{IH} \geq 0.7\ V_{CC}$

$V_{IL} \leq 0.3\ V_{CC}$

Finally, the reference voltages for the timing measurements need specifying. Let us call them V_{RH} and V_{RL}, here, but note that, because these are not physical parameters of the hardware, they are not generally given explicit names in the data sheet. However, they do appear in the “AC Measurement Conditions” table, and in the accompanying “AC Testing Input Output Waveforms” diagram. Generally, they set at V_{IH}(min) and V_{IL}(max), respectively. That is, the measurement equipment is set to recognize the logic thresholds at the same voltages as are recognized by the input buffers of the chip.

$V_{RH} = 0.7\ V_{CC}$

$V_{RL} = 0.3\ V_{CC}$

Notice, though, that this is by definition, and is not itself a measured parameter (hence the “equal” sign, rather than the “less than or equals” or “greater than or equals” sign for the bounded value.

Although, in theory, no timings depend on the rise and fall times of signals, some products may have characteristics which vary with the slew rate of the input. For an ST EPROM device, the data sheet might state “Input rise and fall times are 20 ns (max)”.

As a further point of definition, the data sheets might state that “a signal is defined as Hi-Z (high impedance) when it is not driving or being driven”.

TIMING DIAGRAMS

The JEDEC convention leads to clearer, less ambiguous timing specifications. Also, it allows a substantial simplification to be made to timing diagrams, and hence to an increase in their clarity. Since the voltage reference levels (V_{RH} and V_{RL}) are specified explicitly in the data sheet, as described in the section above, these levels do not need to be spelled out precisely each time on the timing diagram. Instead, it is sufficient to depict, diagrammatically, the timing events starting and ending at the midpoints of logic transitions, and to let the name of the parameter indicate which of the reference levels are involved.

For example, the data sheet might specify the measurement conditions, with V_{CC}=5 V, as follows:

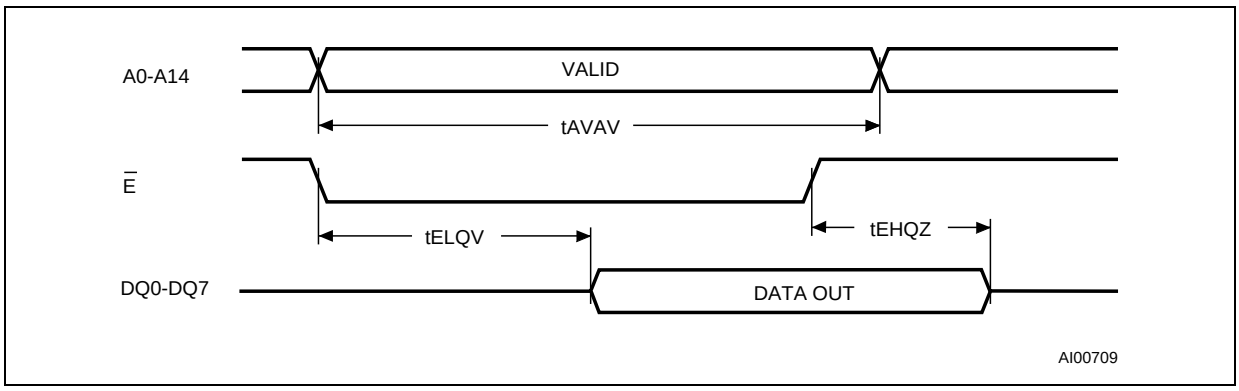
– Input Voltage levels are V_{OL}=1 V and V_{OH}=4 V
– Input and Output timing reference levels are 1.5 V and 3.5 V
– Output Hi-Z is the point where the signal is no longer driving

The parameters in the timing diagram (Figure 3) would then be interpreted as follows:

– t_{AVAV} is measured from the point where all address lines are either above 3.5 V or below 1.5 V, to the point of similar conditions at the end of the cycle.
– t_{ELQV} is measured from $\overline{E}$ being below 1.5 V, to the point when all data lines are either above 3.5 V or below 1.5 V.
– t_{EHQZ} is measured from $\overline{E}$ being above 3.5 V, to the point when the data outputs are no longer driving the signal lines.

Note that, in Figure 3, the t_{ELQV} timing, for example, is shown diagrammatically not from a “low” point on the $\overline{E}$ falling edge, but from the center, and is shown not to a “high/low” point on the Data Output but again to the center.

Figure 3. Timing Diagram (an Example)



If you have any questions or suggestions concerning the matters raised in this document, please send them to the following electronic mail address:

ask.memory@st.com (for general enquiries)

Please remember to include your name, company, location, telephone number and fax number.