



## P-Channel Enhancement-Mode Vertical DMOS FETs

## Ordering Information

BV <sub>DSS</sub> /	R <sub>DS(ON)</sub>	l <sub>D(ON)</sub> (min)	Order Numb	nber / Package		
BVDGS	(max)		TO-39	TO-92		
-60V	0.9Ω	-4A	VP2206N2	VP2206N3		

<sup>†</sup>MIL visual screening available

#### **High Reliability Devices**

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

#### Features

- □ Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- $\hfill\square$  Low  $C_{_{ISS}}$  and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- □ High input impedance and high gain
- Complementary N- and P-channel devices

## Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

## **Absolute Maximum Ratings**

Drain-to-Source Voltage	$BV_{DSS}$
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

\* Distance of 1.6 mm from case for 10 seconds.

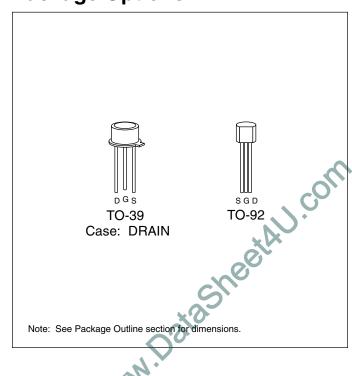
#### 11/12/01

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### **Package Options**



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## **Thermal Characteristics**

Package	I <sub>D</sub> (continuous)*	I <sub>D</sub> (pulsed)	Power Dissipation $\theta_{jc}$ @ T <sub>c</sub> = 25°C°C/W		θ <sub>ja</sub> °C/W	I <sub>DR</sub> *	I <sub>DRM</sub>
TO-39	-0.75A	-8.0A	6.0W	20.8	125	-0.75A	-8.0A
TO-92	-0.64A	-4.0A	1.0W	125	170	-0.64A	-4.0A

\* I<sub>D</sub> (continuous) is limited by max rated T<sub>i</sub>.

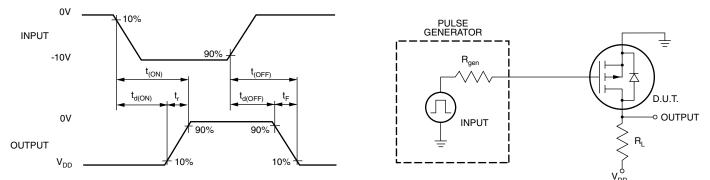
## Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Тур	Max	Unit	Conditions	
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	-60			V	$V_{GS} = 0V, I_{D} = -10mA$	
V <sub>GS(th)</sub>	Gate Threshold Voltage	-1.0		-3.5	V	$V_{GS} = V_{DS}, I_D = -10mA$	
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-4.3	-5.5	mV/°C	$V_{GS} = V_{DS}, I_D = -10mA$	
I <sub>GSS</sub>	Gate Body Leakage		-1	-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current			-50	μΑ	$V_{GS} = 0V, V_{DS} = Max Rating$	
				-10	mA	$V_{GS} = 0V, V_{DS} = 0.8$ Max Rating $T_A = 125^{\circ}C$	
I <sub>D(ON)</sub> (	ON-State Drain Current	-0.85	-2		A	V <sub>GS</sub> = -5V, V <sub>DS</sub> = -25V	
		-4	-9			V <sub>GS</sub> = -10V, V <sub>DS</sub> =- 25V	
· US(ON)	Static Drain-to-Source ON-State Resistance		1.3	1.5	- Ω	V <sub>GS</sub> = -5V, I <sub>D</sub> = -1A	
			0.75	0.9		V <sub>GS</sub> = -10V, I <sub>D</sub> = -3.5A	
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.85	1.2	%/°C	V <sub>GS</sub> = -10V, I <sub>D</sub> = -3.5A	
G <sub>FS</sub>	Forward Transconductance	0.8	1.4		2	$V_{DS} = -25V, I_{D} = -2A$	
C <sub>ISS</sub>	Input Capacitance		325	450			
C <sub>OSS</sub>	Common Source Output Capacitance		125	180	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -25V f = 1 MHz	
C <sub>RSS</sub>	Reverse Transfer Capacitance		30	40			
t <sub>d(ON)</sub>	Turn-ON Delay Time		4	15			
t <sub>r</sub>	Rise Time		16	25		$V_{DD} = -25V$	
t <sub>d(OFF)</sub>	Turn-OFF Delay Time		16	50	ns	$I_D = -4A$ $R_{GEN} = 10\Omega$	
t <sub>f</sub>	Fall Time		22	50	]		
$V_{SD}$	Diode Forward Voltage Drop		-1.1	-1.6	V	$V_{GS} = 0V, I_{SD} = -3.5A$	
t <sub>rr</sub>	Reverse Recovery Time		500		ns	$V_{GS} = 0V, I_{SD} = -1A$	

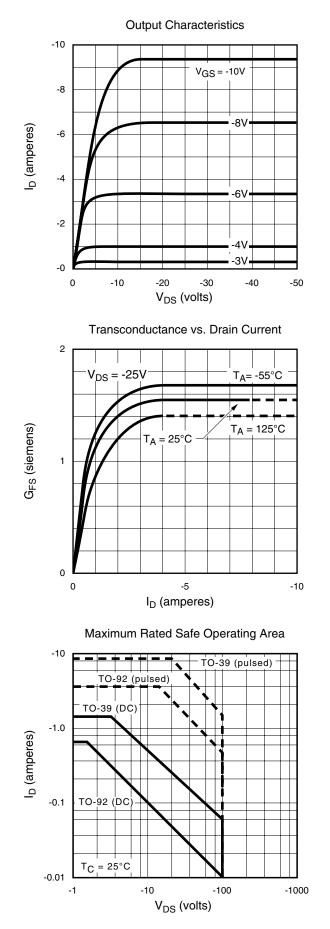
Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 µs pulse, 2% duty cycle.)

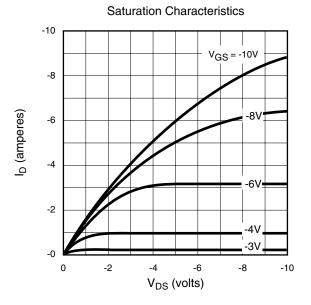
Note 2: All A.C. parameters sample tested.

# **Switching Waveforms and Test Circuit**

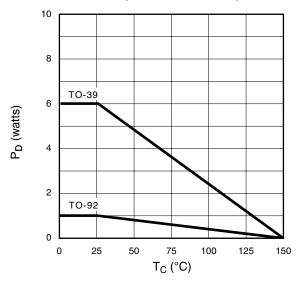


### **Typical Performance Curves**

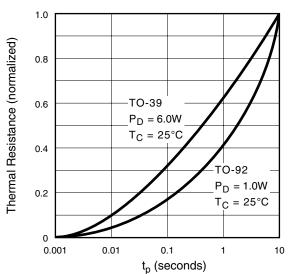




Power Dissipation vs. Case Temperature

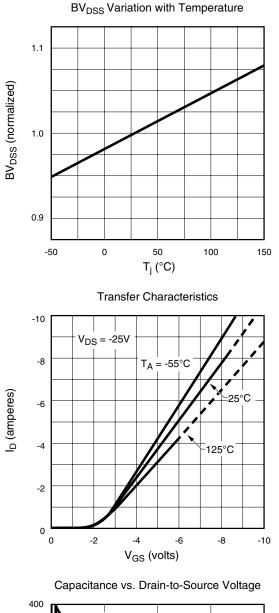


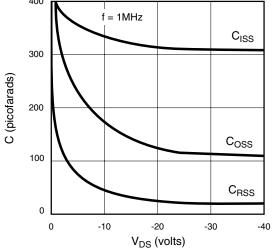
**Thermal Response Characteristics** 



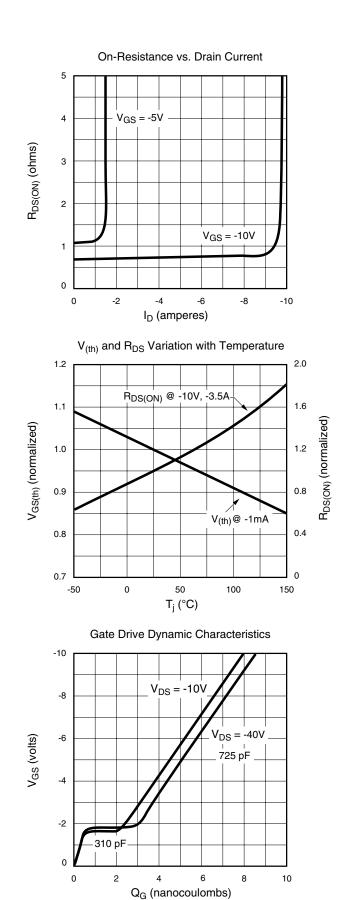
#### VP2206

### **Typical Performance Curves**









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