1024K x 9 Buffered SRAM Module with Separate I/O

Features

- **High-density 8-megabit SRAM module plus parity**
- **High-speed CMOS SRAMs**
  - **Access time of 30 ns**
- **Buffered address and control inputs**
- **Low active power**
  - **6.2W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.53 in.**
- **Small PCB footprint**
  - **1.5 sq. in.**

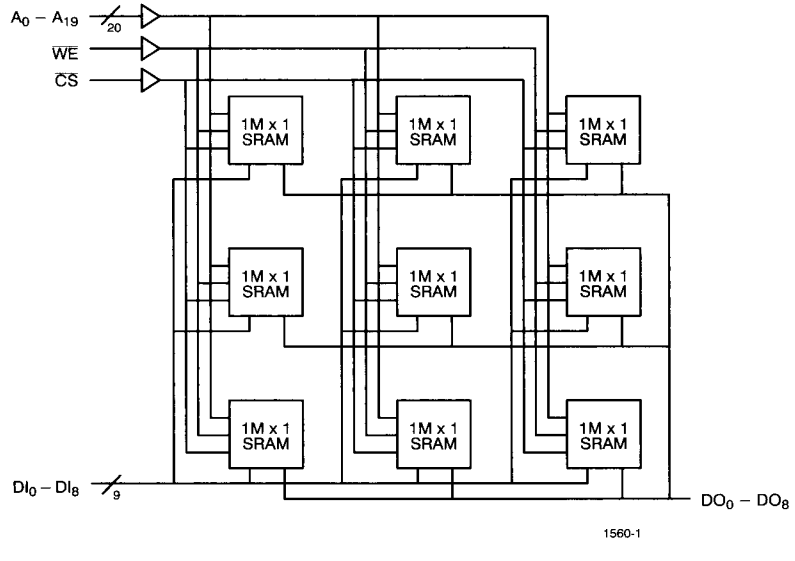
Functional Description

The CYM1560 is a very high performance 8-megabit static RAM module organized as 1024K words by 9 bits. This module is constructed using nine 1024K x 1 static RAMs in SOJ packages mounted on an epoxy laminate board with pins. Input buffers are provided on the address and control lines to reduce input capacitance and loading.

Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the data input pins (DI_0 through DI_8) of the device is written into the memory location specified on the address pins (A_0 through A_{19}). Reading the device is accomplished by taking chip select LOW while write enable remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data output pins.

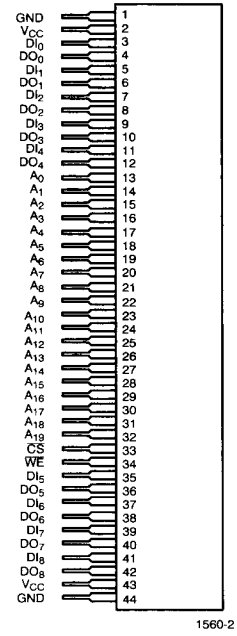
The data output pins remain in a high-impedance state when chip select is HIGH or when write enable is LOW.

Logic Block Diagram



Pin Configuration

SIP
Top View



Selection Guide

	CYM1560–30	CYM1560–35	CYM1560–45
Maximum Access Time (ns)	30	35	45
Maximum Operating Current (mA)	1125	1125	1125
Maximum Standby Current (mA)	350	350	350

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... − 45°C to +125°C

Ambient Temperature with Power Applied ..... − 10°C to +85°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.3V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1560 Min.	CYM1560 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	6.0	V
V_{IL}	Input LOW Voltage		− 0.3	0.8	V
V_{IK}	Input Clamp Level, $A_0 - A_{19}$, $\overline{CS}$, $\overline{WE}$	V_{CC} = Min., I_{IN} = − 18 mA		− 1.2	V
I_{IL}	Input Load Current	GND ≤ V_I ≤ V_{CC}	− 10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	− 10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., $\overline{CS}$ ≤ V_{IL}, I_{OUT} = 0 mA		1125	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		350	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		230	mA

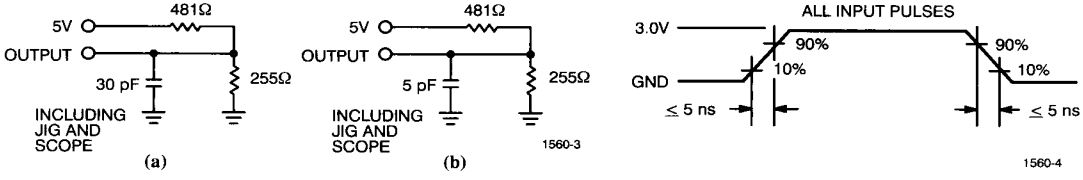
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	15	pF
C_{OUT}	Output Capacitance		20	pF

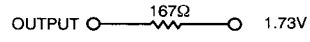
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

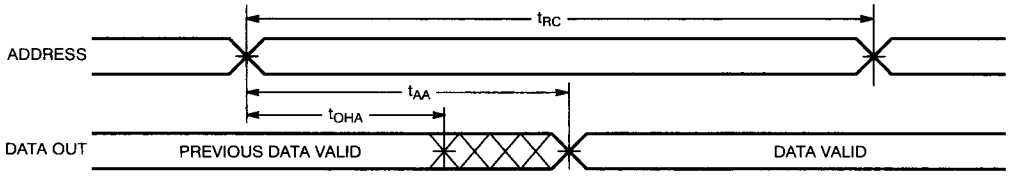
Parameters	Description	1560–30		1560–35		1560–45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	30		35		45		ns
t_{AA}	Address to Data Valid		30		35		45	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		30		35		45	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4]	2	20	2	20	2	20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	3		3		3		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		30		35		45	ns
WRITE CYCLE[5]								
t_{WC}	Write Cycle Time	30		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		35		ns
t_{AW}	Address Set-Up to Write End	20		25		35		ns
t_{HA}	Address Hold from Write End	5		5		5		ns
t_{SA}	Address Set-Up from Write Start	5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		35		ns
t_{SD}	Data Set-Up to Write End	15		20		25		ns
t_{HD}	Data Hold from Write End	5		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	2		2		2		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]	2	20	2	20	2	20	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS} = V_{IL}$.

Switching Waveforms

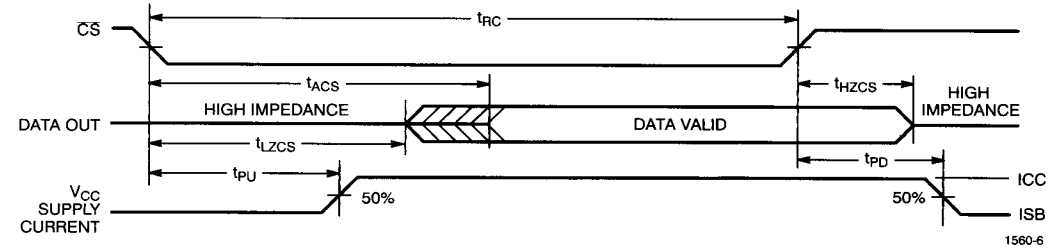
Read Cycle No. 1[6, 7]



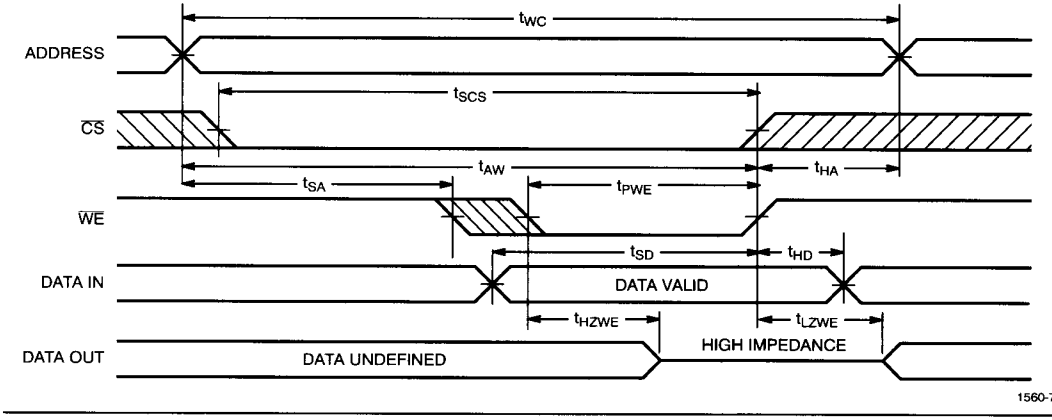
1560-5

Switching Waveforms (continued)

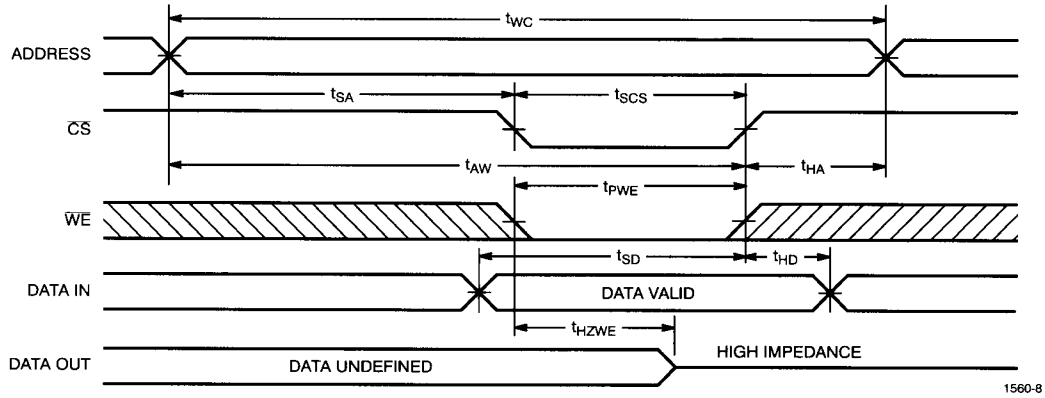
Read Cycle No. 2[6, 8]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[5]



Write Cycle No. 2 ($\overline{CS}$ Controlled)[5, 9]



Notes:

8. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	Data In	Data Out	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	X	Data Out_{0-8}	Read
L	L	Data In_{0-8}	High Z	Write

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
30	CYM1560PF–30C	PF06	44-Pin Flat SIP Module	Commercial
	CYM1560PS–30C	PS07	44-Pin Plastic SIP Module	
35	CYM1560PF–35C	PF06	44-Pin Flat SIP Module	Commercial
	CYM1560PS–35C	PS07	44-Pin Plastic SIP Module	
45	CYM1560PF–45C	PF06	44-Pin Flat SIP Module	Commercial
	CYM1560PS–45C	PS07	44-Pin Plastic SIP Module	

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