AN1263
APPLICATION NOTE

USING THE INTERNAL BOOTSTRAP CHARGE CAPABILITY OF THE L6384, 85, AND 86 IN DRIVING A SIX TRANSISTOR INVERTER BRIDGE

by: Dennis Nolan

Review of Traditional Bootstrap Circuit:

Figure 1.0 depicts a typical six transistor, three phase DC-to-AC inverter bridge which uses the BOOTSTRAP method to power the floating gate drivers for the three upper power transistors. This bridge may employ either MOSFETs or IGBTs so in this text I will use the generic term, transistor, which applies to both. Please note that the gate drivers for the three lower transistors are powered directly by the VCC power supply which is referred to signal common, which is the same circuit node as the negative side of the main DC supply bus and the source (or emitter) terminals of the lower transistors. Since the gate must be driven high with respect to the source (emitter) of the transistor, the gate drivers for the upper transistors and their respective power supplies must be referenced to the nodes labeled Va, Vb, and Vc, respectively and float up and down with these motor terminal voltages.

Consider the gate driver for transistor Qah. The power supply for this driver is the stored charge in capacitor C1. When the control for this bridge is first powered-up, but before any transistors have been gated, gating signals are applied to all three of the lower transistors for a time interval of about one or two milliseconds. During this “pre-charge” period, the negative terminals of C1, C2, and C3 are connected via a low impedance path to circuit common, which will cause current to flow through diodes D1, D2, and D3 until the bootstrap capacitors have been charged up to approximately the voltage level of Vcc. Whenever an upper transistor is turned on, its source (emitter) terminal will be pulled up nearly to the level of the plus side of the DC bus (which is normally higher than Vcc) and the positive terminal of the bootstrap capacitor will “fly up” to the level of the DC bus plus Vcc (the initial voltage it was charged up to).

In this instance the bootstrap capacitor can be thought of like a dry cell battery that is free to float up and down with the motor terminal and continue to power the gate driver. Unfortunately, unlike a battery which can continually supply output current and maintain its output voltage, a capacitor will discharge, with its voltage decreasing in direct proportion to the time integral of the current it supplies. The discharging of the bootstrap capacitors is not normally a problem, however, because the current drawn by the gate driver is very small and the normal operation of the inverter bridge offers periodic opportunities to recharge the cap.

If the inverter bridge is being used to power either an induction motor or a sinusoidally driven brushless DC motor (also called permanent magnet synchronous), then the three individual phases (Qah & Qal, Qbh & Qbl, and Qch & Qcl) are each operated simultaneously in a complementary mode so as to produce a close approximation of a three phase set of sinusoidal phase voltages, displaced from each other by 120 electrical degrees. Consider phase A. Transistor Qah and Qal are alternately gated, one gating signal being essentially the logic inverse of the other except for a short “dead time” of one or two microseconds at the transition from upper on to lower on or vice versa when both are left off. During the latter or “off” part of each pulse width modulation cycle, Qal is gated, which pulls Va to ground and provides a low impedance DC path to recharge the bootstrap capacitor.

Another gating scheme commonly used with this bridge is the so-called six step commutation method. Six step commutation is used primarily with brushless DC motors which employ three Hall effect Sensors to provide rotor position information which is used to control commutation. With six step commutation, no more than two of the six transistors are active at any one time. These transistor pairs consist of one upper and one lower transistor and are referred to as phases AB, AC, BC, BA, CA, and CB. The first letter indicates which one of the upper transistors is on while the second indicates the lower. Note that with six step commutation one of the three motor wires is always de-energized, with no current flowing in it. Pulse width modulation is most often accomplished by leaving the upper transistor on during the entire sixty degree interval for the given phase and modulating the lower one, or leaving the lower one on and modulating the upper, or sometimes modulating both on and off together.

Consider phase AB, modulating the lower transistor. During the ON part of the PWM cycle, Va is pulled up to the DC bus, Vb is pulled down to ground, C2 is being charged and C1 has lost charge equal to the required gate charge of Qah and continues to be discharged by the quiescent current requirements of the Qah gate driver plus whatever leakage currents flow in the transistor gate circuit and on the circuit board itself. During the off part of the PWM cycle, Va is still pulled up to the DC bus and Vb is also pulled up to the DC bus since the motor current that was flowing down through Qbl is now “freewheeling” up through the diode associated with Qbh. None of the bootstrap capacitors charge during this interval. If the motor should get “stuck” on this phase, either because the motor is stalled by an excessive load or it is being used in a positioning type application and being commanded to hold position (perhaps against a gravity load as would be common in a robotics type application), then the charge on C1 will eventually be depleted to the point where operation of the bridge cannot continue. Many integrated gate drivers monitor the bootstrap capacitor voltage and will shutdown when it falls below a preset threshold. We should note here that if the motor does move on to the next phase (which would be AC in normal ABC rotation sequencing), C3 will get charged but poor C1 will still get none.

The next phase, which is BC, will be of no help to our starving capacitor either, but if we can keep the motor moving into the next phase, BA, then C1 will finally get its much needed refresh charge.

Now let us consider phase AB, modulating the upper transistor. The on part of the PWM cycle is, of course, the same situation as that described previously for bottom modulation. During the off part of the PWM cycle, Vb is still pulled down to ground and Va is also pulled down to ground since the motor current that was flowing down through Qah is now “freewheeling” up through the diode associated with Qal. Both bootstrap capacitors C1 and C2 will charge during this interval. As long as the off time of the PWM is adequately long, and we should not need much time since the impedance in the charging circuit is low, this situation can be sustained indefinitely and we can loiter on any given phase for as long as we wish. It is for this reason that modulation of the upper transistor has been generally preferred when the bootstrap method is used.

Bootstrap Circuit Using the STMicroelectronics L6384, 5, and 6:

Now let us consider specifically usage of the STMicroelectronics L6384, L6385, and L6386 integrated gate drivers. These chips contain one gate driver which is referred to ground and one floating gate driver. Three of these chips would be used to operate a six transistor inverter bridge. An examination of the block diagram given in the data sheet for one of these parts will show that a major advance has been made in the design of these parts compared to previous floating driver designs since the external high voltage, fast recovery, diode is no longer required for charging the bootstrap capacitor. There are some caveats which must be observed when using these parts compared to the traditional approach using an external diode. These differences stem from the fact that, although the integrated charging circuit is referred to as a “bootstrap diode” and is drawn as such in the block diagram, this circuit is actually realized by a diode in series with a MOSFET transistor switch which is gated synchronously with the lower gate driver. This diode/MOSFET combination can be accurately modeled by

one of the two circuits presented in figure 3. Circuit one, which consists of an ideal (no forward drop) diode in series with a 0.7VDC independent voltage source and a 125 ohm resistor, is valid whenever the lower driver in on. Circuit two, the same circuit except that the voltage source is now 3.2VDC, is valid whenever the lower driver is off.

Figure 2 shows the new circuit with the diodes replaced by a diode/MOSFET series circuit. For the most part, the synchronously gated MOSFET operates very similarly to a diode in this circuit, but there can arise some subtle differences which must be considered.

In the case of sinusoidal commutation, where the upper and lower transistors of each phase are alternately gated in a nearly complimentary (except for dead time) manner, the bootstrap caps get depleted during the on part of the PWM period for each independent phase, but then get recharged during the off part, when the lower transistor is on (providing a charging path to ground) and the charging MOSFET is on (providing a charging path from Vcc). Some attention should be paid to the sizing of the bootstrap capacitor so that the time constant formed between the cap and the 125 ohms Rdson of the charging mosfet is not too large compared to the PWM off time. This will not normally present a problem, however, since the charge accumulated during the off part of the PWM cycle will probably be more than the charge lost during the on part of the cycle.

Now consider six step, phase AB again. Whether upper or lower modulation is employed, the main concern here is that while we are on phase AB, for example, the lower gate driver for phase A is never turned on and thus the MOSFET which charges C1 is never turned on. A secondary effect causes the MOSFET to behave like a conventional source follower circuit and this accounts for the additional 2.5 volts of drop shown in the equivalent circuit (the 2.5 volts is the effective gate threshold voltage of the MOSFET). If the motor loiters for too long a time without changing phase, then C1 will decay to VCC-3.2VDC, which may cause the upper driver to shut down due to undervoltage in the bootstrap cap, depending on the value of VCC. While the traditional bootstrap circuit (external diode) favors upper modulation, lower modulation is preferred when using the L6384, 5, or 6. This is because modulating the upper transistor removes charge from the bootstrap cap with every PWM cycle since the transistor gate charge is removed from the cap every time the transistor is turned on. With lower modulation, the situation with the upper driver is static and we have only leakage currents discharging the cap. This situation forestalls the eventual shutdown, it does not eliminate it.

One possible modification of the six step gating scheme steals from synchronous rectification methodology. If we employ the conventional top modulation six step gating scheme we know that, if we are on phase AB for example, during the off part of the PWM cycle current will be freewheeling up through the diode associated with Qal. There is no reason why we cannot go ahead and turn on Qal during this interval. The MOSFET is just as happy operating in the third quadrant (reverse voltage and reverse current) as in the first, and the voltage drop across the device will actually be lower giving rise to lower device power dissipation (ALA synchronous rectification). An IGBT will not conduct in the third quadrant but it won't hurt anything to gate it. Of course, since the lower gate driver is on, the capacitor charging MOSFET is on and C1 gets its refresh. We should mention here that a "dead time" must be allowed between turning off the upper and turning on the lower transistor or vice versa to allow for the turnoff time of the transistor. This will generally be just a few microseconds.

Peak Bootstrap Voltage may be Lower Compared to Diode Circuit:

A final caveat. When we use six step commutation with upper modulation and the traditional bootstrap circuit (which employs the fast external diode), during charging the negative terminal of the capacitor is connected to the cathode of a freewheeling diode which is carrying heavy current. Since the anode of this freewheeling diode is connected to ground, the cathode will normally be driven from 1.0 to 1.5 volts below ground. As long as heavy

current flows through the diode, this point can be thought of as a low impedance voltage source at -1.0 to -1.5 volts. The positive terminal of the cap connects to Vcc via the fast recovery diode. This charging circuit has a total charging potential of Vcc plus 1.0 to 1.5Vdc available to charge the cap. Some voltage will be lost across the diode, but current will be low at the end of the charging cycle, this drop will probably be only a few tenths of a volt. With the internal charging circuit method, whenever the cap is being charged the lower MOSFET is on and current is flowing down through the device. This will bring the negative terminal of the bootstrap capacitor above ground to a voltage of Rdson times the load current. This will probably get in the neighborhood of 0.5vdc or so. This give a total charging circuit potential of Vcc minus 0.5Vdc. The net effect of this difference could be a lower bootstrap capacitor voltage on the order of 1.0 to 2.0 volts. If Vcc is 15Vdc this is not likely to be a concern. If Vcc is 12Vdc or lower, it may pose a problem.

If All Else Fails:

A final note. Any of these problems can be circumvented by putting an external diode around the part anyhow. The bootstrap circuit will then work pretty much in the traditional manner.

Figure 1.

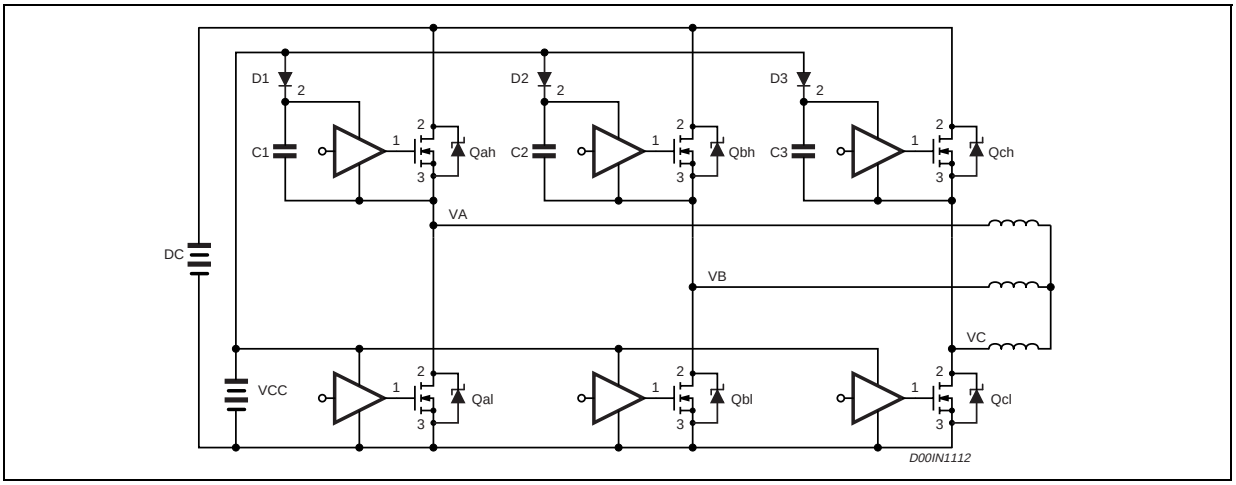


Figure 2.

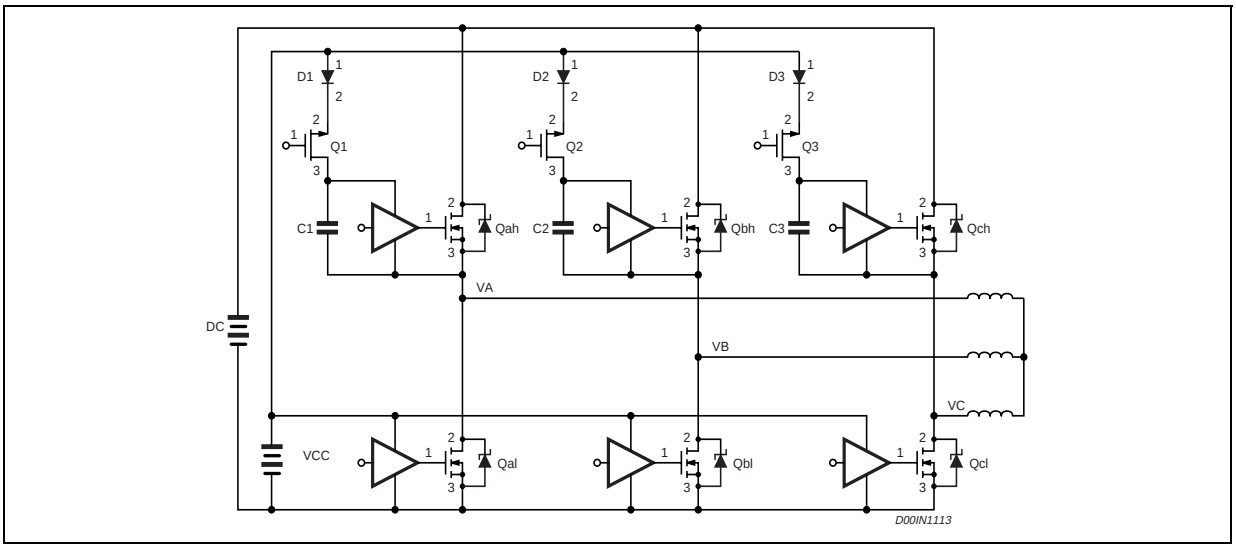
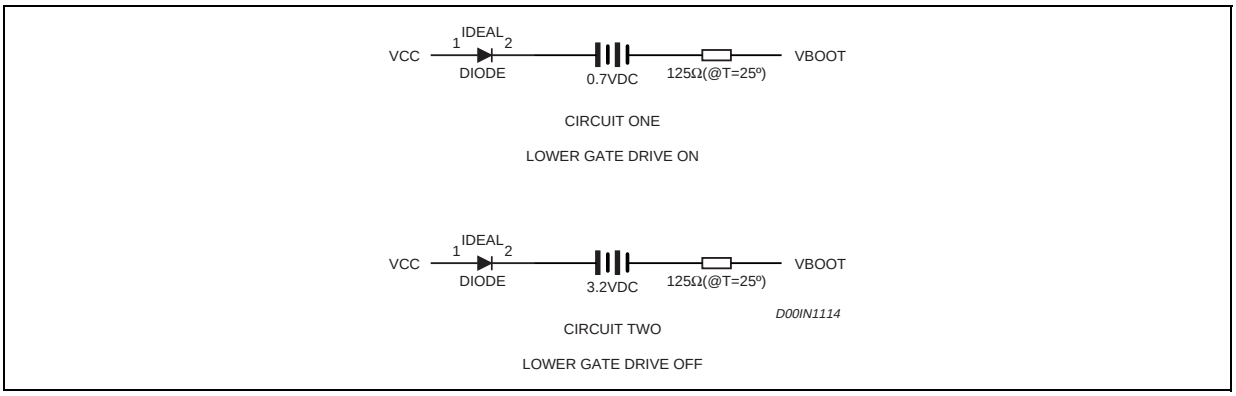
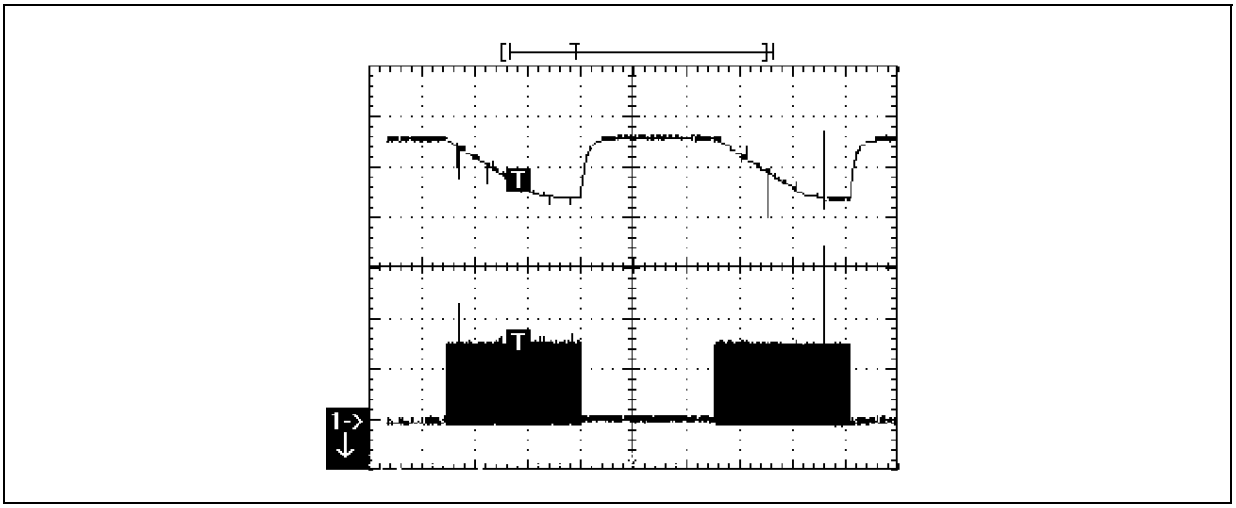


Figure 3. Equivalent Circuit for Internal B00tstrap Charging Path





NOTES:

The upper plot (channel 2) is the 1.5µF bootstrap capacitor voltage at 2.0 volts per division.

The zero reference for channel 2 is the bottom major graticule.

The lower plot (channel 1) is the output voltage at 10.0 volts per division

The zero reference for channel 1 is one major division up from the bottom.

Timebase is 2.0 milliseconds per division

VBUS is set at approximately 18VDC.

VCC for the L6385 is set to precisely 14.0VDC.

OBSERVATIONS:

In this configuration, the circuit alternates between two operating modes, A and B. In mode A, HIN is gated at 25 KHZ and LIN is held low. The plot shows the output voltage switching between groung and Vbus while the bootstrap voltage decays. In mode B, HIN is held low while LIN is held high, allowing the bootstrap cap an opportunity to charge up to within one volt of VCC. This alternate mode switching closely resembles the situation found in six step modulation.