Increased Clock Speeds and Faster Initial Burst Access on Am29BDD160G

Application Note

July 2003

The following document refers to Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this document as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal documentation improvements and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

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Modification to Burst Initial Access Delay Control and CFI Device Geometry Definition– Revision 4a versus Revisions 4 and Earlier

Application Note

INTRODUCTION

This Application Note discusses design improvements to the Am29BDD160G. Technology and application developers are increasingly requiring Flash memory with higher clock speeds and faster access times. This is particularly true for the automotive market in anti-lock braking, engine control, and transmission control applications. One of the factors affecting system performance is the interface between the Flash memory and the microprocessor. Flash memory in burst mode (synchronous) requires a longer access time for the initial access than subsequent accesses (as fast as one clock cycle at 66 MHz). Flash burst initial access delay is therefore an important factor influencing system performance.

AMD is the world leader in Flash memory design, development and production, and is committed to continuous improvement of Flash memory capability. The Am29BDD160G 16 megabit Flash memory is a prime example of how this commitment is driving design modifications. Improvements to the Am29BDD160G have resulted in significantly decreased the burst initial access delay. The number of wait states associated with the burst initial access in Revision 4a (versus all previous revisions) has been decreased by one state across all frequencies. The Am29BDD160G now provides for a 66 MHz operation with a burst initial access time of five clock cycles and subsequent burst access time of one clock cycle (also known as 5-1-1-1… at 56 MHz and 66 MHz).

Design improvements require changes to both the silicon revision level (incremented from 4 to 4a) and the Am29BDD160G datasheet revision level (incremented from B to C). There are three areas of discussion:

- **Initial Access Delay Control**

User Configurable Control Register determines the initial access delay in burst mode i.e., Initial Access Delay Control (Burst Control Configuration). Allows for proper configuration of the Flash memory to match the microprocessor interface.

- **CFI Device Geometry Definition**

Fixed configuration information in Common Flash Memory Interface i.e., CFI Device Geometry Definition containing details about memory size, word–size, and erase block configuration.

- **Summary of Silicon Revision 4 and 4a Differences**

Discussion of differences between silicon revision 4 from 4a with respect to external attributes (such as part number, part marking) and internally through interrogation of Flash configuration registers (software). This third section also discusses issues that should be considered when different revision level devices are used.

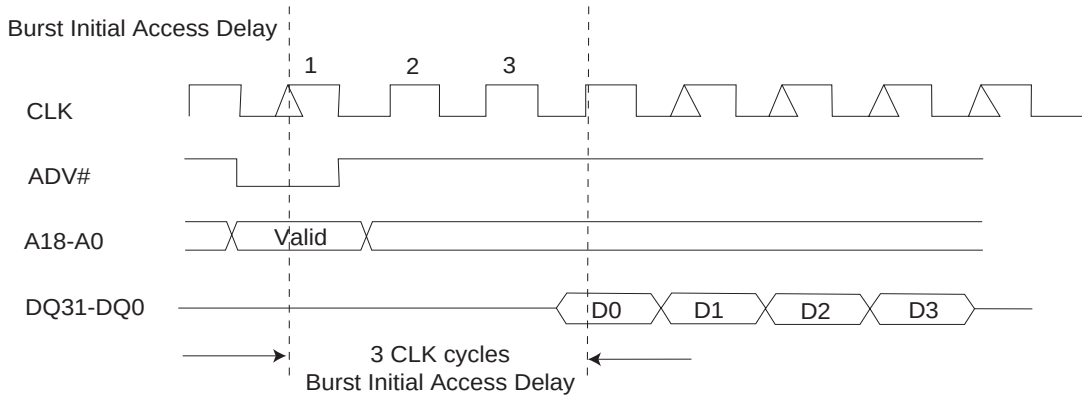
BURST INITIAL ACCESS DELAY CONTROL (BURST CONTROL CONFIGURATION)

Design modifications have decreased the Burst Initial Access Delay by one clock cycle for all control register configuration values and for frequencies up to 66 MHz. Configuration Registers CR13 through CR10 determine the Burst Initial Access Delay. The Burst Initial Access Delay is defined as the number of CLK cycles that must elapse from the first valid clock edge after ADV# assertion (or the rising edge of ADV#) until the first valid CLK edge when the data is valid. Figure 1 and Table 1 are valid for the majority of applications, and have the following operating conditions:

1. Burst initial access starts with the first CLK rising edge after ADV# assertion.
2. Configuration Register 6 is set to 1 (CR[6] = 1). Burst starts and data outputs on rising CLK edge.

For a complete discussion of this and other operating conditions see the Am29BDD160G datasheet (Publication# 24960 Rev: C or later).

For example, Revision 4 control register setting CR[13-10] = 0010 results in a Burst Initial Access Delay of five clock cycles; while Revision 4a the same control register setting results in a Burst Initial Access Delay with four clock cycles.



Notes:

1. *Burst access process starts when rising CLK edge after ADV# assertion.*
2. *Configuration register 6 is set to 1 (RC[6] = 1). Burst starts and data outputs on Rising CLK edge.*

Figure 1. Burst Initial Access Delay Control

Table 1. Burst Initial Access Delay Control

Configuration Register Setting				Burst Initial Access Delay (CLK cycles)	
CR13	**CR12**	**CR11**	**CR10**	**Rev. 4**	**Rev. 4a**
0	0	0	0	**3**	2
0	0	0	1	**4**	3
0	0	1	0	**5**	4
0	0	1	1	**6**	5
0	1	0	0	**7**	6
0	1	0	1	**8**	7
0	1	1	0	**9**	8
0	1	1	1	**10**	9

CFI DEVICE GEOMETRY DEFINITION

The Am29BDD160G datasheet (Publication number 24960) Table 13 through Table 16 details the CFI device information. These tables outline the Flash device and host system software interrogation handshake that allows specific vendor-specific software algorithms to be used for entire families of devices. Table 15 details the CFI Device Geometry such as memory size (capacity), interface description (8,16, 32 bit word size), and erase block region information. The quantity of erase blocks regions is stored in memory location 2Ch for a 32 bit wide word (or 58h for a 16 bit wide word). Revision 4 has a value of 4h while for Revision 4a has a value of 3h. A query returns a correct result in both cases. Table 2 shows the valid configuration information for the number of erase block regions within the device.

All devices have three usable Erase Blocks. Revisions 4 and earlier have a fourth Erase Block; however, that Erase Block has a size of 0 x 0 Kb. This is a zero length block and is effectively not present. Revision 4a removed the fourth Erase Block and modified the CFI Device Geometry Definition accordingly. See Table 3. This change allows for a distinction of the two revisions by querying the CFI information table.

Table 2. CFI Geometry Data

Address (x32 Mode)	Address (x16 Mode)	Data	Description
2Ch	58h	3h or 4h	Number of Erase Block Regions within device
		3h	For Flash Part Numbers: Am29BDD160GX54CYZ, Am29BDD160GX65DYZ, Am29BDD160GX64CYZ, and Am29BDD160GX65AYZ, where X, Y, and Z reflect user selectable options, i.e. X = Boot Sector, Y = Package, Z = Temperature
		4h	For Flash Part Numbers: Am29BDD160GX80CYZ, Am29BDD160GX90AYZ, and Am29BDD160GB–DS3/4/5/6/7, where X, Y, and Z reflect user selectable options, i.e. X = Boot Sector, Y = Package, Z = Temperature. These part numbers are obsolete and are replaced by the above parts

Table 3. Erase Block Region Configurations

Erase Block Region	Revisons 4 and Earlier	Revision 4a	Description
1	8 x 8 Kb	8 x 8 Kb	Same size
2	30 x 64 Kb	30 x 64 Kb	Same size
3	8 x 8 Kb	8 x 8 Kb	Same size
4	0 x 0 Kb	None	Block of 0 x 0 is unusable and is effectively not present

SUMMARY OF SILICON REVISION 4 AND 4A DIFFERENCES

Hardware/Physical Considerations

Burst Initial Access Delay Control

Revision 4 and 4a differ by one clock cycle for a particular setting. See burst initial delay access discussion above for details.

CFI Device Geometry Definition, Number if Erase Block Regions, memory location 2Ch while in x32 mode)

Revision 4 has a value of 4h while Revision 4a has a value of 3h.

Software Considerations

CFI Device Geometry Definition

The CFI Device Geometry Definition change between revisions provides software/firmware to determine of the revision level of a given Flash device by interrogating the CFI information. Software/firmware can then program the device appropriately for proper operation by programming the Burst Initial Access Delay. This assumes that the Flash device has a speed rating (D, C, or A) compatible with the microprocessor.

Datasheet/Part Number Considerations

Device Speed and Clock Rate Information

The Product Selector Guide and Ordering Information sections in the Datasheet have details on device speed and clock rate.

Revisions 4 and earlier have options for 80C and 90A while Revision 4a has options for 54D, 64C, and 65A. The 80C and 90A options for Revisions 4 are obsolete with Revision 4a.

Ordering information (Part Number)

Revisions 4 and earlier have the following valid combinations, which are obsolete with Revision 4a:

Am29BDD160GX80CYZ, Am29BDD160GX90AYZ, and AM29BDD160GB-DS3/4/5/6/7

Revision 4a has the following valid combinations:

Am29BDD160GX54DYZ, Am29BDD160GX64CYZ, Am29BDD160GX65AYZ,and Am29BDD160GY65DYZ

Note:
X, Y, and Z reflect user selectable options, i.e. X = Boot Sector, Y = Package, Z = Temperature

Additional Considerations

It is important that each user understand that the microprocessor of choice must be paired to a Flash device with a compatible speed and clock rate. Achieving intended operation of the system is not just a matter of interrogating the CFI Device Geometry Definition to determine the revision level and configuring the Flash device. For example:

A Flash Device must meet or exceed the microprocessor clock speed. Assume that a Revision 4 (or earlier revision) Flash device with a Device Speed and Clock Rate of 80C (80 ns, 56 MHz) is used. Then later, when a revision 4a device replaces the Revision 4 device, a Flash Device Speed and Clock Rate 65A (65 ns, 40 MHz) cannot be used. The reason is the 65A part has a maximum clock rate of 40 MHz, which is less than the 80C Revision 4 device.

The example above demonstrates that simply interrogating the CFI Device Geometry Definition to determine the revision level is not sufficient. There is no way to determine that an A (40 MHz) device is in a system clocked at a C speed (56 MHz). The device must be capable of operating properly at the microprocessor clock speed.