8. ELECTRICAL SPECIFICATIONS

Thermal condition

In terms of temperature characteristics, forced air cooling is assumed. Forced air of at least 1.5m/s is required under the worst condition. This may depend on pertinent conditions.

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}		-0.5 to +7.0	V
Input voltage	V_I*		-0.5 to +7.0	V
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		-65 to +150	°C

*: V_I is allowed to be up to -3.0V, if the pulse does not exceed 15ns.

Note: Never ground any output.

DC Characteristics (Ta=0 to +70°C, V_{DD}=+5V±5%)

Parameter	Symbol	Conditions	25MHz		33MHz		Unit
			MIN.	MAX.	MIN.	MAX.	
High level output voltage	V_{OH}	V_{DD}=Min. I_{OH}=-4mA	3.5		3.5		V
High level output voltage*3	V_{OHC}	V_{DD}=Min. I_{OH}=-4mA	4.0		4.0		V
Low level output voltage	V_{OL}	V_{DD}=Min. I_{OL}=4mA		0.4		0.4	V
High level input voltage	V_{IH}		2.0	V_{DD} +0.5	2.0	V_{DD} +0.5	V
Low level input voltage*1	V_{IL}		-0.5	0.8	-0.5	0.8	V
High level input voltage*2	V_{IHS}		3.0	V_{DD} +0.5	+3.0	V_{DD} +0.5	V
Low level input voltage*2	V_{ILS}		-0.5	0.4	-0.5	0.4	V
Supply current	I_{DD}	V_{DD}=5.25V Ta=70°C		850		1000	mA

*1: V_{IL} is allowed to be up to -3.0V, if the pulse does not exceed 15nS.

*2: V_{IHS} and V_{ILS} are applicable to the Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, and $\overline{\text{Reset}}$ pins.

*3: V_{OHC} is applicable to the $\overline{\text{Run}}$ and $\overline{\text{Exception}}$ pins.

Leakage Current

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Low level output leakage current	I_{OZL}	V_{DD}=5.25V V=0V	-100	+100	uA
High level output leakage current	I_{OZH}	V_{DD}=5.25V V=5.25V	-100	+100	uA
Low level input current	I_{IL}	V_{DD}=5.25V V=0V	-100	+100	uA
High level input current	I_{IH}	V_{DD}=5.25V V=5.25V	-100	+100	uA

Test Conditions for AC Test

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
High level input voltage	V_{IH}		3.0		V
Low level input voltage	V_{IL}			0.4	V
High level input voltage*	V_{IHS}		3.5		V
Low level input voltage*	V_{ILS}			0.4	V

*: V_{IHS} and V_{ILS} are applicable to the Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, CpBusy, and $\overline{\text{Reset}}$ pins.

Capacitance (Ta=0 to +70°C, V_{DD}=+5V±5%)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input capacitance	C_{In}			10	pF
Output capacitance	C_{out}			10	pF
Load capacitance	C_{Ld}			50	pF
Load capacitance*	C_{Lds}			10	pF

*: C_{Lds} is applicable to the $\overline{\text{Exception}}$, $\overline{\text{Run}}$, CpBusy, CpCond1, and $\overline{\text{CpSync}}$ pins.

AC Characteristics (Ta=0 to +70°C, V_{DD}=+5V+5%)

Remarks: 1.5V is used for all timing levels.

Parameter	Symbol	Conditions	25MHz		33MHz		Unit
			MIN.	MAX.	MIN.	MAX.	
Clock high level width	T_{CkHigh}	*2	8		6		nS
Clock low level width	T_{CkLow}	*2	8		6		nS
Clock frequency	T_{CkP}		20	100	15	100	nS
Clk2xSmp Delay (vs. Clk2xSys)	T_{DSS}		0	$\frac{T_{Cyc}}{4}$ *1	0	$\frac{T_{Cyc}}{4}$	nS
Clk2xRd Delay (vs. Clk2xSmp)	T_{DRS}		0	$\frac{T_{Cyc}}{4}$	0	$\frac{T_{Cyc}}{4}$	nS
Clk2xPhi Delay (vs. Clk2xSmp)	T_{DPS}		5	$\frac{T_{Cyc}}{4}$	4.5	$\frac{T_{Cyc}}{4}$	nS

*1: $T_{Cyc} = 2 \times T_{CkP}$

*2: tr, tf ≦ 5ns: 25MHz operation;
tr, tf ≦ 2.5ns: 33MHz operation

Run Cycle Parameters

Parameter	Symbol	Conditions	25MHz		33MHz		Unit
			MIN.	MAX.	MIN.	MAX.	
Data enable	T_{DEn}			-1.5		-1.0	nS
Data disable	T_{DDis}			-0.5		-0.5	nS
Data valid	T_{DVal}	Load capacitance = 25pF		3		2.5	nS
Write delay	T_{WrDly}			3		3	nS
Data set up	T_{DS}		6		5		nS
Data hold	T_{DH}		-1.5		-1.0		nS
Access type (1:0)	T_{ACTY}	Load capacitance = 25pF		5		4	nS
Access type (2)	T_{AT2}			12		8.5	nS
Memory write	T_{MWr}		0	18	0	8.5	nS
Address valid	T_{AVal}			3		2	nS
Exception	T_{EXC}		0	5	0	3.5	nS
Interrupt set up	T_{IntS}		7		5		nS
Interrupt hold	T_{IntH}		-1.5		-1.0		nS
CpBusy delay	T_{CpBusy}			10		7	nS
CpCond1 delay	$T_{CpCond1}$			25		17	nS
$\overline{\text{FpInt}}$ delay	T_{FpInt}	Load capacitance = 25pF		25		19	nS

Stall Cycle Parameter

Parameter	Symbol	Conditions	25MHz		33MHz		Unit
			MIN.	MAX.	MIN.	MAX.	
Stall address valid	T_{SAVal}	Load capacitance = 25pF		20		15	nS
Access type	T_{SACTy}			18		9.5	nS
Memory read initiation	T_{MRdI}			18		9.5	nS
Memory read termination	T_{MRdT}			5		3.5	nS
Run termination	T_{StI}		0	10	0	8	nS
Run initiation	T_{Run}		0	4	0	3	nS
Memory write	T_{SMWr}	Load capacitance = 25pF		18		9.5	nS
Exception valid	T_{SEXC}			15		9	nS

Reset, Mode Parameters

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Reset pulse width	T_{Reset}	$T_{Cyc} \leqq 67nS$	200		uS
		$T_{Cyc} > 67nS$	3000		T_{Cyc}
Mode set up	T_{ModeS}		20		T_{Cyc}
Mode hold	T_{ModeH}		0		nS

*: $T_{Cyc}=2xT_{CKP}$

Load Coefficient (delay time for a given load capacitance)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Load coefficient	CLD		0.5	1	ns/25pF

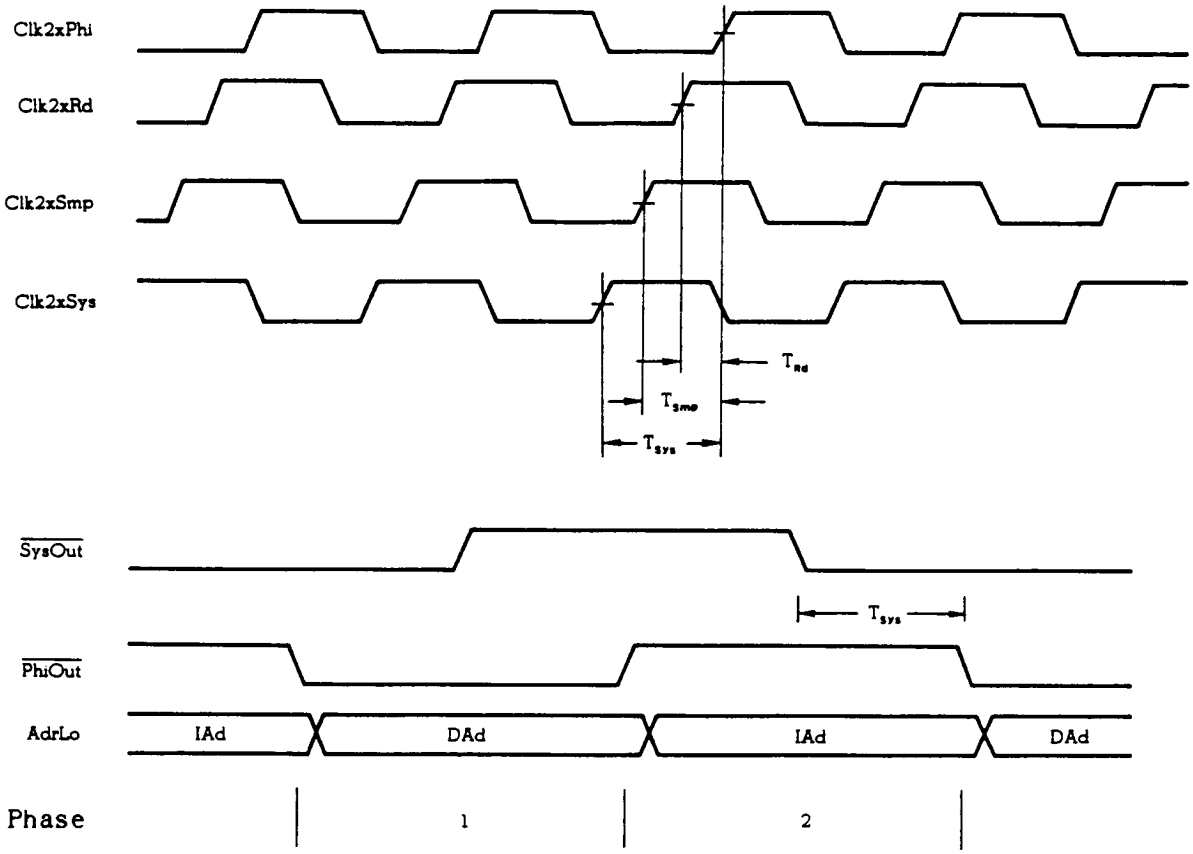
Timing Chart

Symbols in the table below are used in the following timing charts.

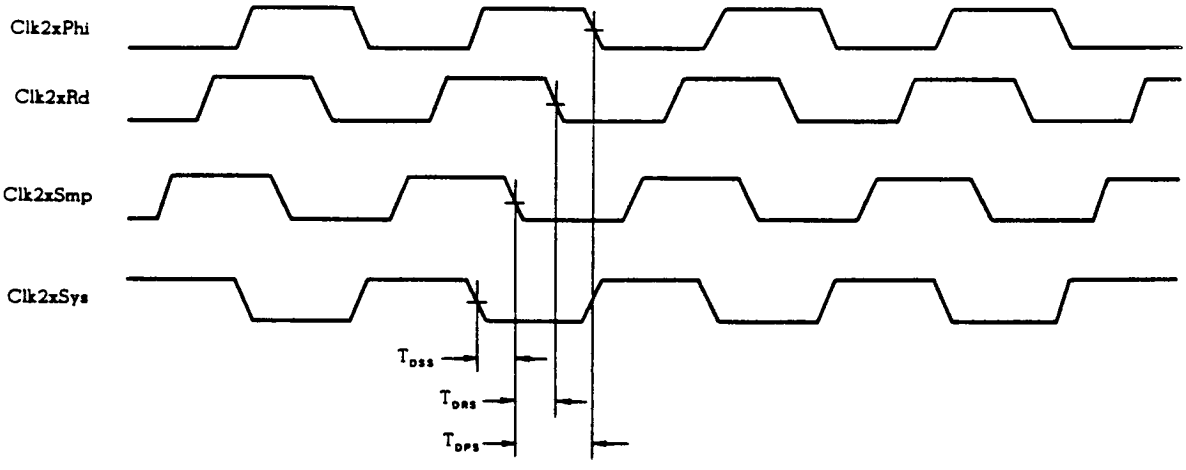
Symbol	Meanings
D	Data
I	Instructions
!	Unused data
#	Invalid data
Data:	D (31:0), DP (3:0)
Tag:	Tag (31:0), Tag P (2:0), Tag V
AdrLo:	AdrLo (17:0)

Phase Clock

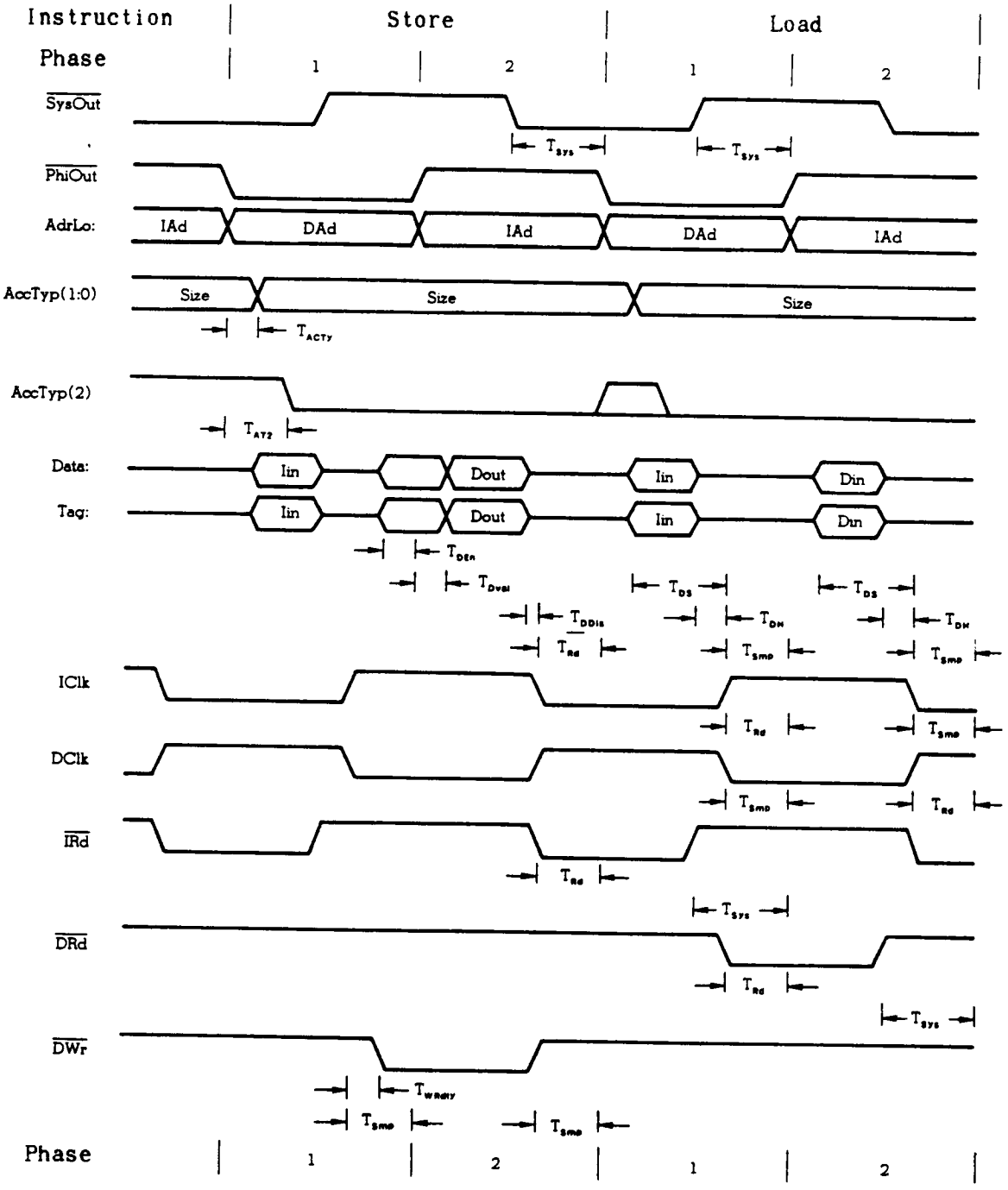
Each input/output signal timing for the V_R3600 can be adjusted by the phase differential of the 4-phase clock.



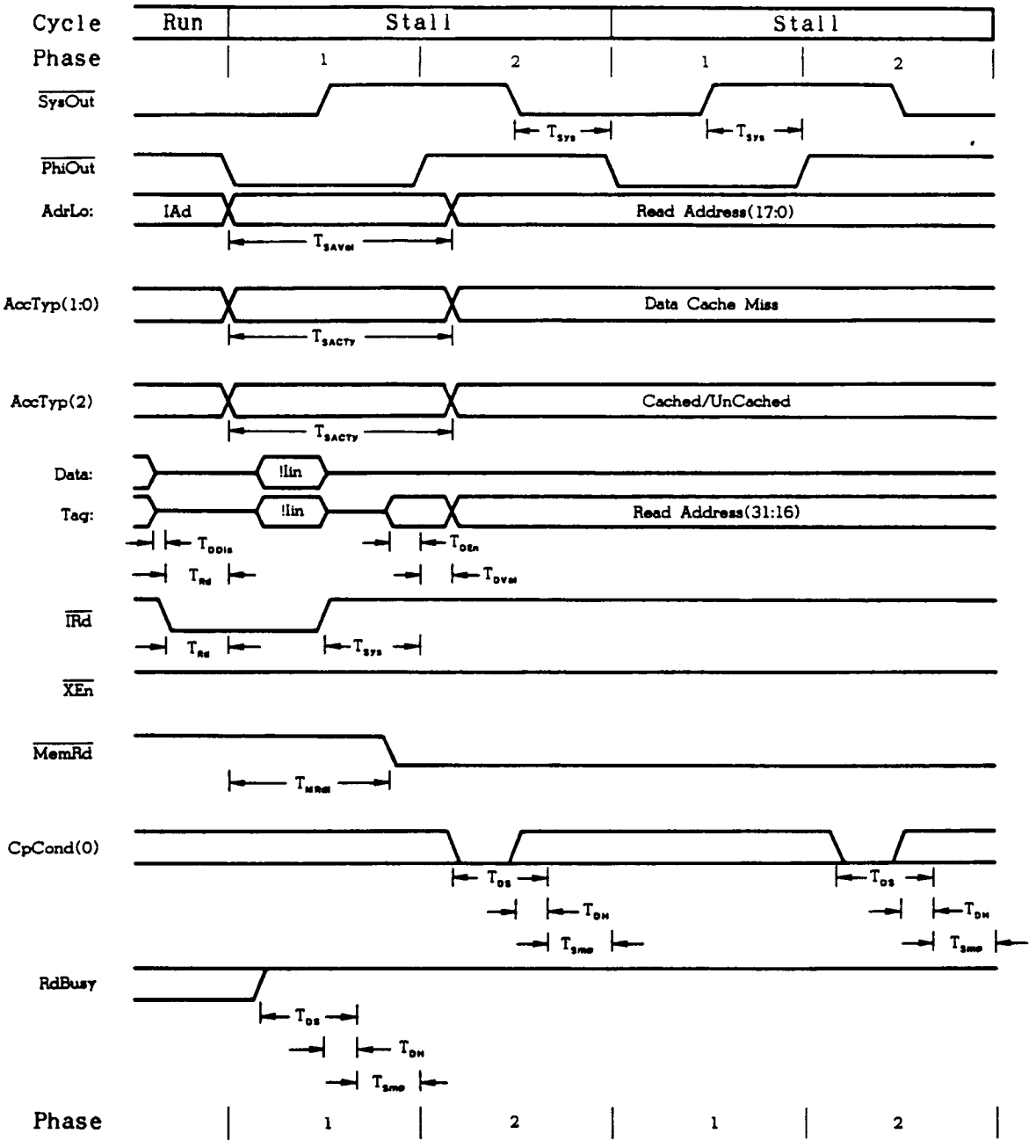
Clock



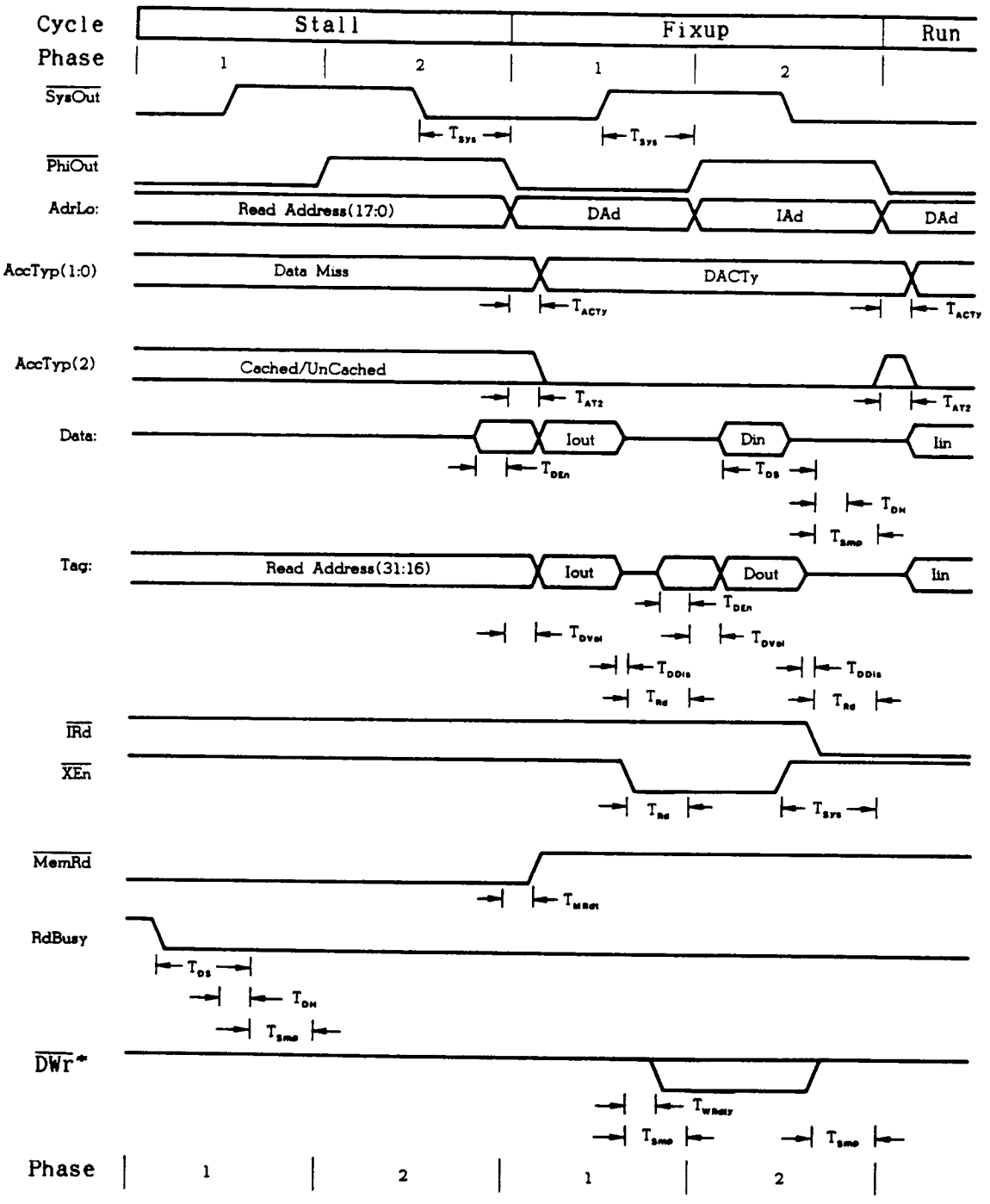
Cache Timing



Single Word Data Transfer - Beginning of Stall

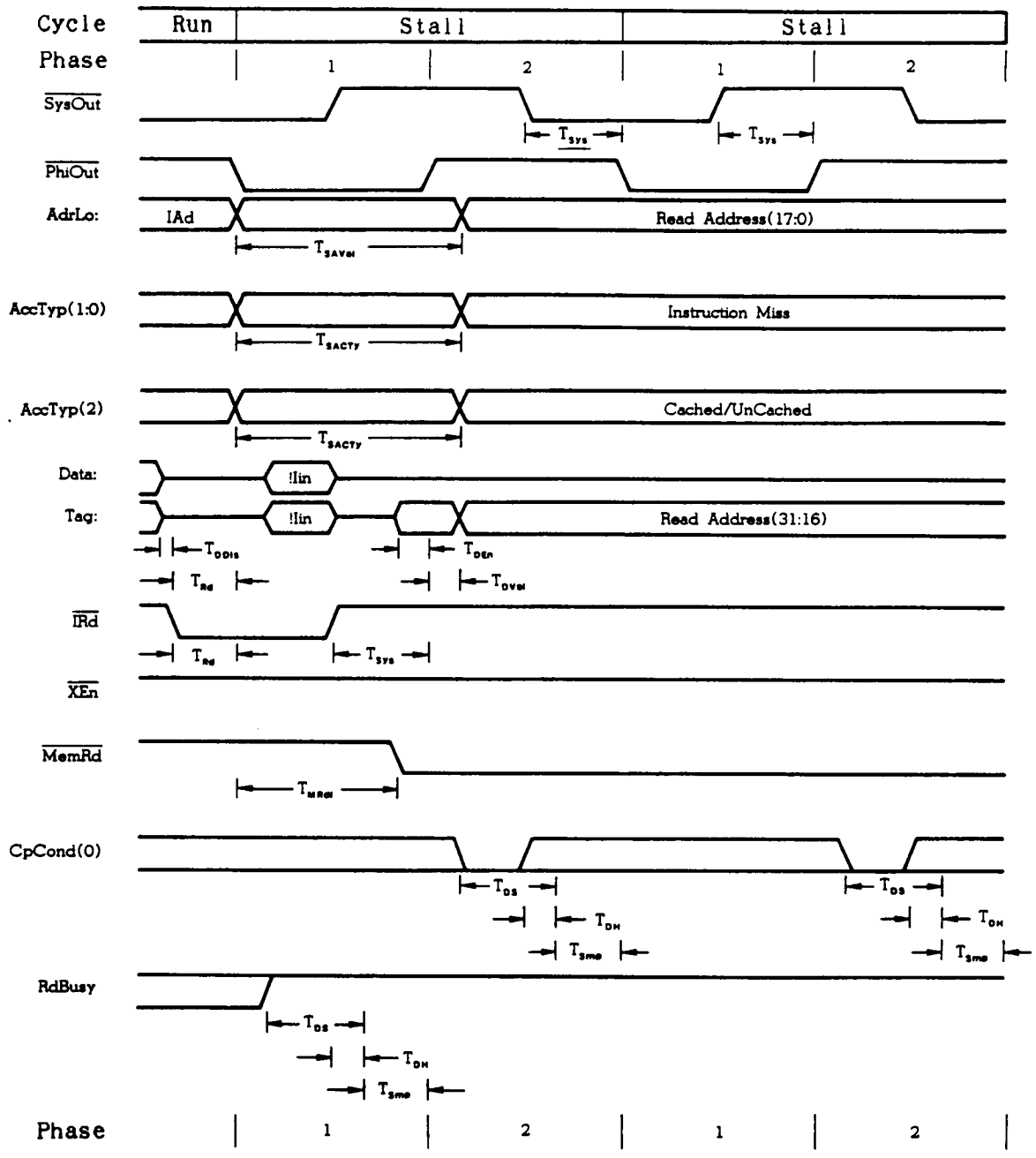


Single Word Data Transfer - End of Stall

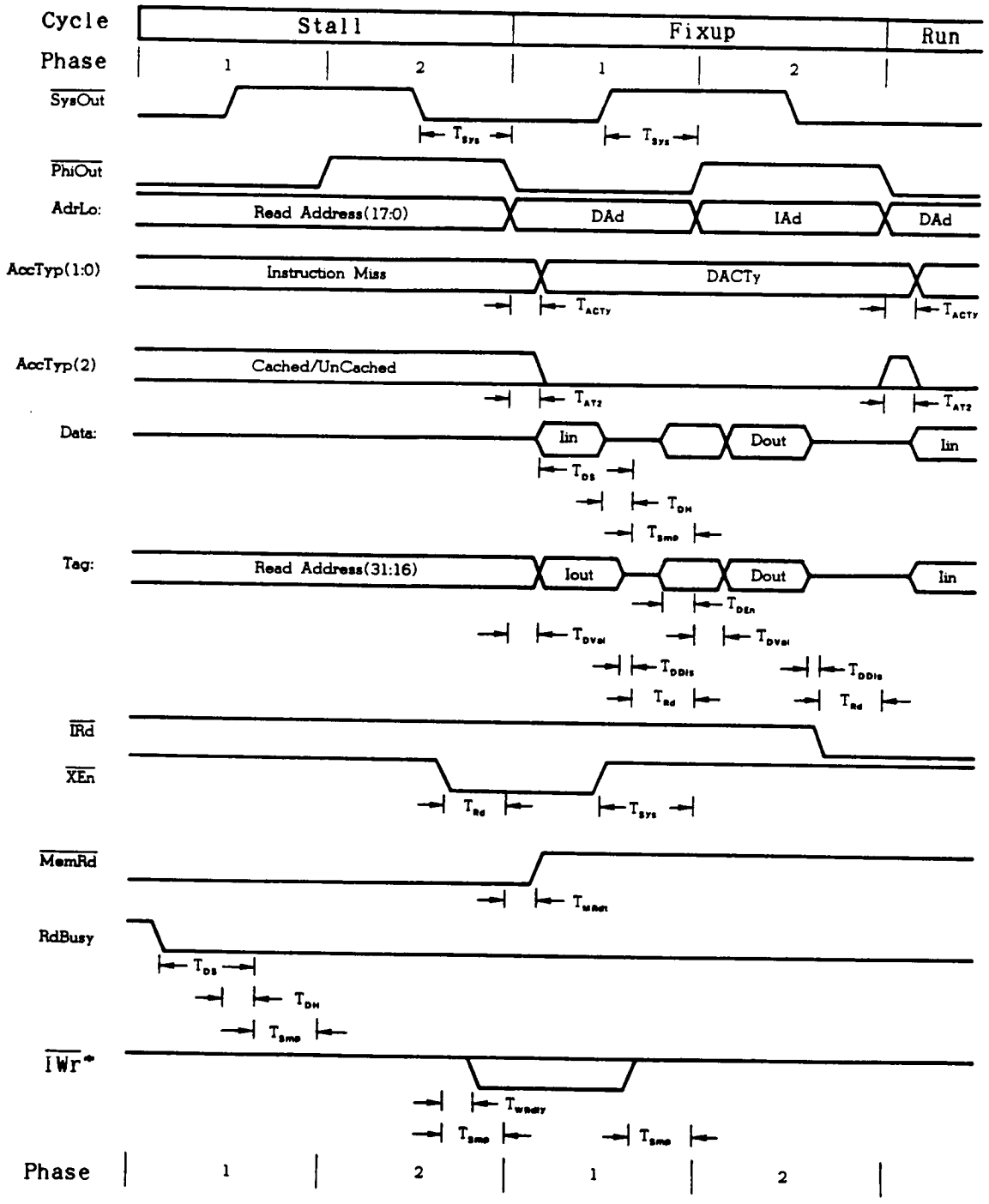


*: This signal becomes active in a cached area. In a uncached area, this signal does not become active.

Single Word Instruction Transfer - Beginning of Stall

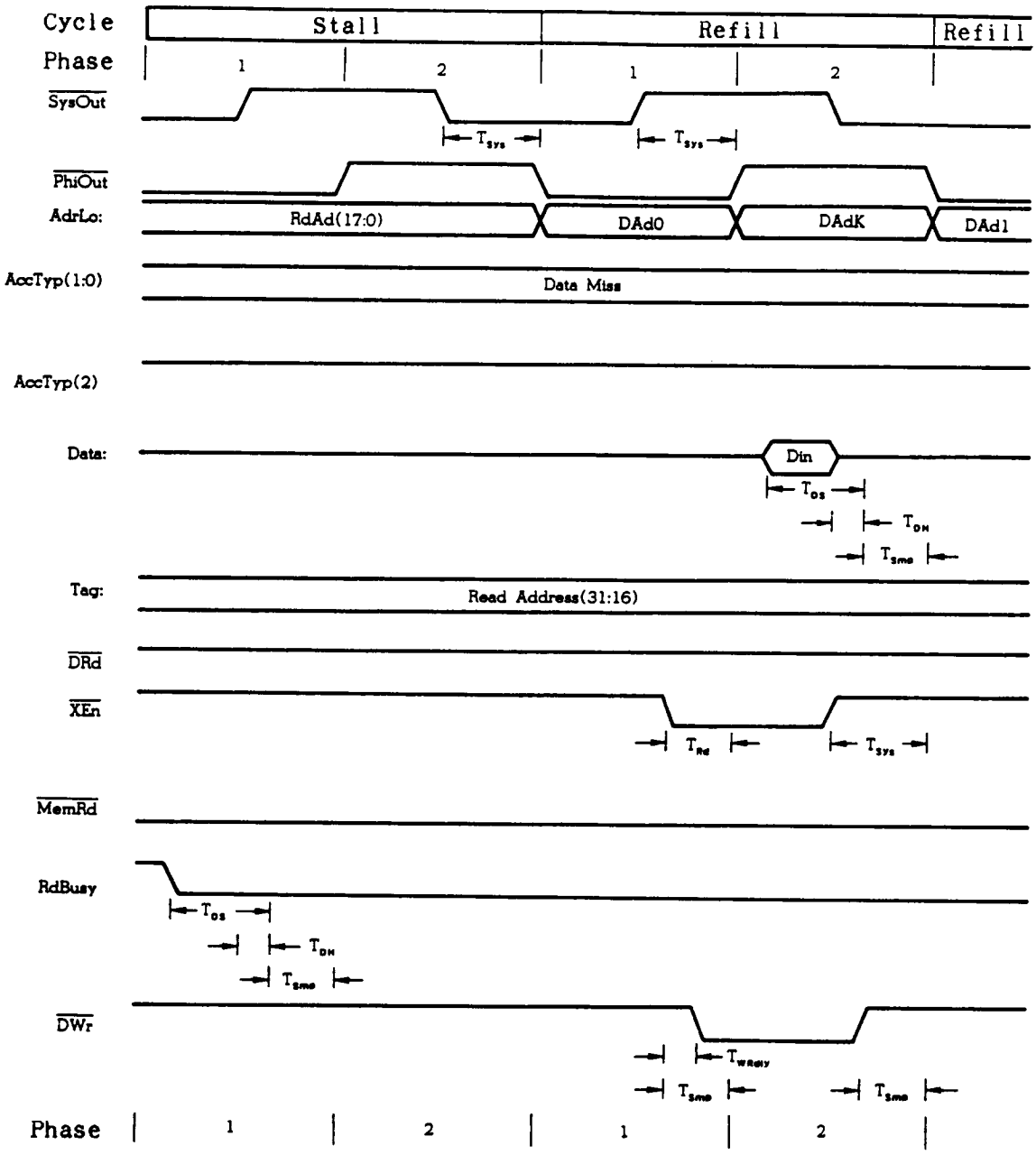


Single Word Instruction Transfer - End of Stall

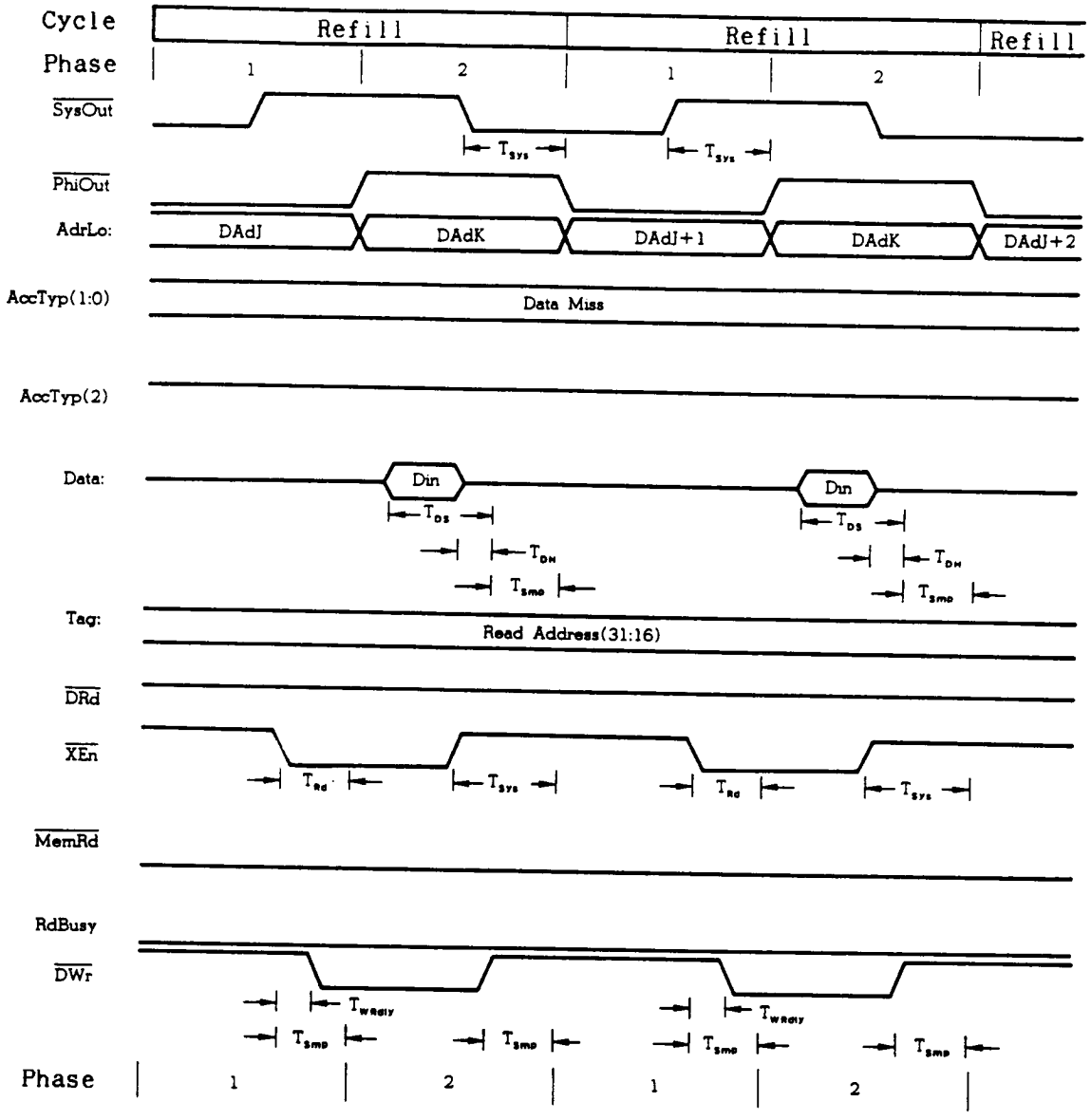


*: This signal becomes active in a cached area. In a uncached area, this signal does not become active.

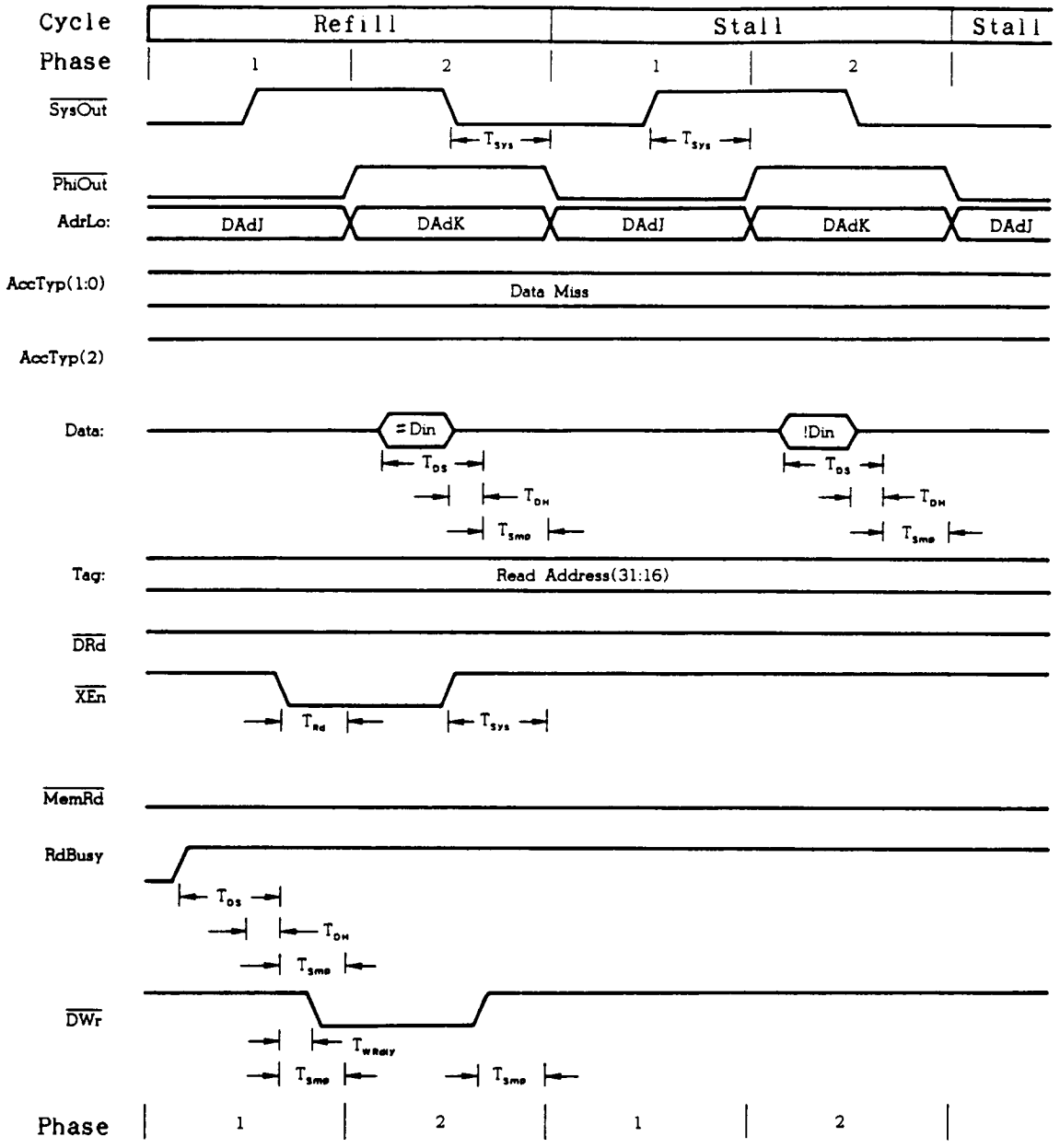
Data Block Transfer: Stall - Refill



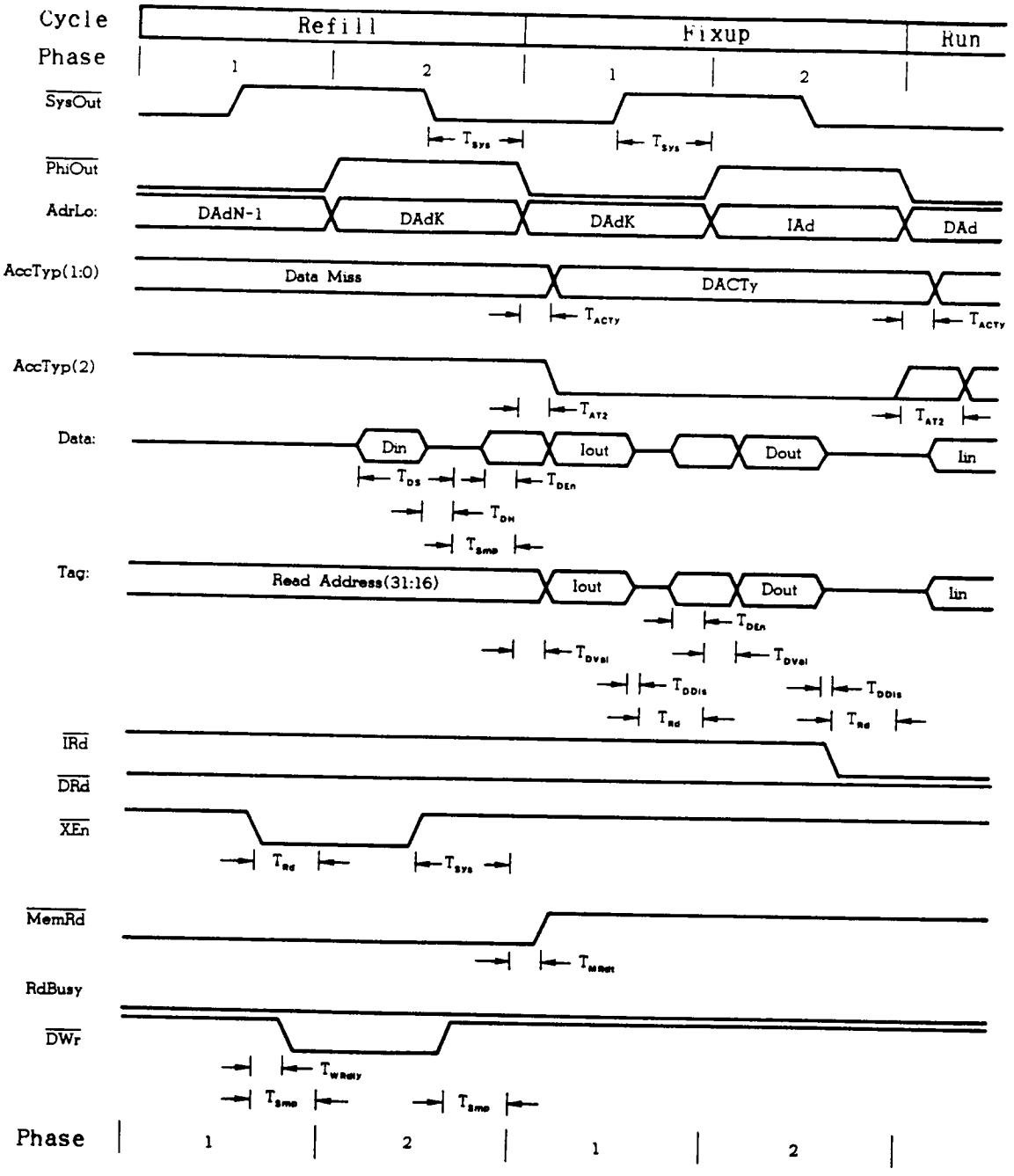
Data Block Transfer: Refill - Refill



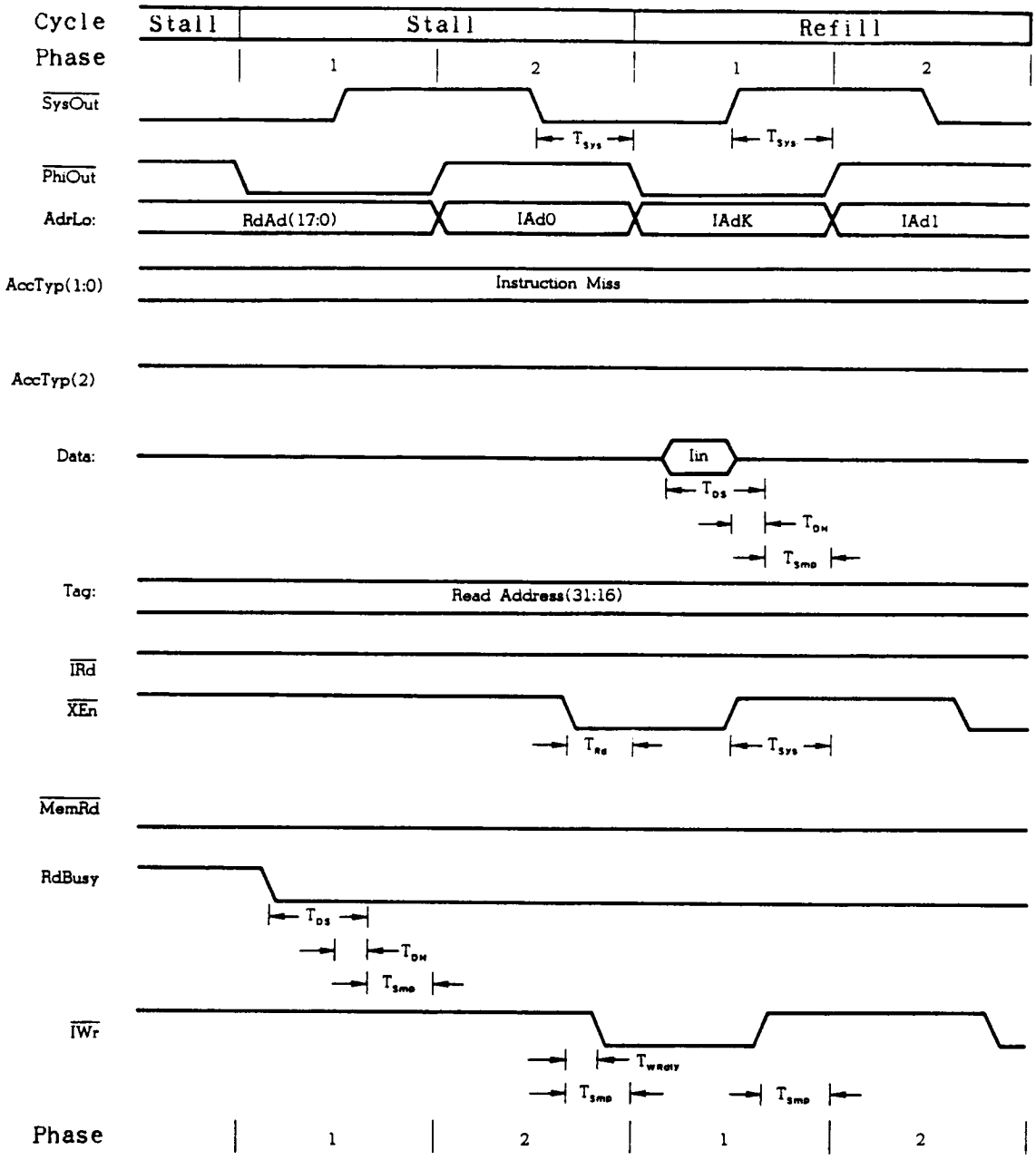
Data Block Transfer: Refill - Stall



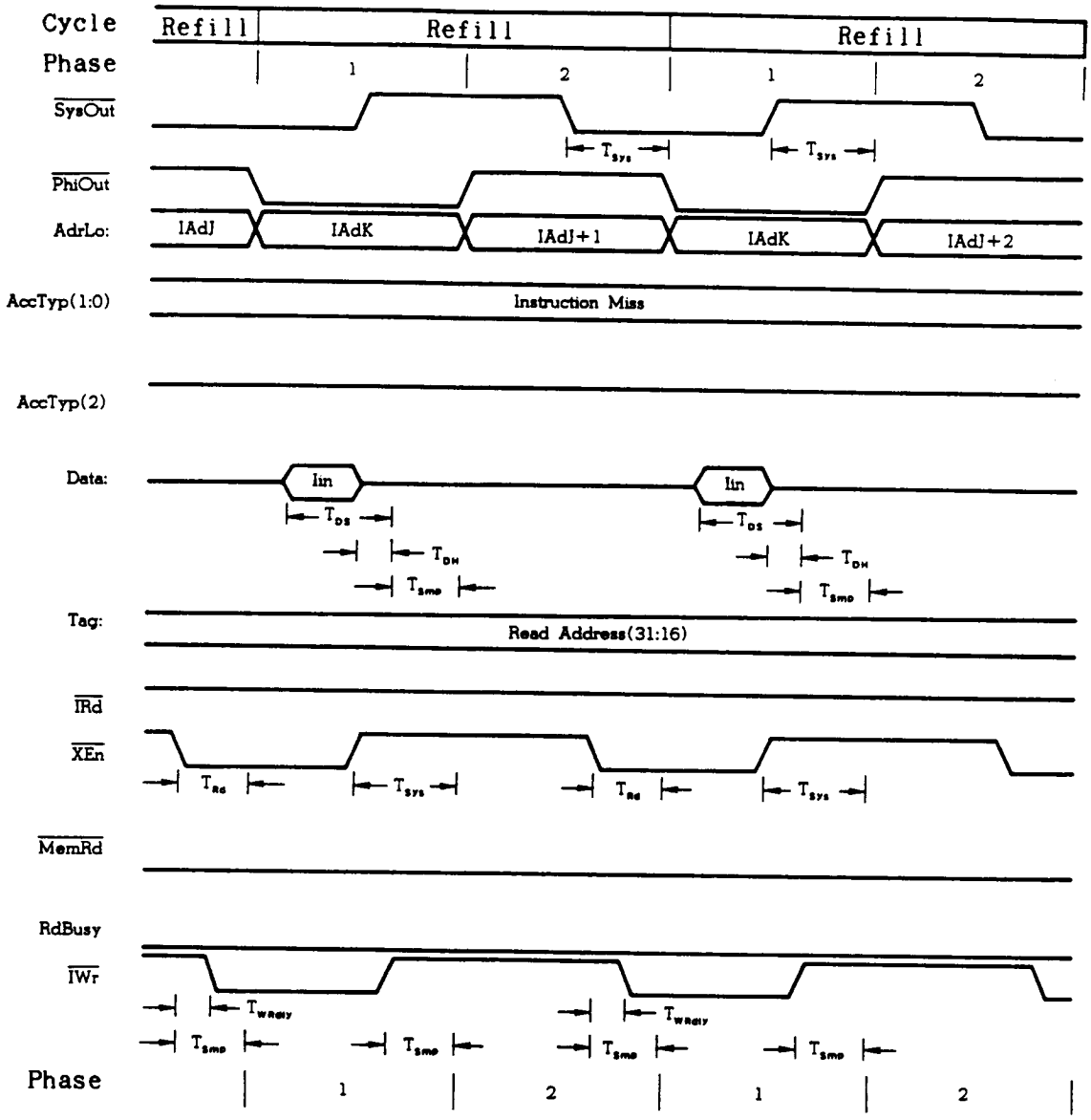
Data Block Transfer: Refill - Fixup



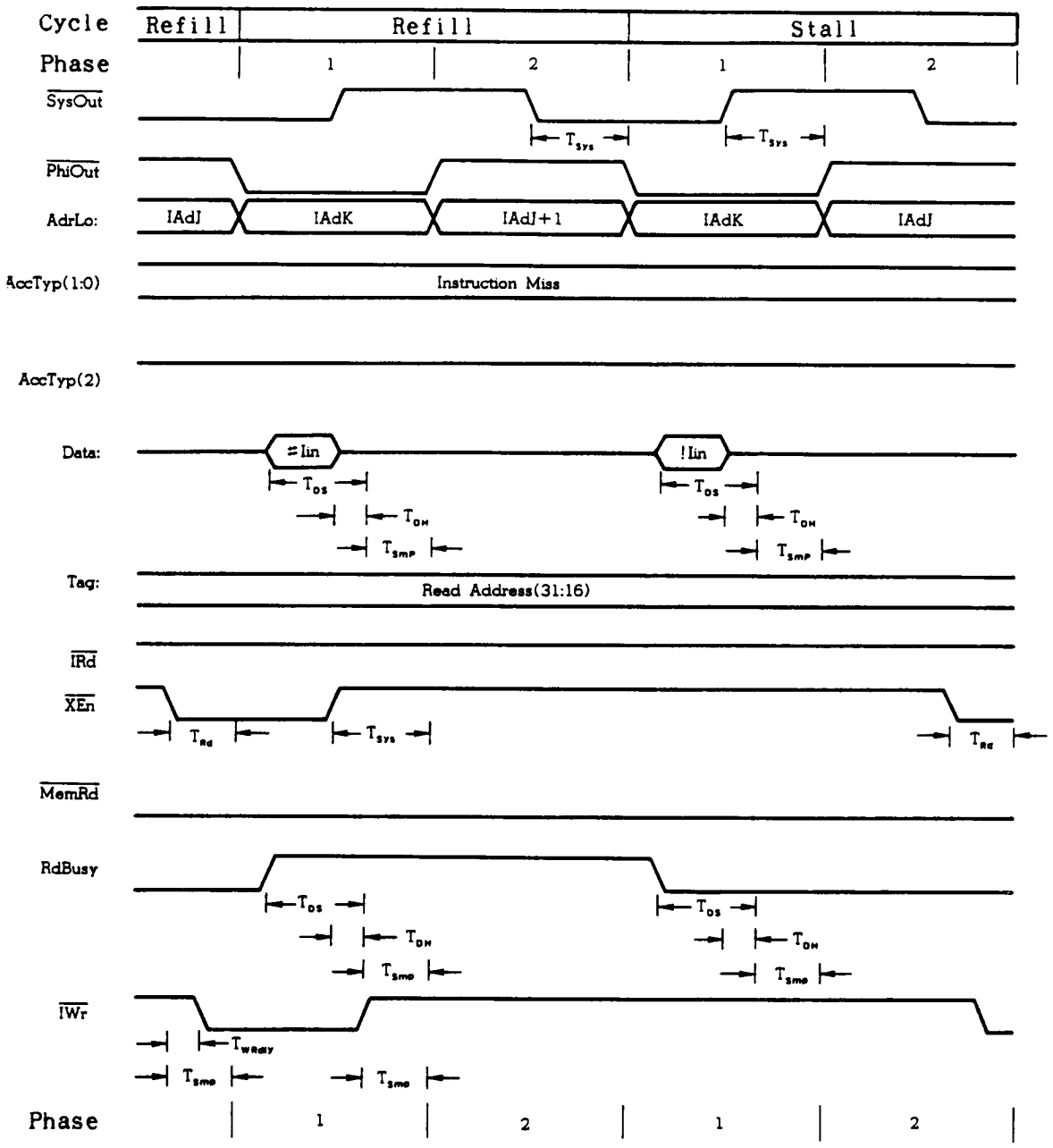
Instruction Block Transfer: Stall - Refill



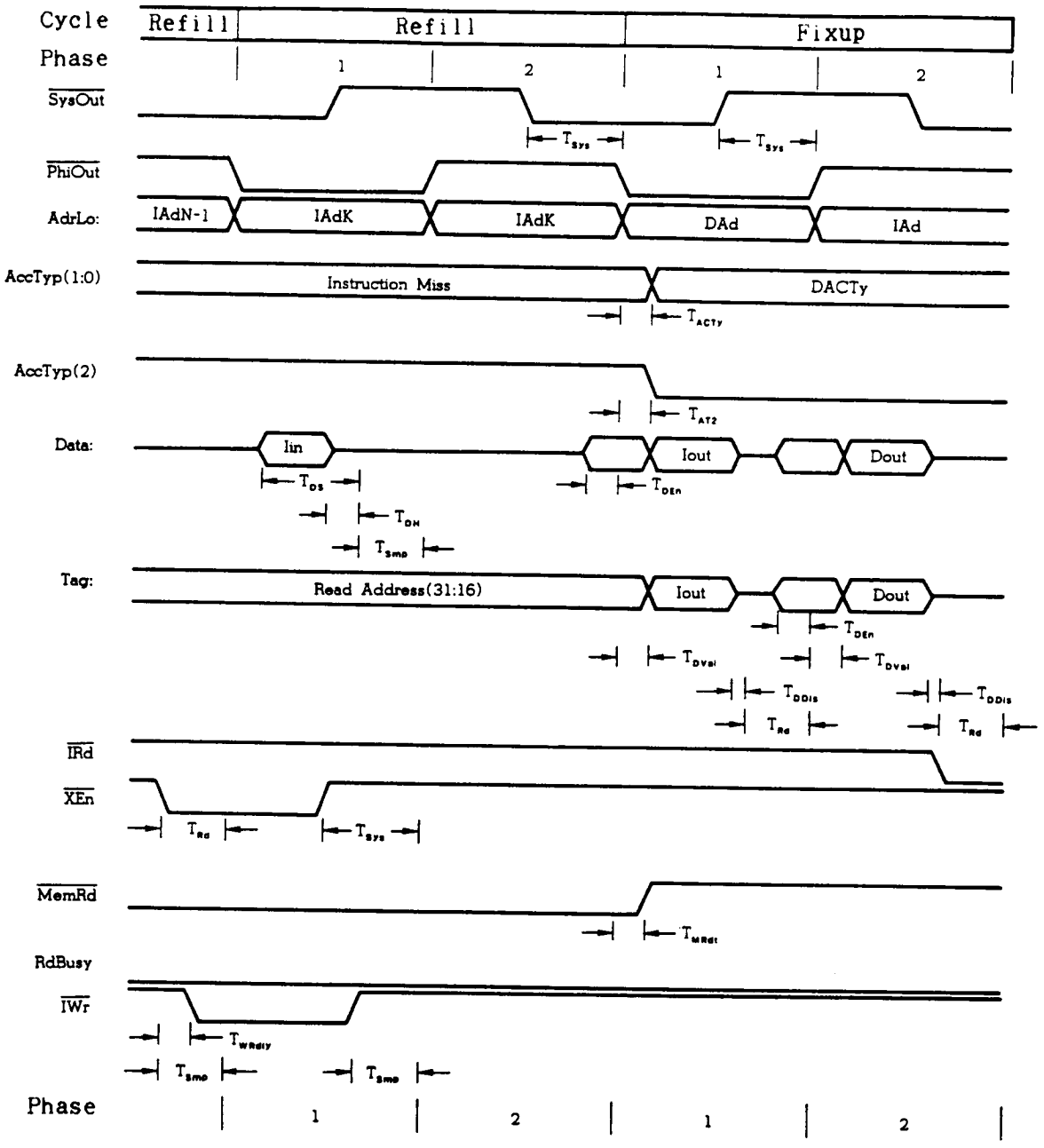
Instruction Block Transfer: Refill - Refill



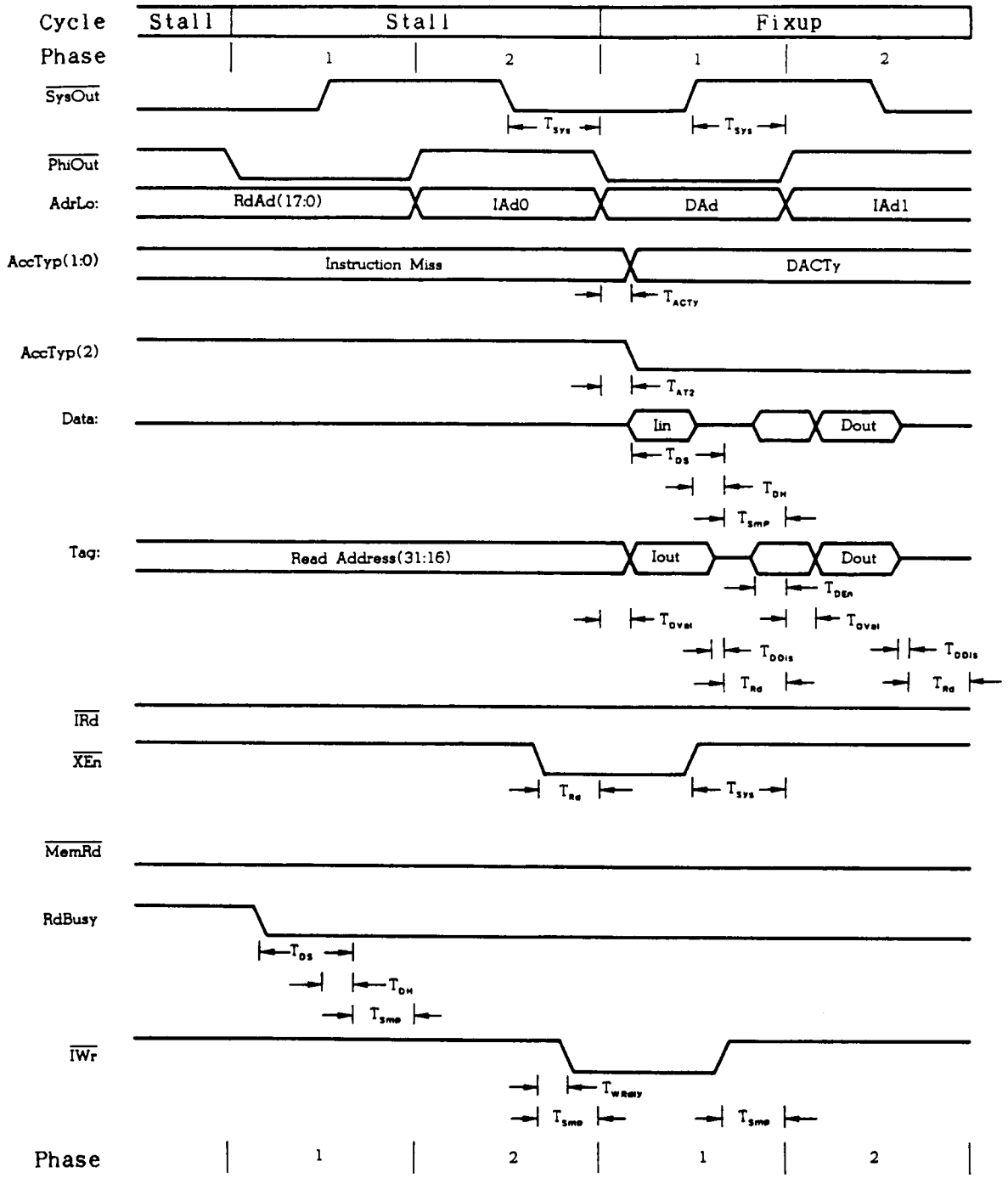
Instruction Block Transfer: Refill - Stall



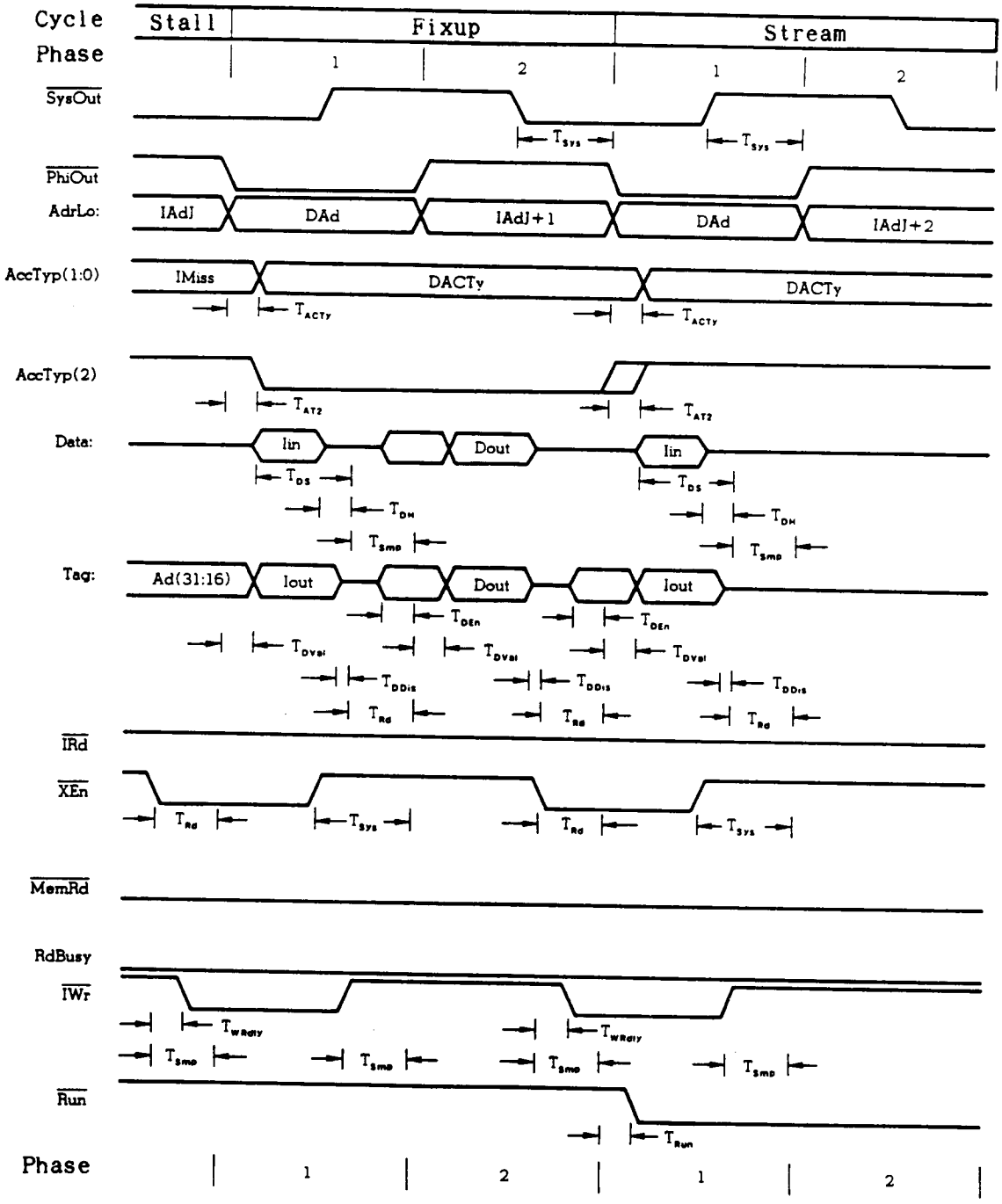
Instruction Block Transfer: Refill - Fixup



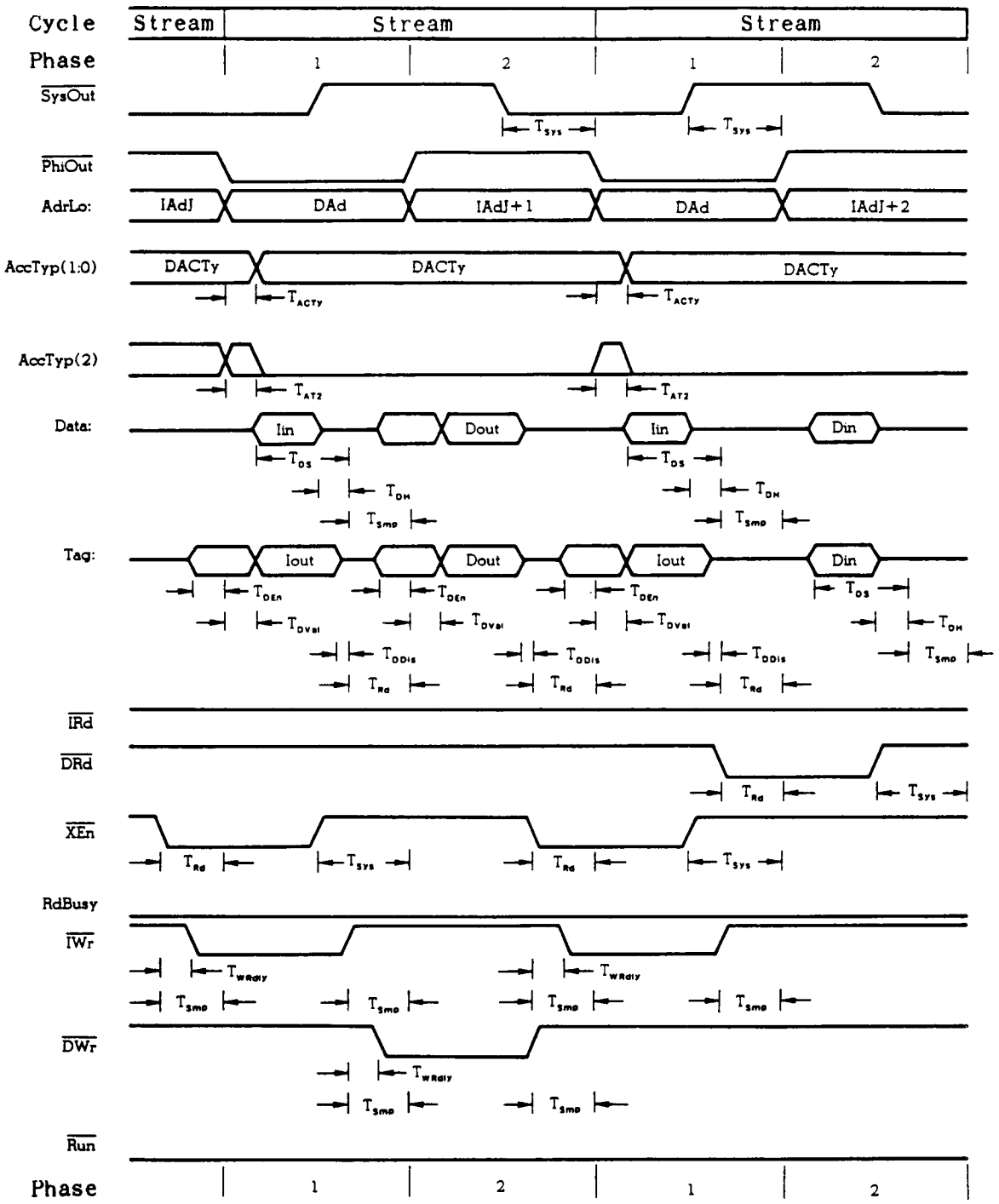
Instruction Stream: Stall - Fixup



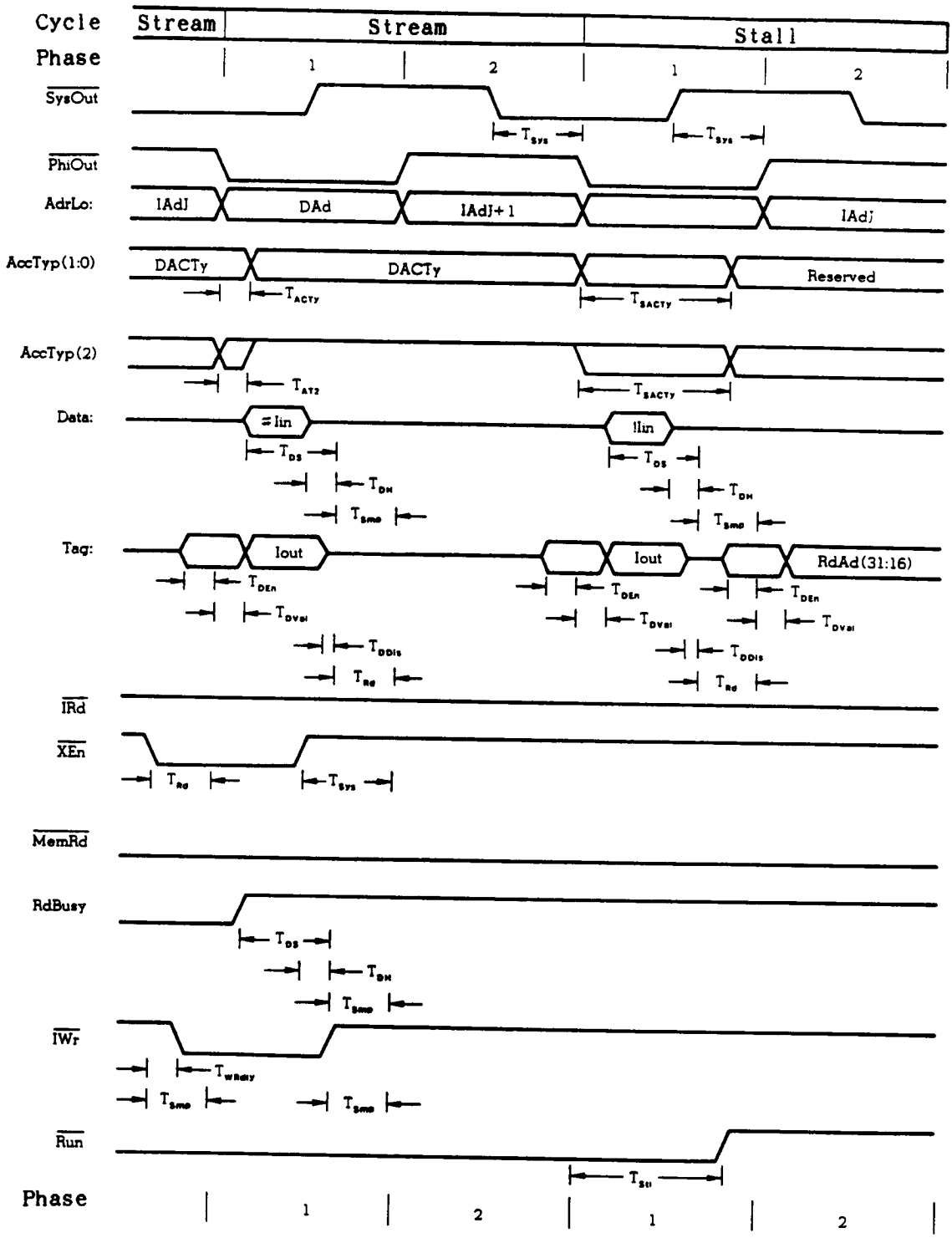
Instruction Stream: Fixup - Stream



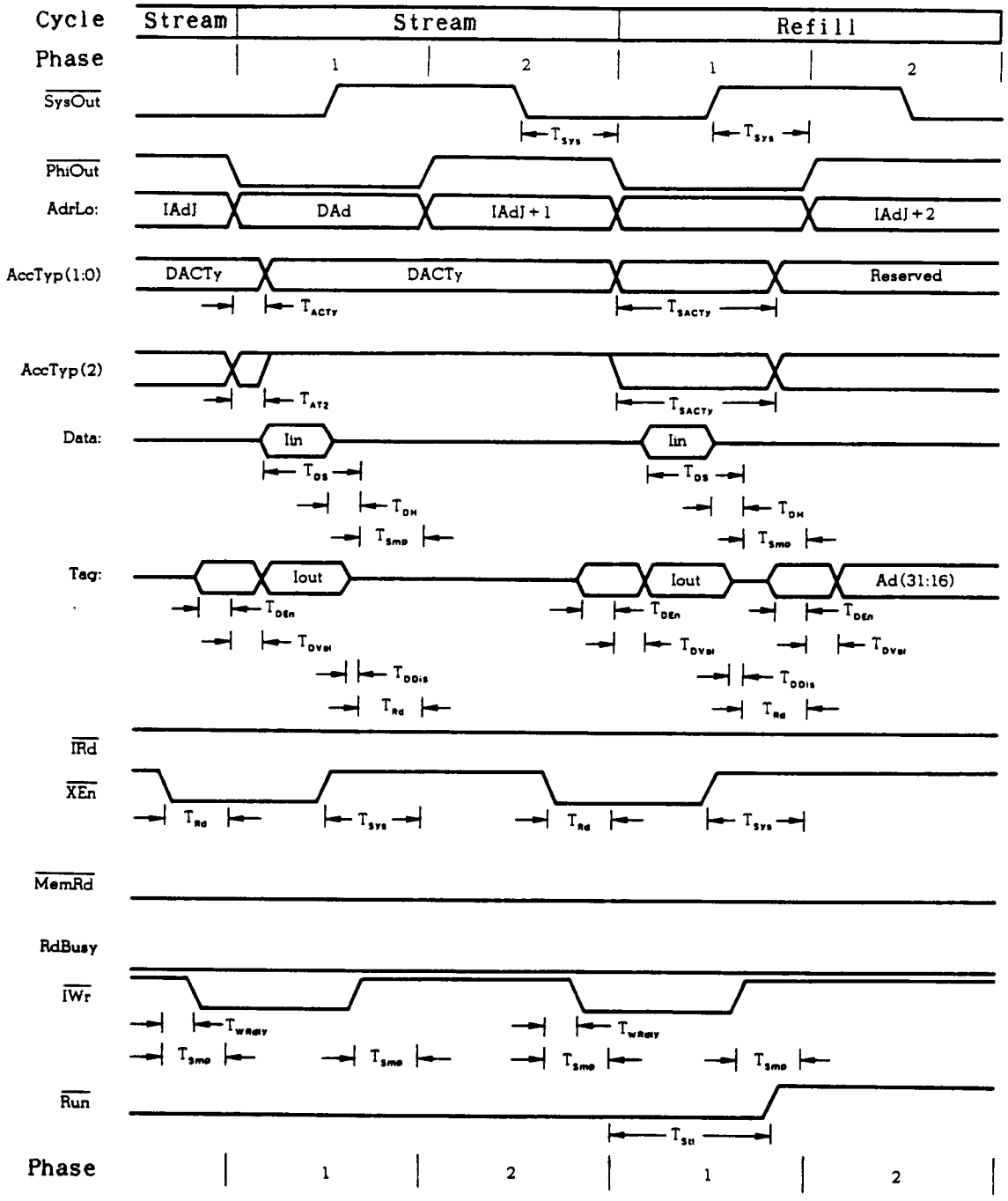
Instruction Stream: Stream - Stream



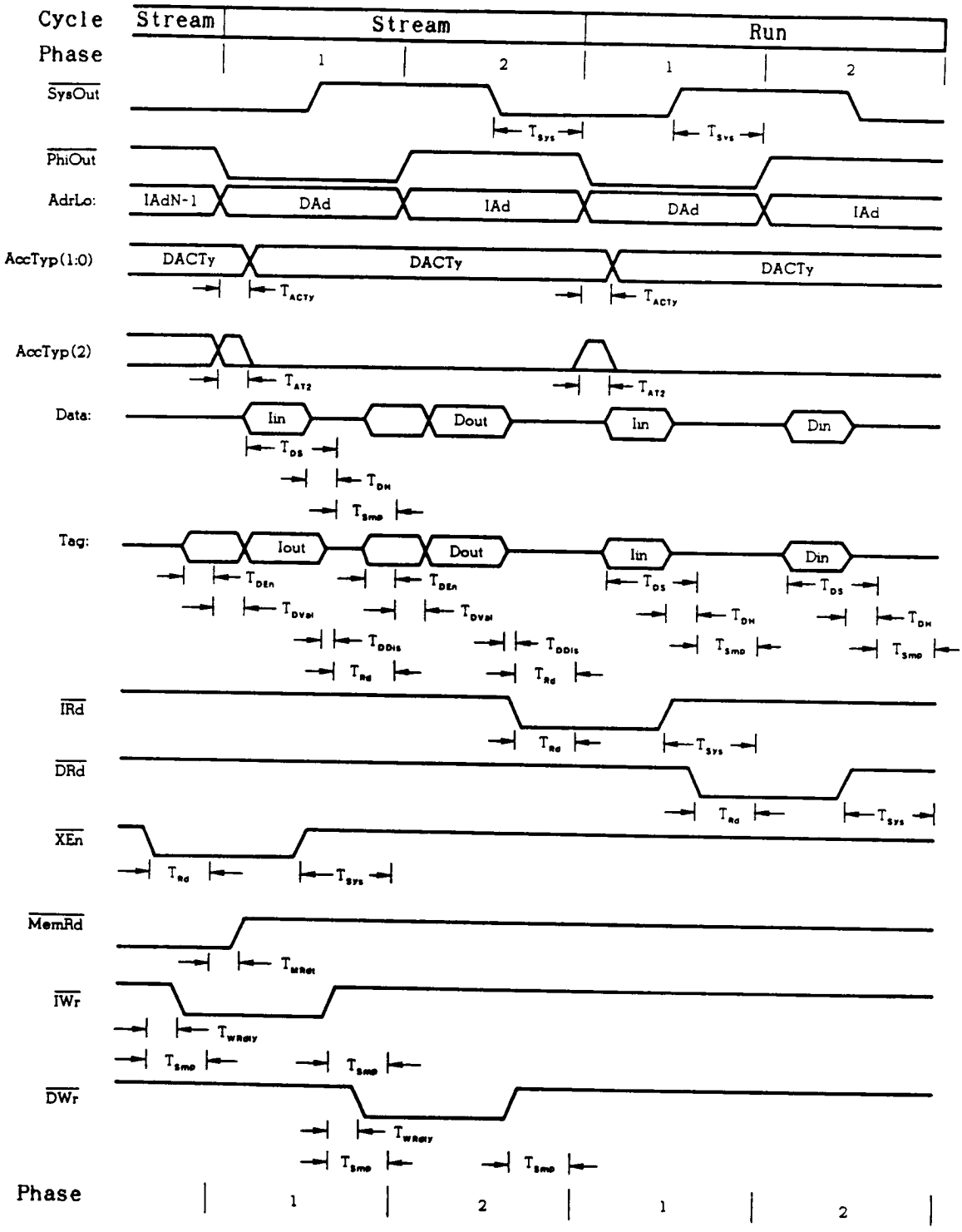
Instruction Stream: Stream - Stall



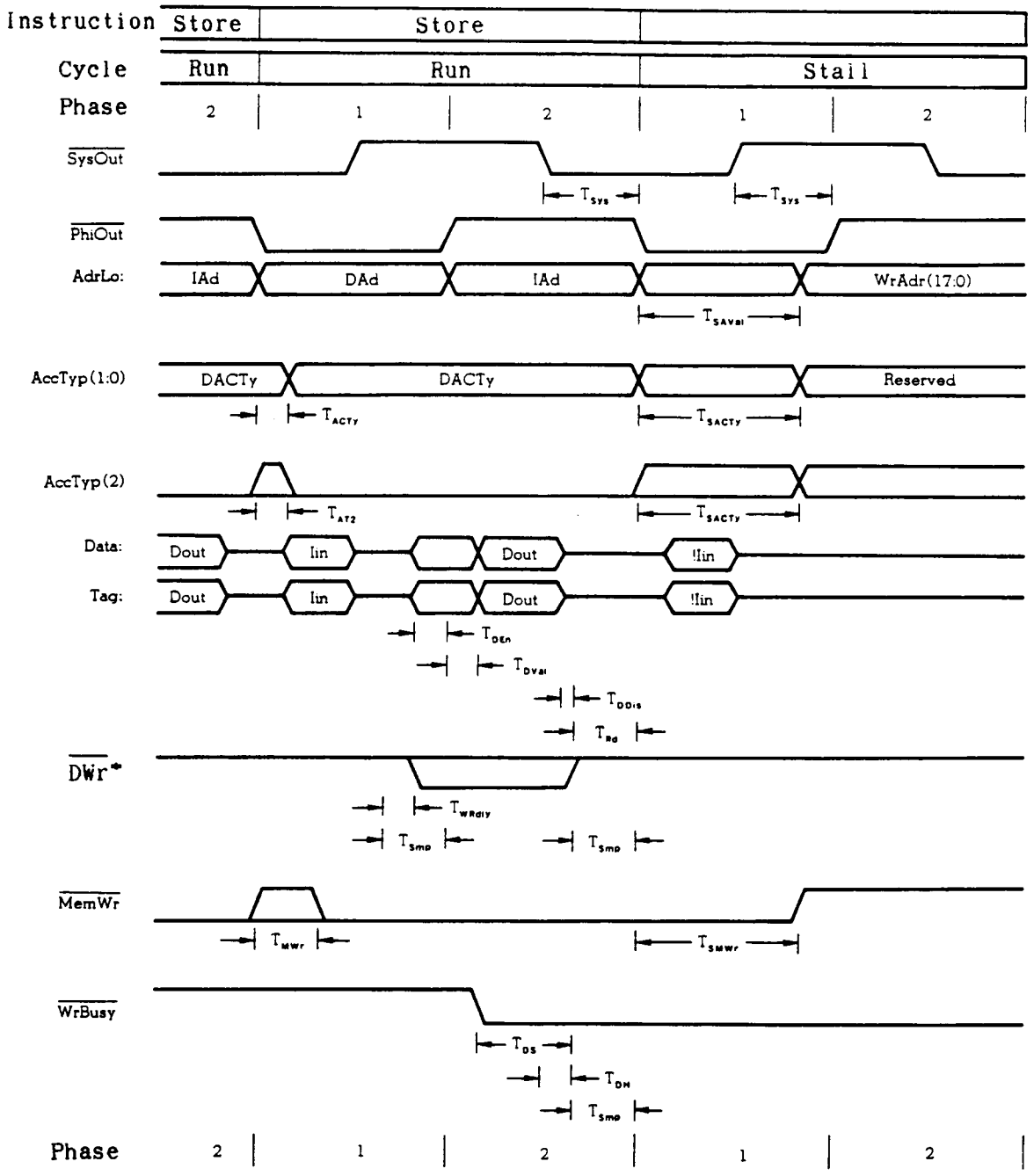
Instruction Stream: Stream - Refill



Instruction Stream: Stream - Run

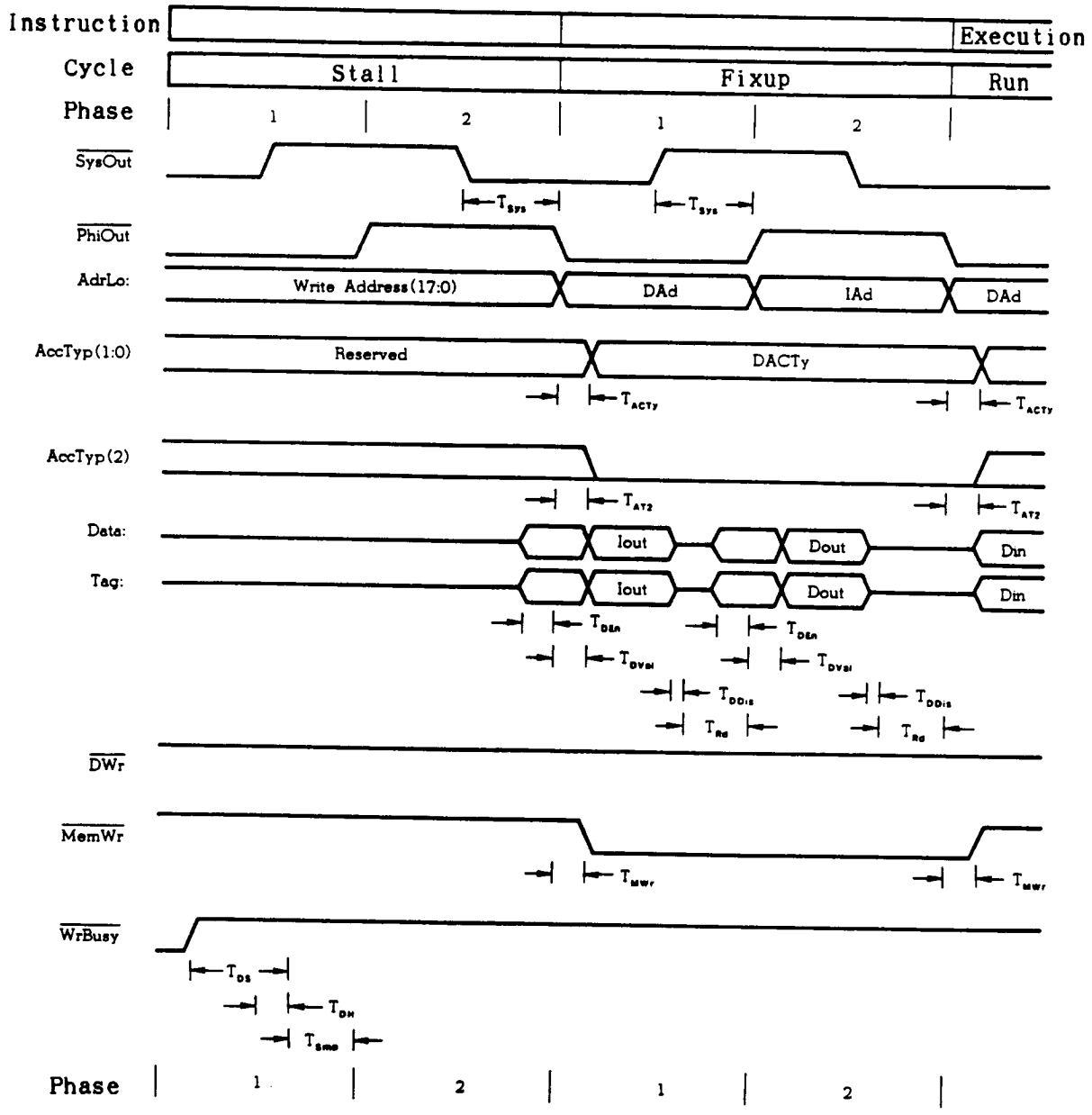


Write Timing: Run - Stall

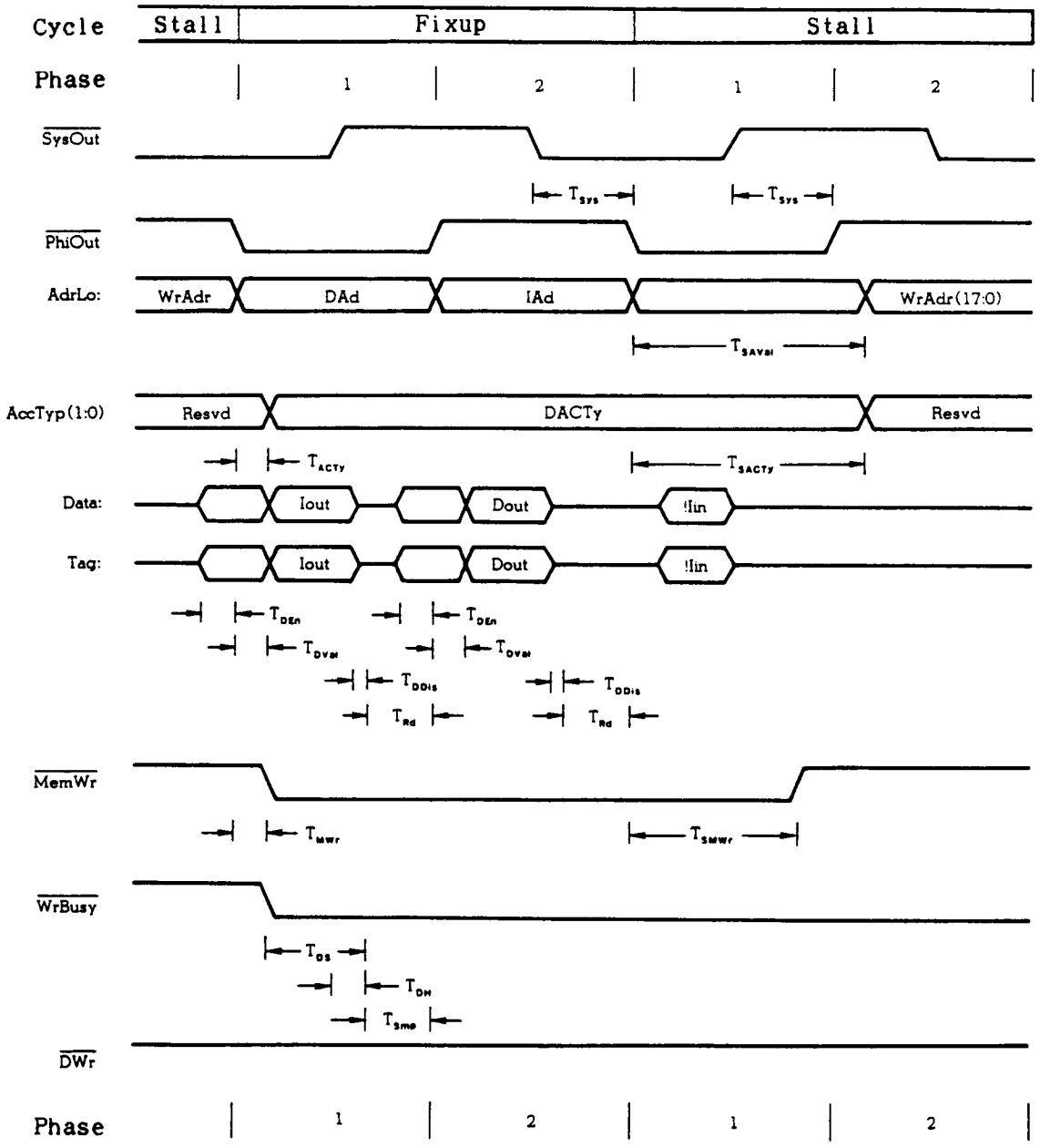


*: This signal becomes active in a cached area. In a uncached area, this signal does not become active.

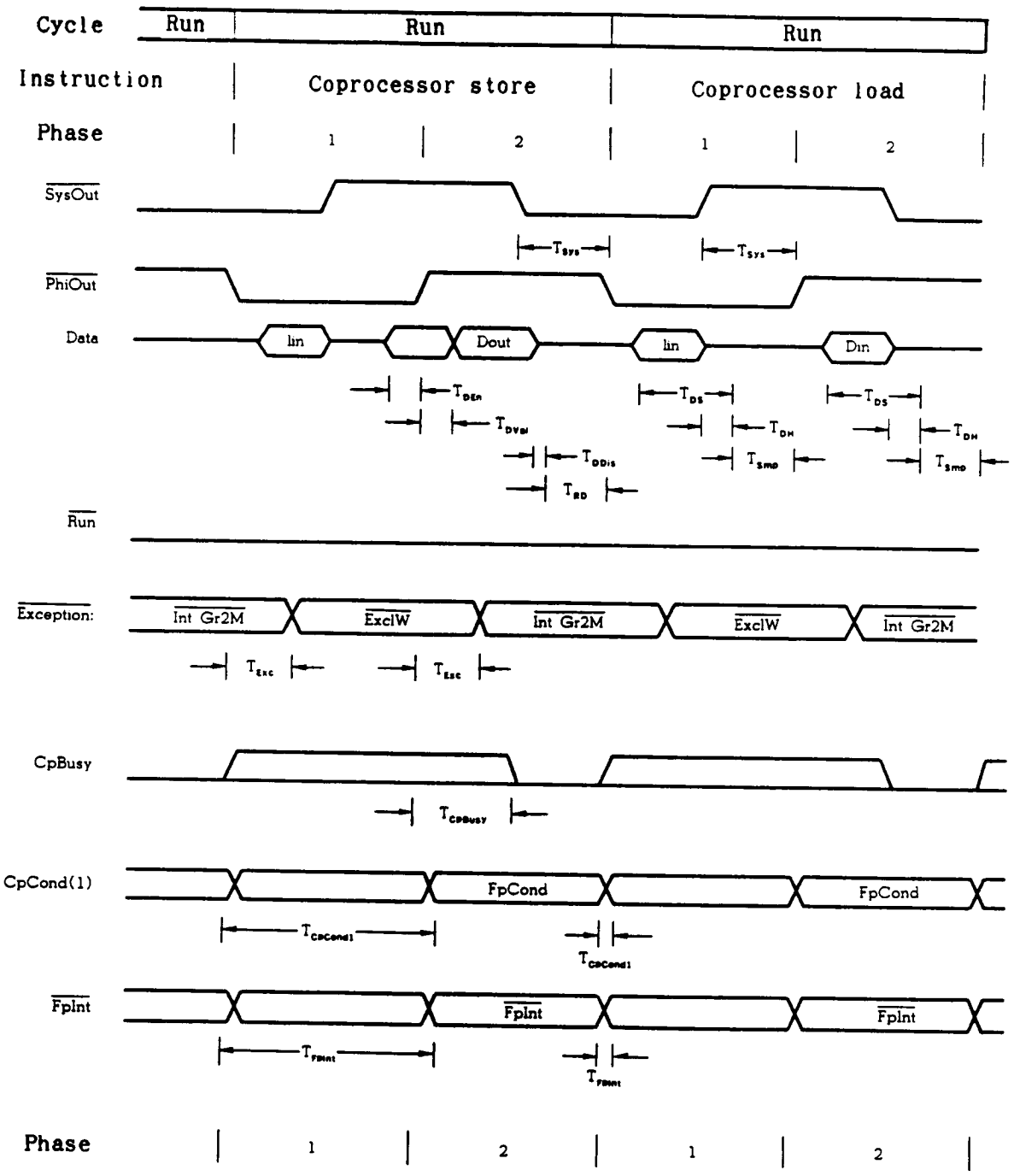
Write Timing: Stall - Fixup



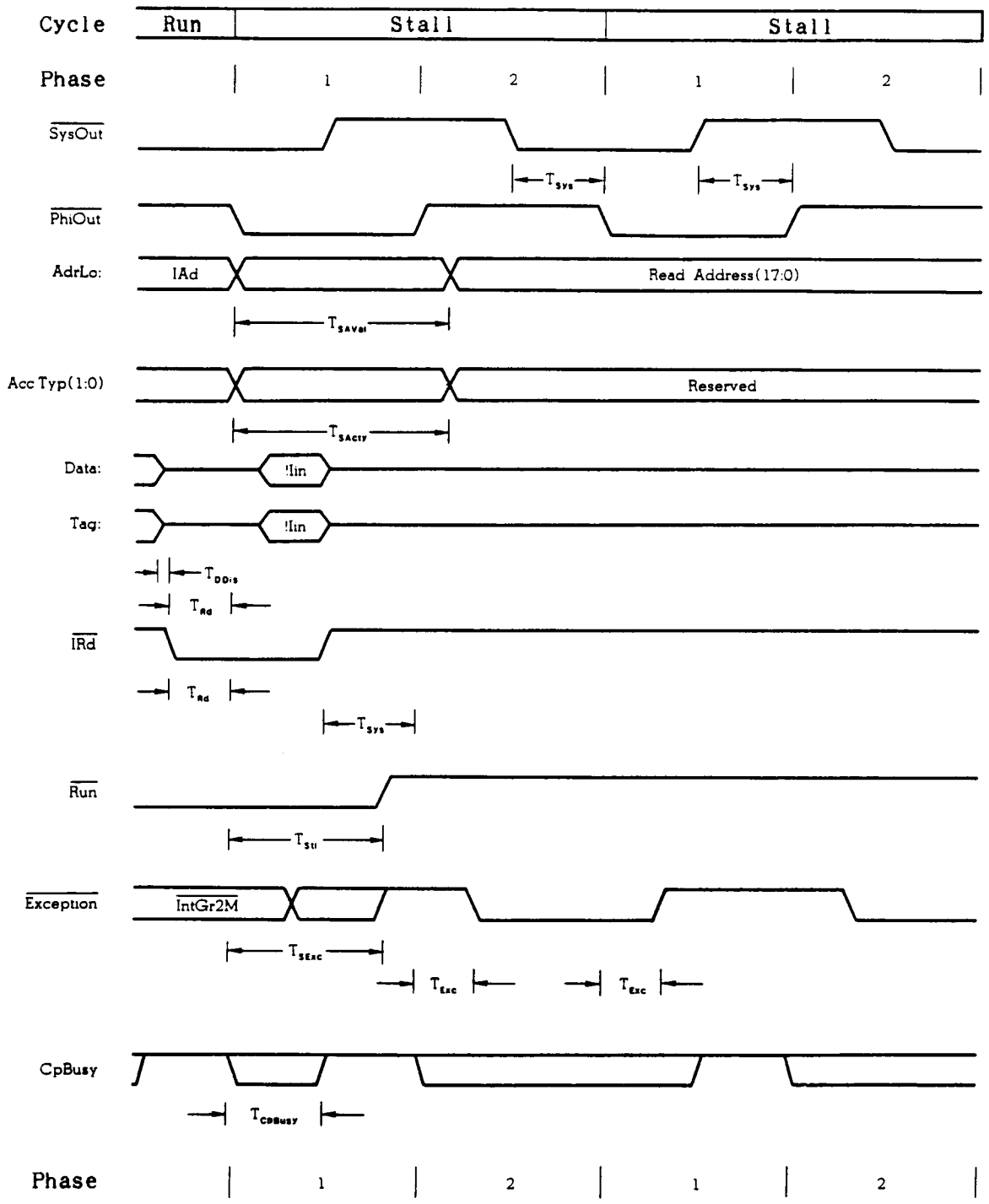
Write Busy Retry Timing: Fixup - Stall



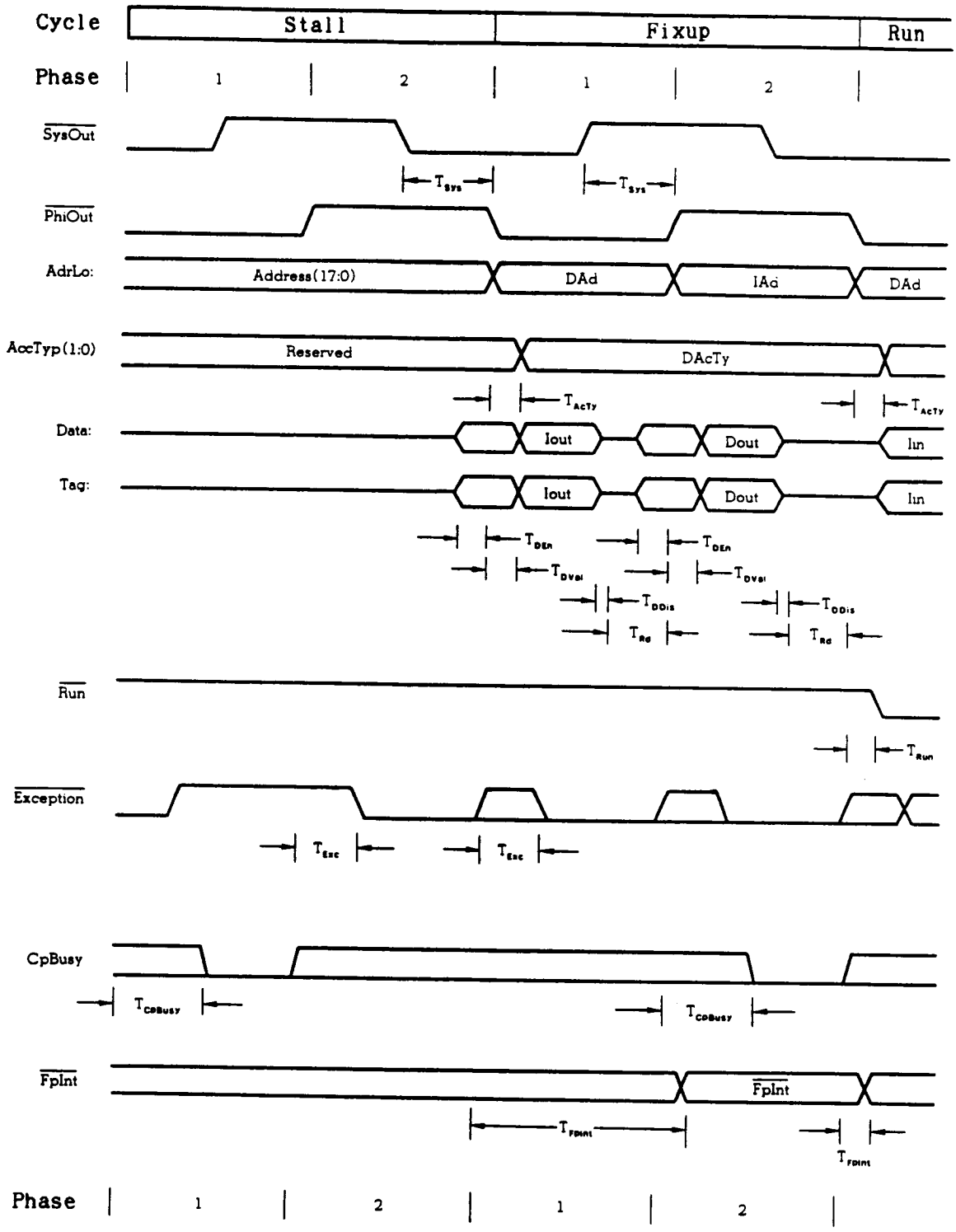
Coprocessor Interface Timing (Coprocessor Load/Store)



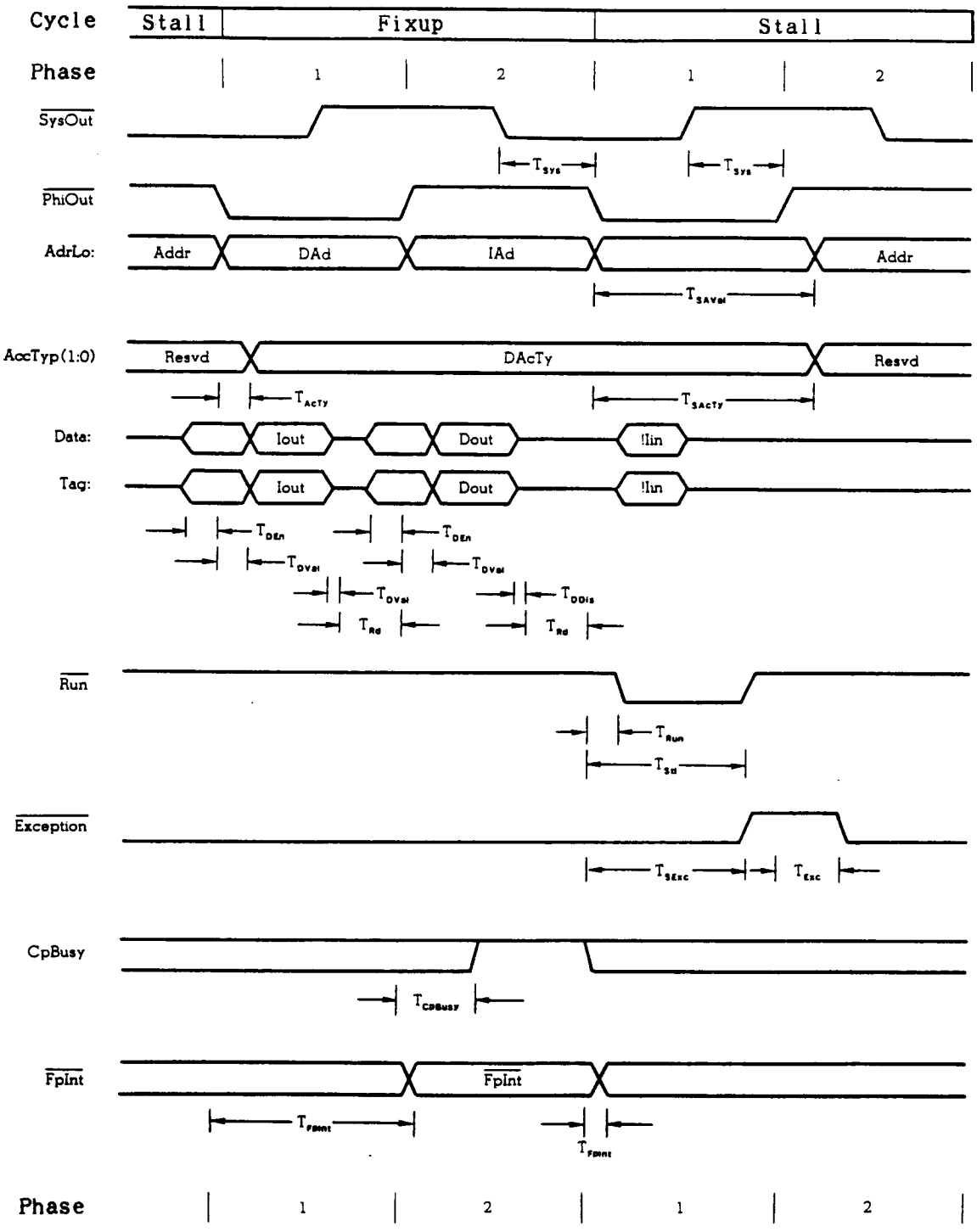
Coprocessor Busy Timing: Run - Stall



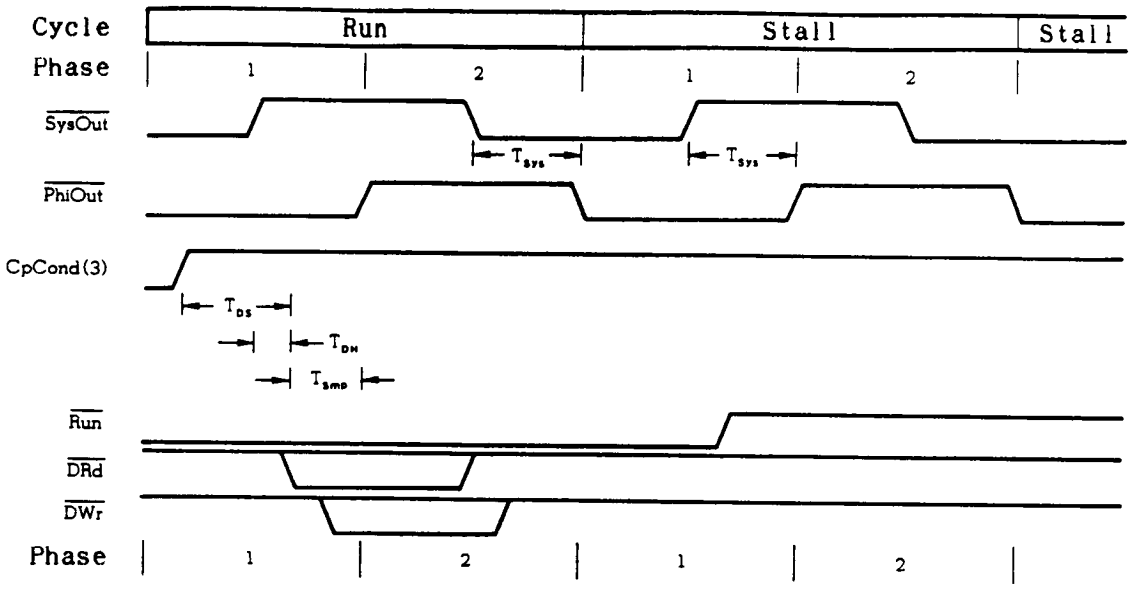
Coprocessor Busy Timing: Stall - Fixup



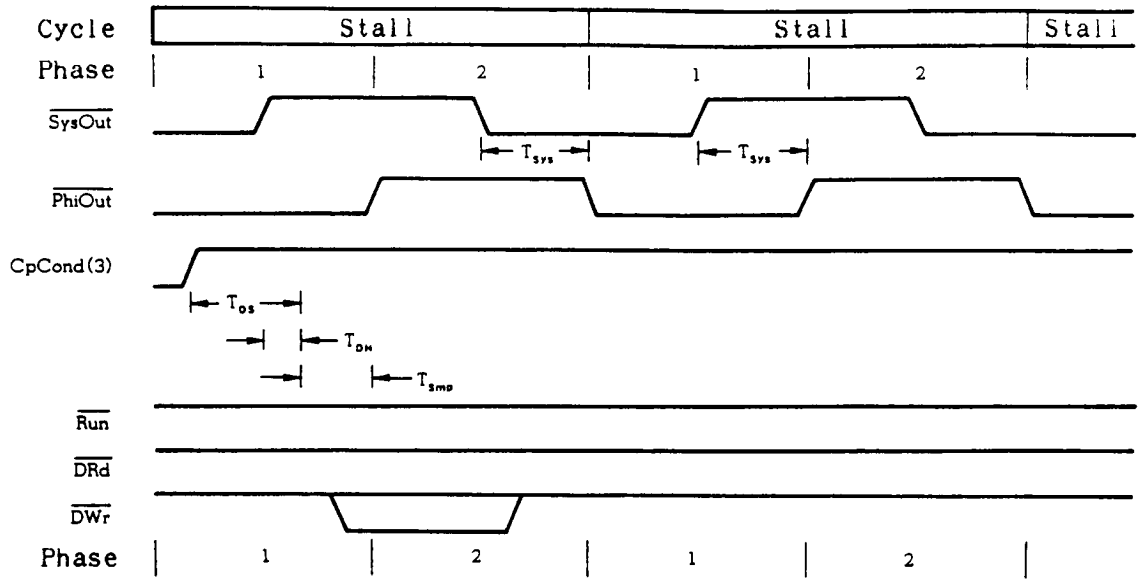
Coprocessor Busy Retry Timing: Fixup - Stall



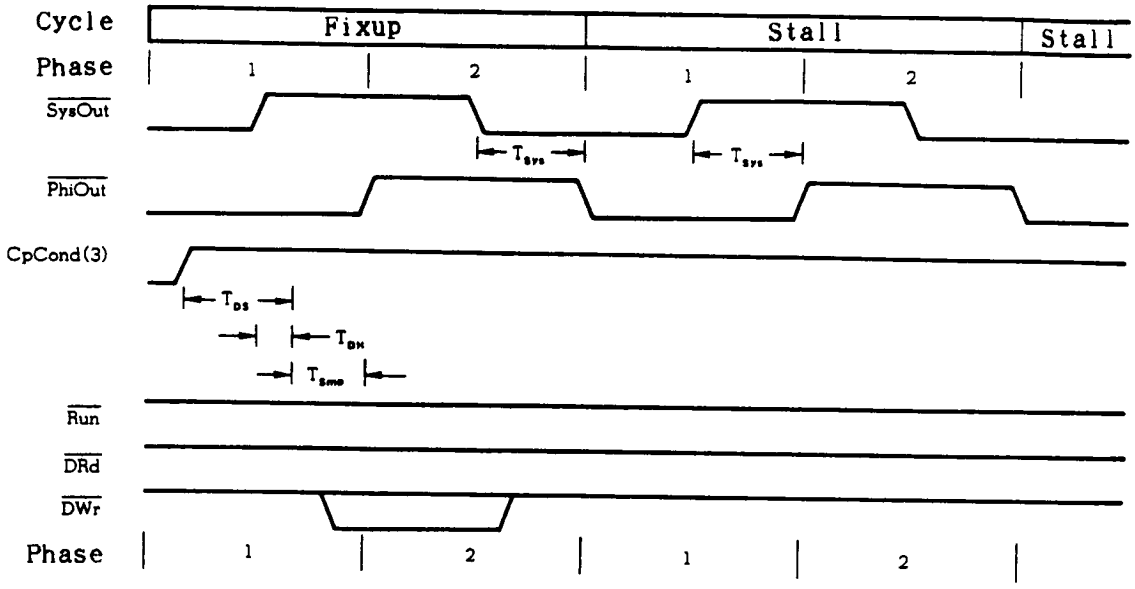
MP Stall Entering from Run



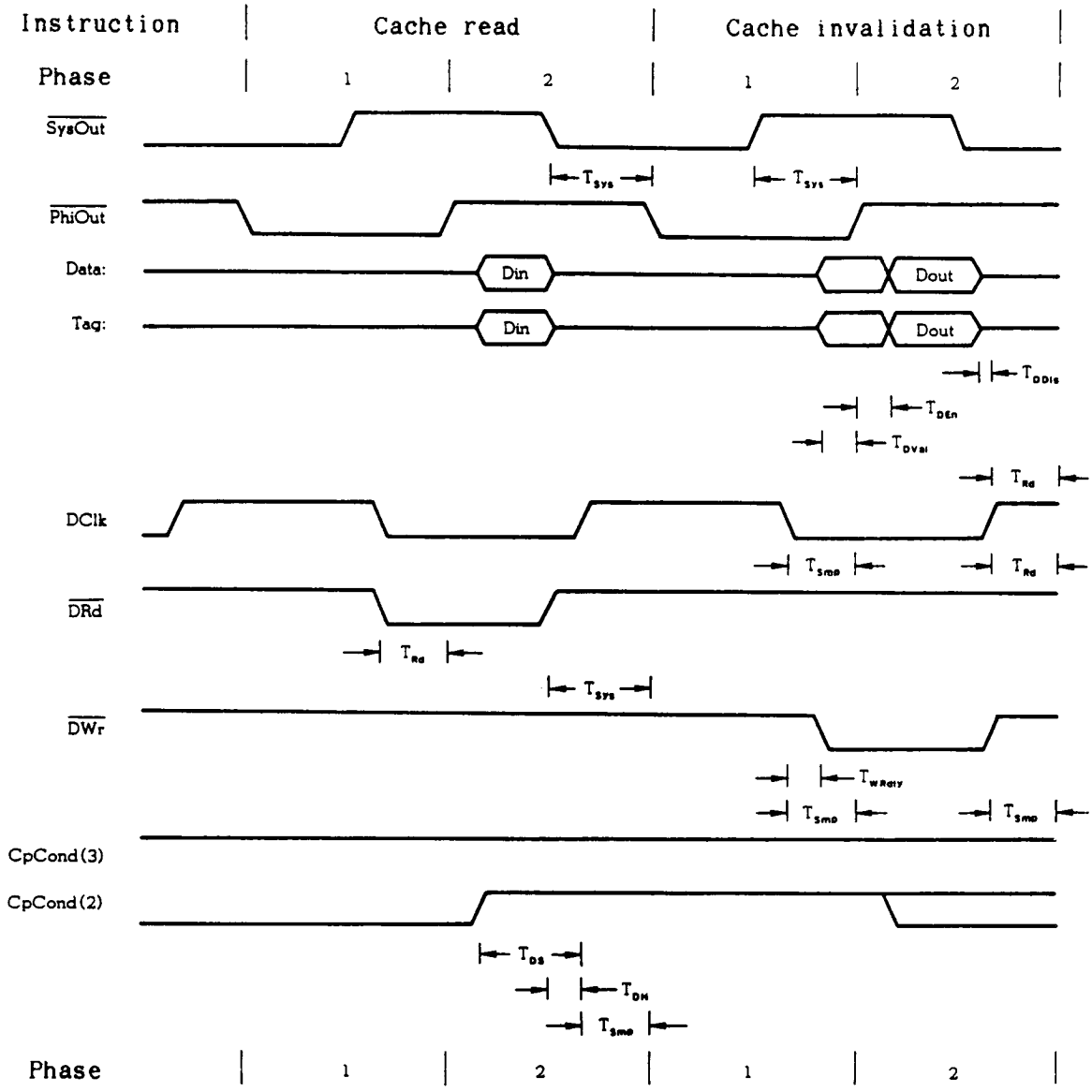
MP Stall Entering from Stall



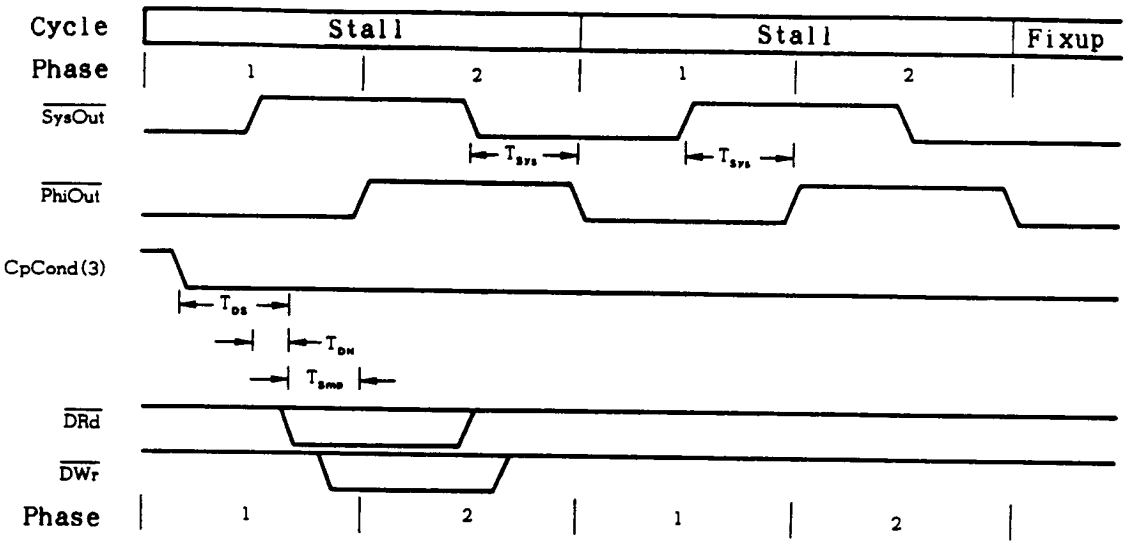
MP Stall Entering from Fixup



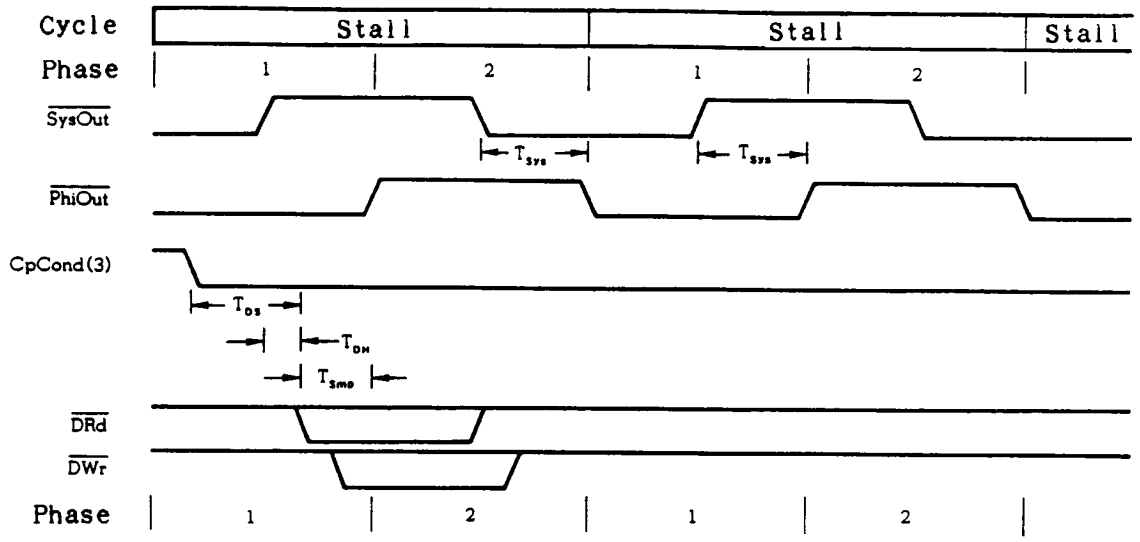
MP Stall Read and Invalidate Timing



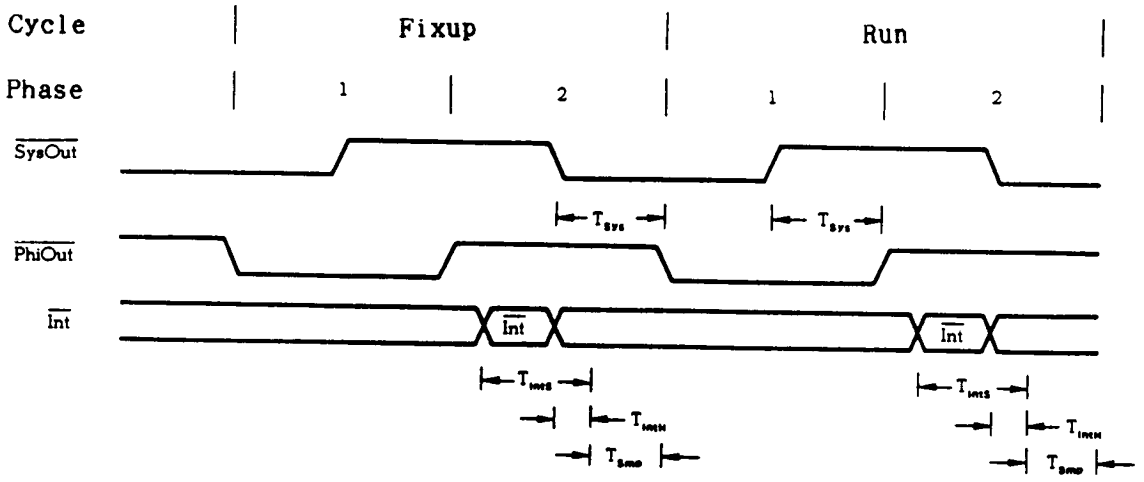
MP Stall Timing: MP Stall - Fixup



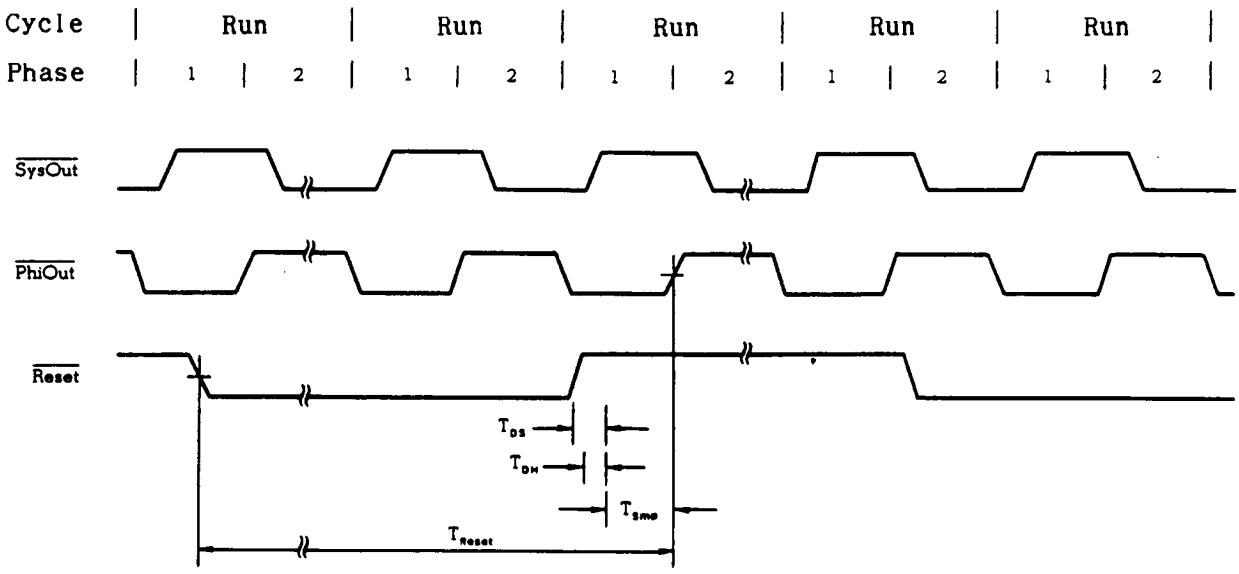
MP Stall Timing: MP Stall - Stall



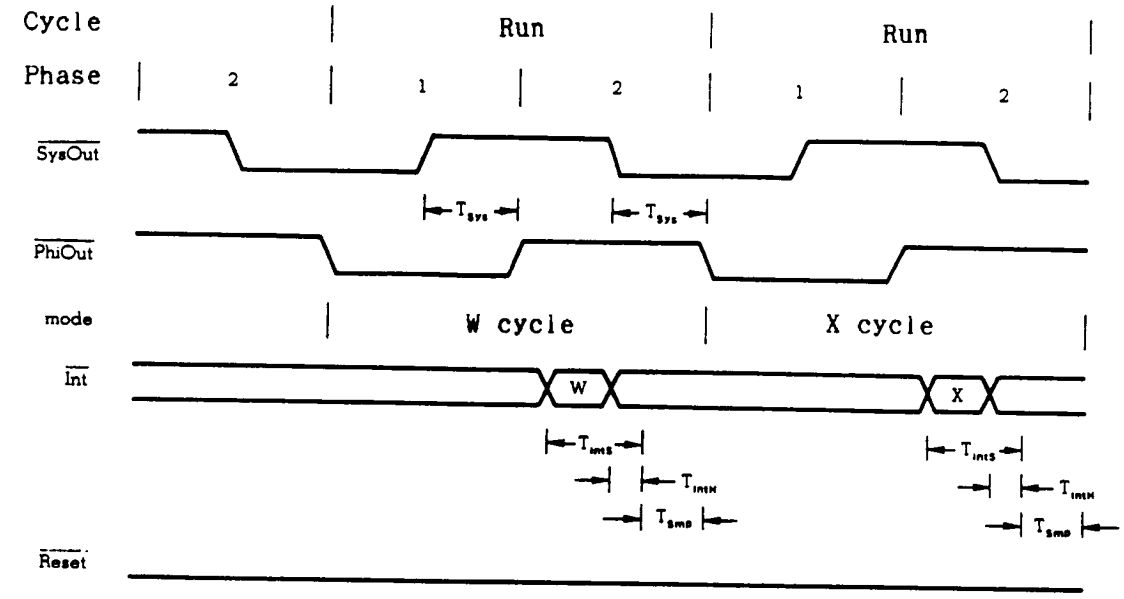
Interrupt Timing

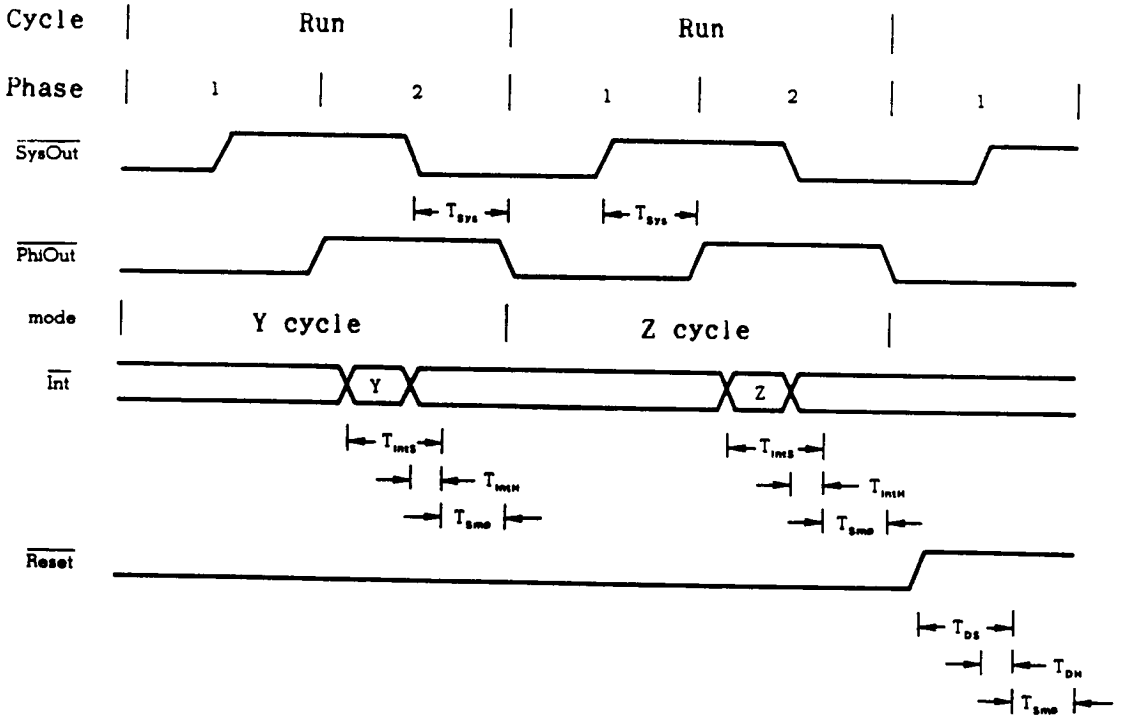


Reset Timing ($\overline{\text{Reset}}$ Input)



Reset Timing (Mode Selection)





Mode Setting Timing