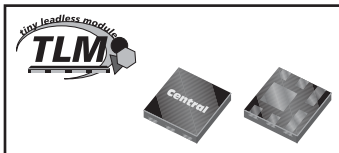
CTLDM7120-M563

SURFACE MOUNT
N-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET



Top View Bottom View

TLM563 CASE

• Device is ***Halogen Free*** by design

APPLICATIONS:

- Load Power Switches
- DC/DC Converters
- Battery powered devices including Cell Phones, PDAs, Digital Cameras, MP3 Players, etc.

Central Semiconductor Corp.

www.centralsemi.com

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLDM7120-M563 is a high quality, enhancement-mode N-channel MOSFET packaged in a space saving 1.6 x 1.6mm TLM™ surface mount package. This device is a TLM™ equivalent of the popular CMLDM7120G, SOT-563 device, featuring enhanced thermal characteristics, a package footprint compatible with standard SOT-563 mounting pad geometries, and a height profile of only 0.4mm.

MARKING CODE: CKN

FEATURES:

- ESD protection up to 2kV
- High Current (I_D=1.0A)
- Low $r_{DS(ON)}$ (0.14Ω MAX @ V_{GS}=2.5V, I_D=0.5A)
- Logic level compatibility
- High Thermal Efficiency
- TLM563 with a package profile of 0.4mm, compatible with SOT-563 mounting geometries

MAXIMUM RATINGS: (T_A=25°C)	**SYMBOL**		**UNITS**
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	8.0	V
Continuous Drain Current (Steady State)	I_D	1.0	A
Maximum Pulsed Drain Current, tp=10μs	I_{DM}	4.0	A
Power Dissipation (Note 1)	P_D	500	mW
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	°C
Thermal Resistance (Note 1)	Θ_{JA}	250	°C/W

ELECTRICAL CHARACTERISTICS: (T_A=25°C unless otherwise noted)

SYMBOL	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
I_{GSSF}, I_{GSSR}	V_{GS}=8.0V, V_{DS}=0			10	μA
I_{DSS}	V_{DS}=20V, V_{GS}=0			10	μA
BV_{DSS}	V_{GS}=0, I_D=250μA	20			V
$V_{GS(th)}$	V_{DS}=10V, I_D=1.0mA	0.5		1.2	V
V_{SD}	V_{GS}=0, I_S=1.0A			1.1	V
$r_{DS(ON)}$	V_{GS}=4.5V, I_D=500mA		0.075	0.10	Ω
$r_{DS(ON)}$	V_{GS}=2.5V, I_D=500mA		0.10	0.14	Ω
$r_{DS(ON)}$	V_{GS}=1.5V, I_D=100mA		0.20	0.25	Ω
g_{FS}	V_{DS}=10V, I_D=500mA		2.5		S
C_{rss}	V_{DS}=10V, V_{GS}=0, f=1.0MHz		45		pF
C_{iss}	V_{DS}=10V, V_{GS}=0, f=1.0MHz		220		pF
C_{oss}	V_{DS}=10V, V_{GS}=0, f=1.0MHz		120		pF
t_{on}	V_{DD}=10V, V_{GS}=5.0V, I_D=500mA		25		ns
t_{off}	V_{DD}=10V, V_{GS}=5.0V, I_D=500mA		140		ns

Notes: (1) Mounted on 2 inch square FR4 PCB with copper mounting pad area of 2.4mm^2.

R2 (17-February 2010)

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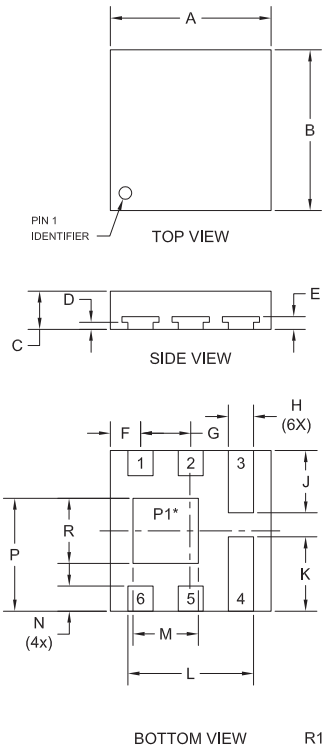
TLM563 CASE - MECHANICAL OUTLINE

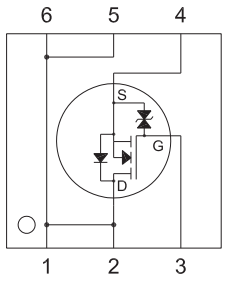


* Exposed pad P1 common to pins 1, 2, 5, and 6.

DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.062	0.064	1.57	1.63
B	0.062	0.064	1.57	1.63
C	0.014	0.017	0.36	0.43
D	0.002	0.004	0.04	0.10
E	0.004	0.006	0.10	0.16
F	0.011	0.013	0.27	0.33
G	0.019	0.021	0.47	0.53
H	0.009	0.011	0.22	0.28
J	0.023	0.026	0.59	0.65
K	0.028	0.030	0.71	0.77
L	0.048	0.050	1.22	1.28
M	0.024	0.027	0.62	0.68
N	0.009	0.011	0.22	0.28
P	0.043	0.045	1.09	1.16
R	0.024	0.027	0.62	0.68

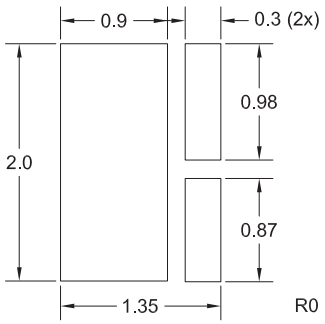
TLM563 (REV:R1)

PIN CONFIGURATION



SUGGESTED MOUNTING PADS

(Dimensions in mm)



LEAD CODE:
1) Drain
2) Drain
3) Gate
4) Source
5) Drain
6) Drain

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