

**CMOS Hex Buffer/Converters**

High-Voltage Types (20-Volt Rating)  
 CD4049UB—Inverting Type  
 CD4050B—Non-Inverting Type

■ CD4049UB and CD4050B are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply (voltage  $V_{CC}$ ). The input-signal high level ( $V_{IH}$ ) can exceed the  $V_{CC}$  supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads. ( $V_{CC}=5\text{ V}$ ,  $V_{OL} \leq 0.4\text{ V}$ , and  $I_{OL} \geq 3.3\text{ mA}$ .)

The CD4049UB and CD4050B are designated as replacements for CD4009UB and CD4010B, respectively. Because the CD4049UB and CD4050B require only one power supply, they are preferred over the CD4009UB and CD4010B and should be used in place of the CD4009UB and CD4010B in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049UB and CD4050B are pin compatible with the CD4009UB and CD4010B respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049UB or CD4050B, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069UB Hex Inverter is recommended.

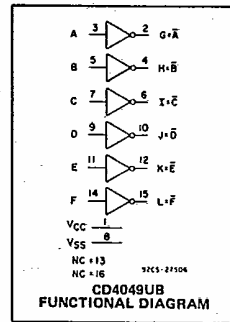
The CD4049UB and CD4050B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

**Features:**

- High sink current for driving 2 TTL loads
- High-to-low level logic conversion
- 100% tested for quiescent current at 20 V
- Maximum input current of 1  $\mu\text{A}$  at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-, 10-, and 15-volt parametric ratings

**Applications:**

- CMOS to DTL/TTL hex converter
- CMOS current "sink" or "source" driver
- CMOS high-to-low logic-level converter



**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )	-0.5V to +20V
Voltages referenced to $V_{SS}$ Terminal	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to $V_{DD} + 0.5\text{V}$
DC INPUT CURRENT, ANY ONE INPUT	$\pm 10\text{ mA}$
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$	500mW
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$	Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	100mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
STORAGE TEMPERATURE RANGE ( $T_{stg}$ )	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ Inch ( $1.59 \pm 0.79\text{mm}$ ) from case for 10s max	$+265^\circ\text{C}$

**RECOMMENDED OPERATING CONDITIONS at  $T_A=25^\circ\text{C}$ , Except as Noted.**

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range ( $V_{CC}$ ) (For $T_A = \text{Full Package-Temperature Range}$ )	3	18	V
Input Voltage Range ( $V_{IN}$ )	$V_{CC}^*$	18	V

\*The CD4049 and CD4050 have high-to-low-level voltage conversion capability but not low-to-high-level; therefore it is recommended that  $V_{IN} \geq V_{CC}$ .

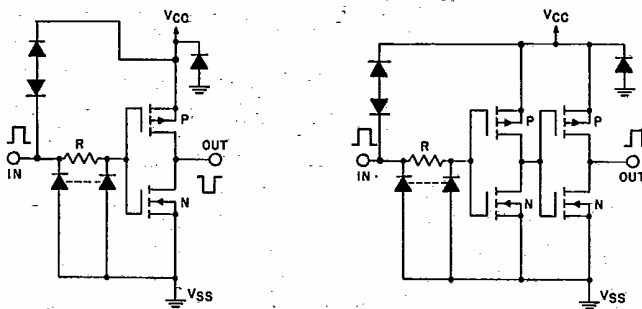
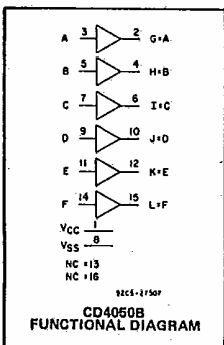


Fig. 1-a) Schematic diagram of CD4049UB, 1 of 6 identical units;  
 b) Schematic diagram of CD4050B, 1 of 6 identical units.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>CC</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	-	0.5	5	1	1	30	30	-	0.02	1	μA
	-	0.10	10	2	2	60	60	-	0.02	2	
	-	0.15	15	4	4	120	120	-	0.02	4	
	-	0.20	20	20	20	600	600	-	0.04	20	
Output Low (Sink) Current I <sub>OL</sub> Min.	0.4	0.5	4.5	3.3	3.1	2.1	1.8	2.6	5.2	-	mA
	0.4	0.5	5	4	3.8	2.9	2.4	3.2	6.4	-	
	0.5	0.10	10	10	9.6	6.6	5.6	8	16	-	
Output High Current I <sub>OH</sub> Min.	4.6	0.5	5	-0.81	-0.73	-0.58	-0.48	-0.65	-1.2	-	mA
	2.5	0.5	5	-2.6	-2.4	-1.9	-1.55	-2.1	-3.9	-	
	9.5	0.10	10	-2.0	-1.8	-1.35	-1.18	-1.65	-3.0	-	
	13.5	0.15	15	-5.2	-4.8	-3.5	-3.1	-4.3	-8.0	-	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	-	0.5	5	0.05			-	0	0.05	-	V
	-	0.10	10	0.05			-	0	0.05	-	
	-	0.15	15	0.05			-	0	0.05	-	
Output Voltage: High-Level, V <sub>OH</sub> Min.	-	0.5	5	4.95			4.95	5	-	-	V
	-	0.10	10	9.95			9.95	10	-	-	
	-	0.15	15	14.95			14.95	15	-	-	
Input Low Voltage: V <sub>IL</sub> Max. CD4049UB	4.5	-	5	1			-	-	1	-	V
	9	-	10	2			-	-	2	-	
	13.5	-	15	2.5			-	-	2.5	-	
Input Low Voltage: V <sub>IL</sub> Max. CD4050B	0.5	-	5	1.5			-	-	1.5	-	V
	1	-	10	3			-	-	3	-	
	1.5	-	15	4			-	-	4	-	
Input High Voltage: V <sub>IH</sub> Min. CD4049UB	0.5	-	5	4			4	-	-	-	V
	1	-	10	8			8	-	-	-	
	1.5	-	15	12.5			12.5	-	-	-	
Input High Voltage: V <sub>IH</sub> Min. CD4050B	4.5	-	5	3.5			3.5	-	-	-	V
	9	-	10	7			7	-	-	-	
	13.5	-	15	11			11	-	-	-	
Input Current, I <sub>IN</sub> Max.	-	0.18	18	±0.1	±0.1	±1	±1	-	±10 <sup>-5</sup>	±0.1	μA

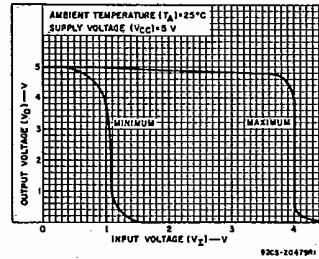


Fig. 2—Minimum and maximum voltage transfer characteristics for CD4049UB.

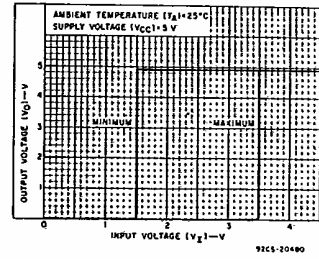


Fig. 3—Minimum and maximum voltage transfer characteristics for CD4050B.

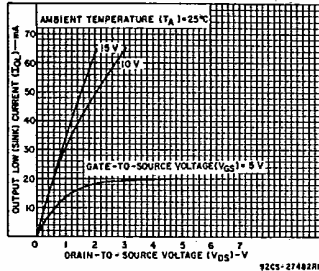


Fig. 4—Typical output low (sink) current characteristics.

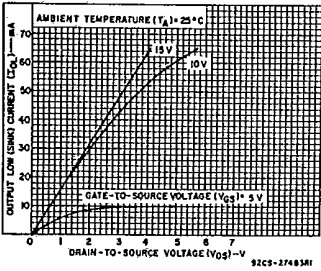


Fig. 5—Minimum output low (sink) current drain characteristics.

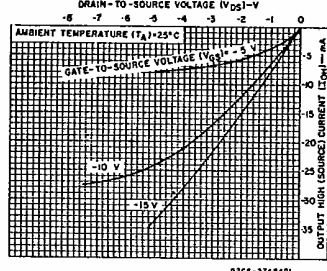


Fig. 6—Typical output high (source) current characteristics.

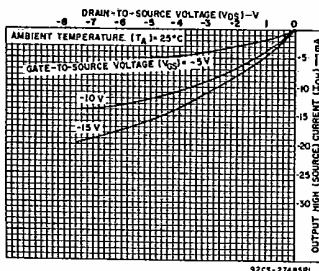


Fig. 7—Minimum output high (source) current characteristics.

COMMERCIAL CMOS HIGH VOLTAGE ICs

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A=25^\circ\text{C}$ ; Input  $t_r, t_f=20\text{ ns}$ ,  $C_L=50\text{ pF}$ ,  $R_L=200\text{ k}\Omega$

CHARACTERISTIC	CONDITIONS		LIMITS ALL PKGS.		UNITS	
	$V_{IN}$	$V_{CC}$	Typ.	Max.		
Propagation Delay Time: Low-to-High, $t_{PLH}$	CD4049UB	5	5	60	120	ns
		10	10	32	65	
		15	5	45	90	
		15	15	25	50	
	CD4050B	5	5	70	140	
		10	10	40	80	
		10	5	45	90	
		15	15	30	60	
High-to-Low, $t_{PHL}$	CD4049UB	5	5	32	65	ns
		10	10	20	40	
		15	15	15	30	
		15	5	10	20	
	CD4050B	5	5	55	110	
		10	10	22	55	
		10	5	50	100	
		15	15	15	30	
Transition Time: Low-to-High, $t_{TLH}$	CD4049UB	5	5	80	160	ns
		10	10	40	80	
		15	15	30	60	
		15	5	30	60	
	CD4050B	5	5	30	60	
		10	10	20	40	
		10	5	15	30	
		15	15	15	30	
Input Capacitance, $C_{IN}$	CD4049UB	—	—	15	22.5	pF
	CD4050B	—	—	5	7.5	

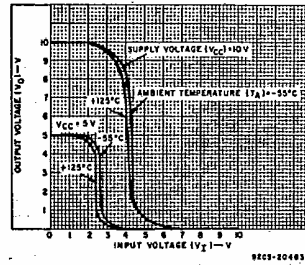


Fig. 8 — Typical voltage transfer characteristics as a function of temperature for CD4049UB.

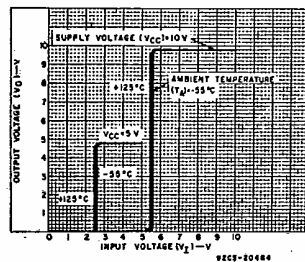


Fig. 9 — Typical voltage transfer characteristics as a function of temperature for CD4050B.

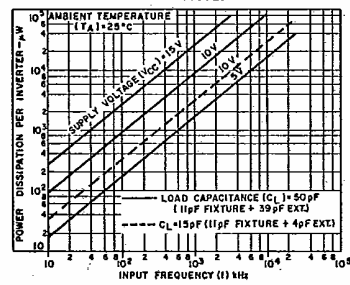


Fig. 10 — Typical power dissipation vs. frequency characteristics.

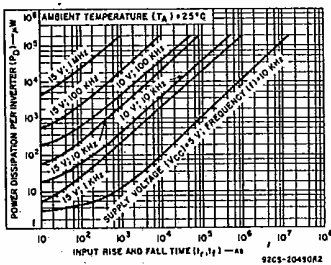


Fig. 11 — Typical power dissipation vs. input rise and fall times per inverter for CD4049UB.

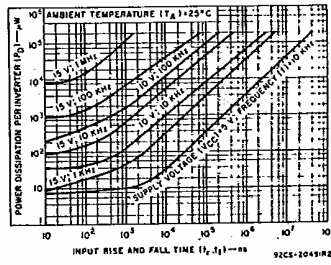


Fig. 12 — Typical power dissipation vs. input rise and fall times per inverter for CD4050B.

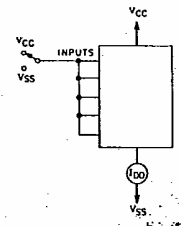


Fig. 13 — Quiescent device current test circuit.

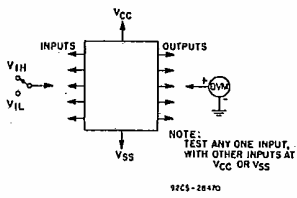


Fig. 14 - Input voltage test circuit.

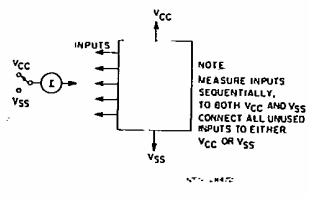


Fig. 15 - Input current test circuit.

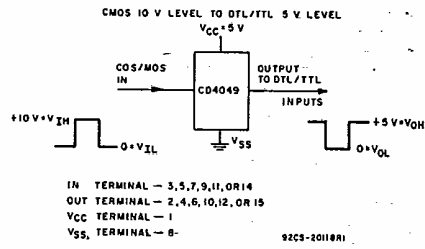
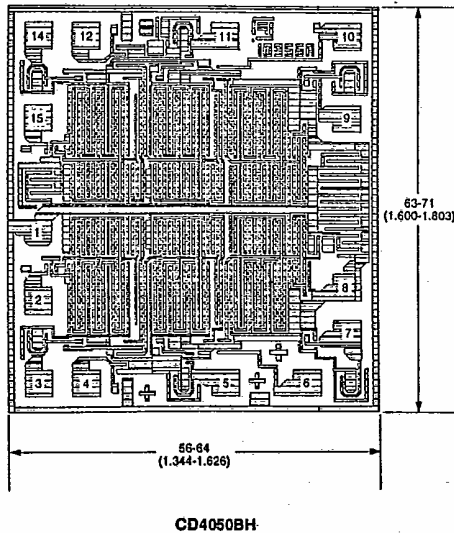
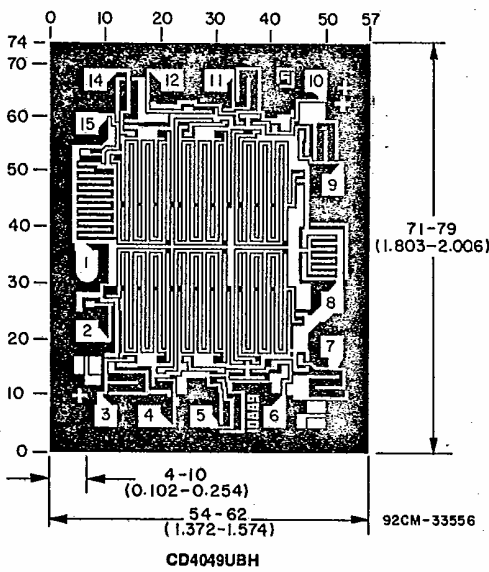


Fig. 16 - Logic-level conversion application.

CHIP DIMENSIONS AND PAD LAYOUTS



3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

TERMINAL ASSIGNMENTS

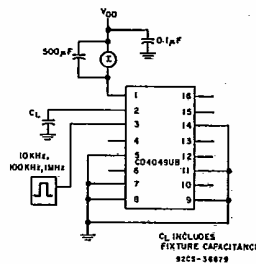
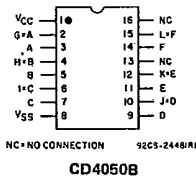
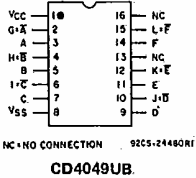


Fig. 17 - Dynamic power dissipation test circuit.