MOTOROLA
Semiconductor Products Sector

MMC2080/2075/D
Rev. 0, 10/1999

MMC2080/2075

Advance Information

MMC2080/2075 Integrated Processor with Roaming FLEX™ Decoder

Part 1 Introduction

The MMC2080/2075 is designed to provide the messaging and paging marketplace with a powerful and flexible solution to carry communications design into the next millennium. The MMC2080 integrates two of Motorola's most successful product families, M•CORE™ and the Roaming FLEX™ alphanumeric decoders, a combination that will set a new standard in the communications industry. Except for the FLEX decoder, the MMC2075 offers all features of the MMC2080.

Both the The MMC2080/2075 are members of the low-power, high-performance M•CORE family of 32-bit microcontroller units (MCUs). The M•CORE is a streamlined execution engine that provides many of the performance enhancements found in mainstream reduced instruction set computers (RISCs). Combining performance, speed, and cost efficiency in a compact, low-power design, the M•CORE microRISC architecture is a natural solution for applications where battery life and systems cost are critical design goals.

Given that a total system's components and processor core determine its power consumption, the instruction set architecture (ISA) for the M•CORE is designed to optimize the trade-off between performance and total power consumption. The result is system-wide reduction of total energy consumption with maintenance of acceptable performance levels. Memory power consumption (both on-chip and external) is a major factor in system energy consumption. By adopting 16-bit instruction encoding, and thus significantly decreasing the memory bandwidth needed for a high rate of instruction execution, the MMC2080/2075 minimizes the overhead of memory system energy consumption.

The MMC2080/2075 also reduces power consumption by coupling a fully static design with dynamic power management and low-voltage operation. Versatile power management is achieved through automatic power downs of any internal functional blocks not needed on a clock-by-clock basis. Power conservation modes are also provided for absolute power conservation.

A table of contents for this document appears on the following page. Figure 1 on page 3 and Figure 2 on page 4 provide simplified block diagrams of the MMC2080/2075.

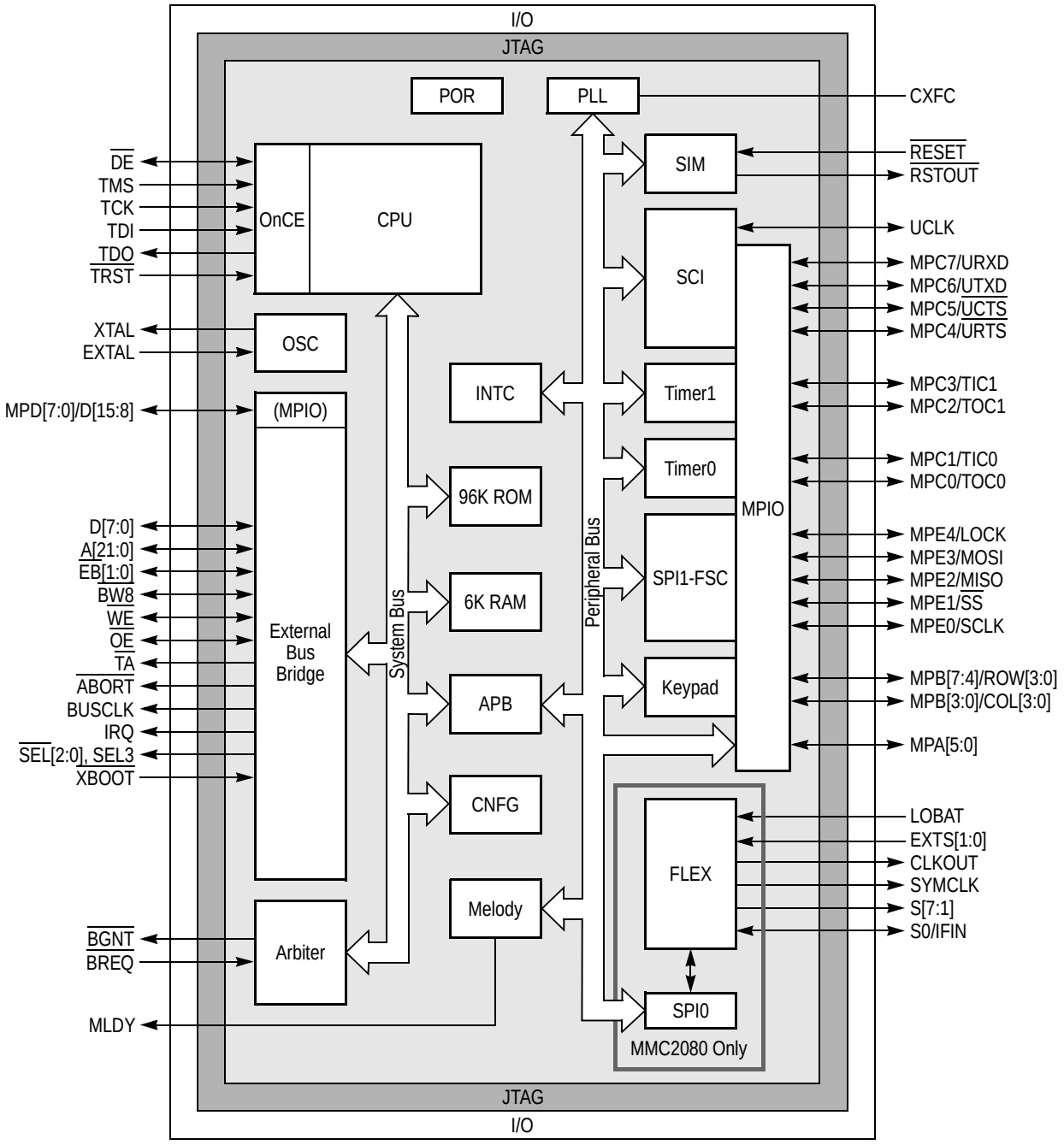


Figure 1. MMC2080/2075 144 Block Diagram (144-Pin Package)

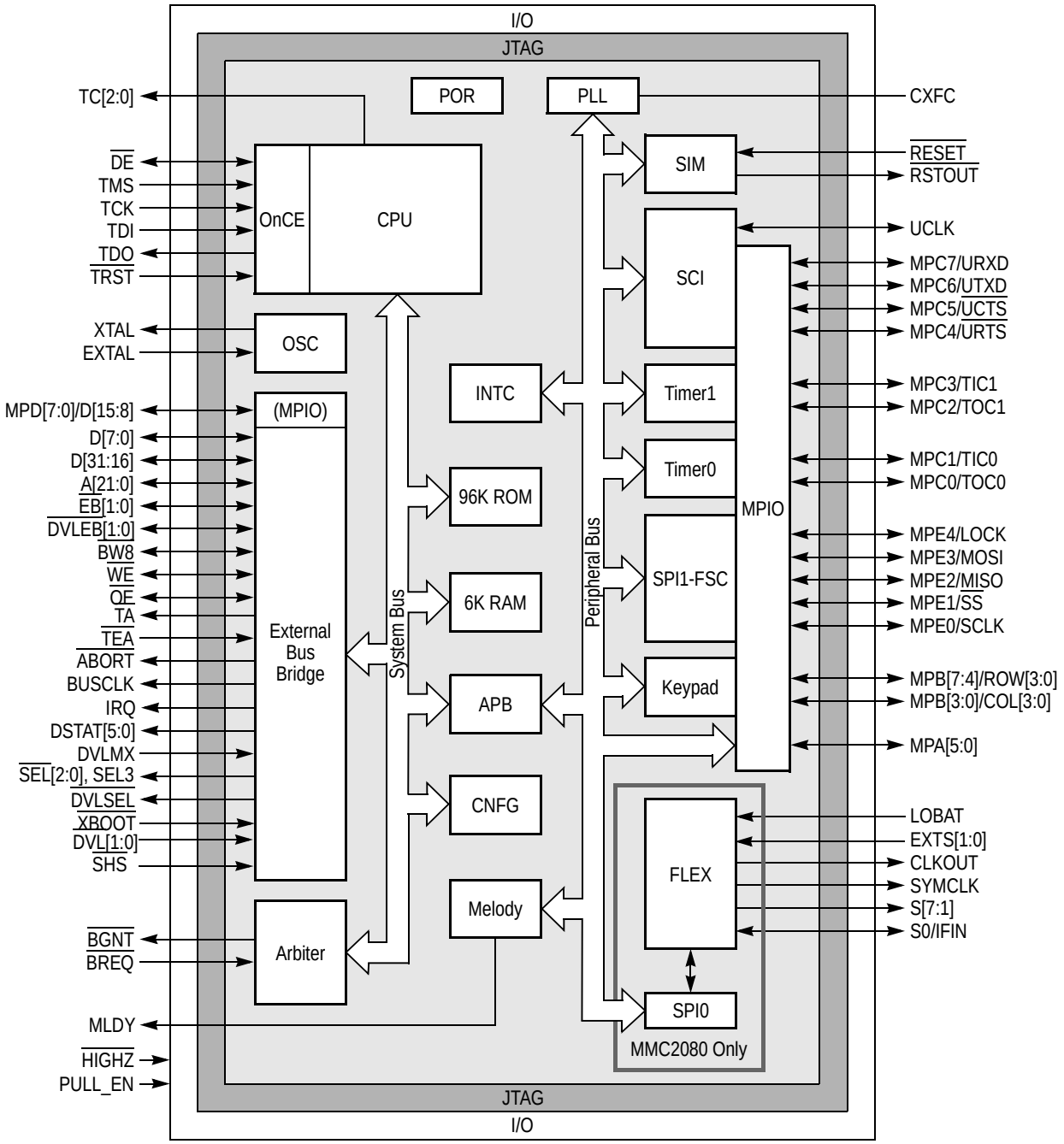


Figure 2. MMC2080/2075 DVL Block Diagram (208-Pin Package)

1.1 Conventions and Terminology

This document uses the following conventions:

- $\overline{\text{OVERBAR}}$ is used to indicate a signal that is active when pulled low: for example, $\overline{\text{RESET}}$.
- *Logic level one* is a voltage that corresponds to Boolean true (1) state.
- *Logic level zero* is a voltage that corresponds to Boolean false (0) state.
- To *set* a bit or bits means to establish logic level one.
- To *clear* a bit or bits means to establish logic level zero.
- A *signal* is an electronic construct whose state or changes in state convey information.
- A *pin* is an external physical connection. The same pin can be used to connect a number of signals.
- *Asserted* means that a discrete signal is in active logic state.
  - *Active low* signals change from logic level one to logic level zero.
  - *Active high* signals change from logic level zero to logic level one.
- *Deasserted* means that an asserted discrete signal changes logic state.
  - *Active low* signals change from logic level zero to logic level one.
  - *Active high* signals change from logic level on to logic level zero.
- LSB means *least significant bit* or *bits*. MSB means *most significant bit* or *bits*. References to low and high bytes or words are spelled out.

Please refer to the examples in Table 1.

Table 1. Data Conventions

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

1.2 Features

The MMC2080/2075 offers the following suite of features.

- M•CORE™ RISC Processor
  - — 32-bit load/store M•CORE RISC architecture
  - — Fixed 16-bit instruction length
  - — 16-entry 32-bit general-purpose register file
  - — 32-bit internal address and data buses
  - — Efficient, four-stage, fully interlocked execution pipeline
  - — Single-cycle execution for most instructions; two cycles for branches and memory accesses
  - — Special branch, byte, and bit manipulation instructions
  - — Support for byte, halfword, and word memory accesses
  - — Fast interrupt support via vectoring/auto-vectoring and a 16-entry dedicated alternate register file
- Integrated Roaming FLEX alphanumeric decoder (MMC2080 only)
  - — FLEX paging protocol signal processor
  - — 1600, 3200, and 6400 bits per second (bps) decoding
  - — Highly programmable receiver control
  - — FLEX message fragmentation and group messaging support
  - — SSID and NID roaming support
  - — Internal demodulator and data slicer
  - — Improved battery savings via partial address correlation and intermittent receiver clock
  - — Full support for revision G1.9 of the FLEX protocol
  - — External CAP code access through parallel or serial FLASH/PROM
- On-chip memory
  - — 24 K × 32 CPU ROM (96 K)
  - — 1.5 K × 32 CPU RAM (6 K)
- On-chip peripherals
  - — Asynchronous serial communications interface (SCI) with IrDA capability
  - — Synchronous serial peripheral interface (SPI)
  - — Frequency synthesizer controller (FSC)
  - — Melody generator
  - — 4 × 4 keypad interface
  - — Multipurpose I/O ports (MPIO)
  - — Two 16-bit general purpose timers
  - — Time-of-day (TOD) timer
  - — Watchdog timer
  - — Vectored interrupt controller with 16 programmable priority levels

  - — Oscillator and PLL with software selectable speeds
  - — AMBA peripheral bridge depipelines system bus for simpler peripheral bus
  - — 8/16-bit external system bus with 22-bit address bus
- Operating features
  - — Processor operation to 10 MHz over full operating range
  - — Low-power modes
  - — OnCE™ (On-Chip Emulation) debug module
  - — Voltage range 1.8 V to 3.6 V; temperature range -20 °C to 85 °C
  - — Chip-select outputs for four external devices (4 Mbyte per chip select, 16 Mbyte directly addressable)
  - — Programmable wait states for external accesses
  - — External boot option
  - — External bus interface that accepts internal, half-word, and byte transfers
  - — External device that may become system bus master
- Development tools
  - — Development option (different package) that adds select to bypass internal ROM
  - — Development option (different package) that extends external bus to 32 bits
  - — External bus that can display internal transfers

1.3 Integrated Roaming FLEX Protocol and the MMC2080

The MMC2080 integrates several field-proven technologies, providing a versatile Roaming FLEX solution. The MMC2080 operates the integrated FLEX decoder in an efficient power-consumption mode, allowing the CPU to operate in a low-power mode when monitoring for message information. The Roaming FLEX protocol is a multichannel, high-performance protocol that leading service providers worldwide have adopted as a de facto standard for roaming paging. Roaming FLEX protocol gives service providers increased capacity, added reliability, enhanced pager battery performance, and the ability to control a PLL-synthesized receiver and to receive paging messages from a list of paging channels. Finally, the MMC2080 gives the service provider an upward migration path that is completely transparent to the end user.

1.4 Target Applications

The MMC2080/2075 is intended for use in wireless and paging applications. The MMC2080 is designed for applications needing an M•CORE CPU coupled with a roaming FLEX Decoder. The MMC2075 is intended for applications requiring the processing power and flexibility of the M•CORE CPU.

1.5 Product Documentation

The three documents listed in Table 2 are required for a complete description of the MMC2080/2075 and are necessary to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola Semiconductor Products Sector sales office, a Motorola Literature Distribution Center, or the World Wide Web. See the last page of this document for contact information.

Table 2. MMC2080/2075 Documentation

Document Name	Description of Contents	Order Number
M•CORE Reference Manual	Detailed description of the M•CORE MCU and instruction set	MCORERM/AD
MMC2080/2075 User's Manual	Detailed description of the MMC2080/2075 memory, peripherals, and interfaces	MMC2080/2075UM/D
MMC2080/2075 Technical Data	MMC2080/2075 pin and package descriptions; electrical and timing specifications	MMC2080/2075/D

1.6 Ordering Information

Table 3 lists the information you need to supply when placing an order. Consult a Motorola Semiconductor Products Sector sales office or authorized distributor to determine availability and to order parts.

Table 3. MMC2080/2075 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Order Number
MMC2080	3 V	12 mm x 12 mm MAP BGA	144	MMC2080VF001
MMC2075	3 V	12 mm x 12 mm MAP BGA	144	MMC2075VF001
MMC2080	3 V	43 mm x 43 mm Ceramic PGA	208	Contact Factory Development Use Only
MMC2075	3 V	43 mm x 43 mm Ceramic PGA	208	

Part 2 Signal and Connection Descriptions

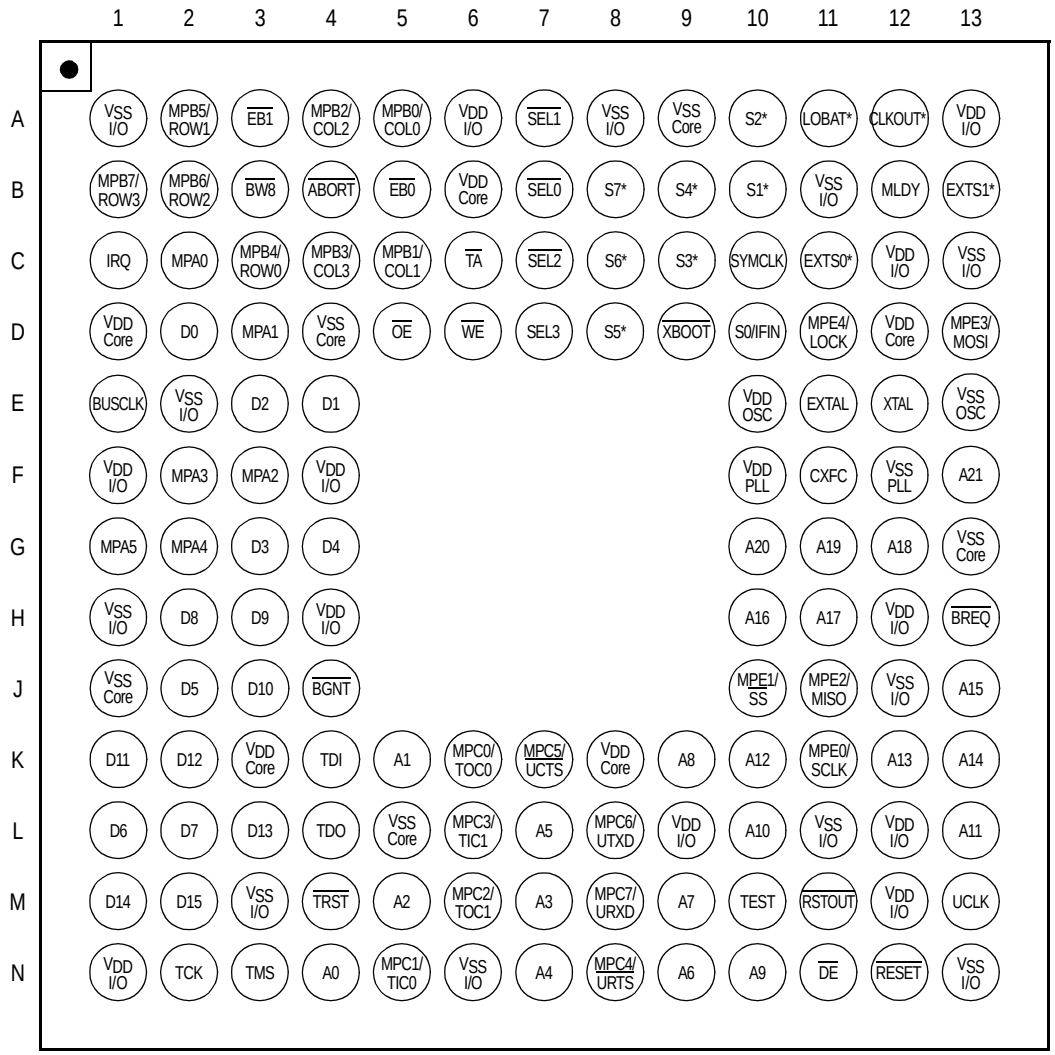
The pins and signals of the MMC2080/2075 are described in the following sections. Figure 3 on page 10 and Figure 4 on page 11 are top and bottom views, respectively, of the 12 mm x 12 mm MAP Ball Grid Array (BGA) package, and Figure 5 on page 12 and Figure 6 on page 13 are top and bottom views, respectively, of the 43 mm x 43 mm ceramic Pin Grid Array (PGA) package, showing the pin-outs. Table 4 on page 14 and Table 5 on page 17 list the pins by number and signal name.

Figure 7 on page 21 is a representational pin-out of the chip, grouping the signals by their function. Table 6 on page 20 identifies the number of signals for each group and refers to Table 8 on page 23 through Table 20 on page 27, which are organized according to signal type and give a brief description of each signal pin.

2.1 MMC2080/2075 Pin Descriptions

The following section provides information about the available packages for this product, including diagrams of the package pin-outs and tables describing how the signals of the MMC2080/2075 are allocated. There are two packages for each part:

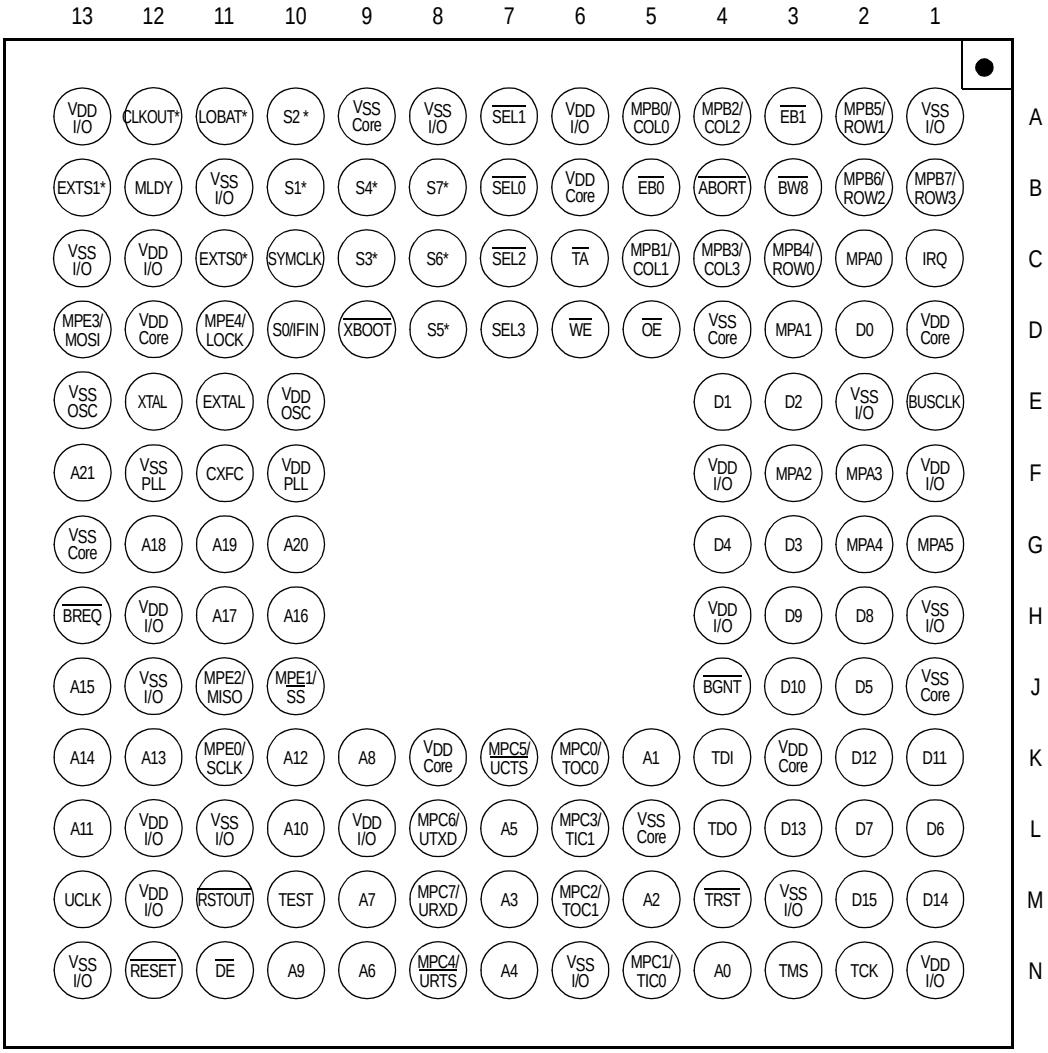
- The 144-pin I/O, STD small ball (SMBALL) mold array process (MAP) ball grid array (BGA), 12 mm x 12 mm package. Table 4 on page 14 identifies the signal associated with each pin.
- The 208-pin I/O, PGA, 43 mm x 43 mm ceramic package. Table 5 on page 17 identifies the signal associated with each pin.



Top View

* Signal available only in 2080

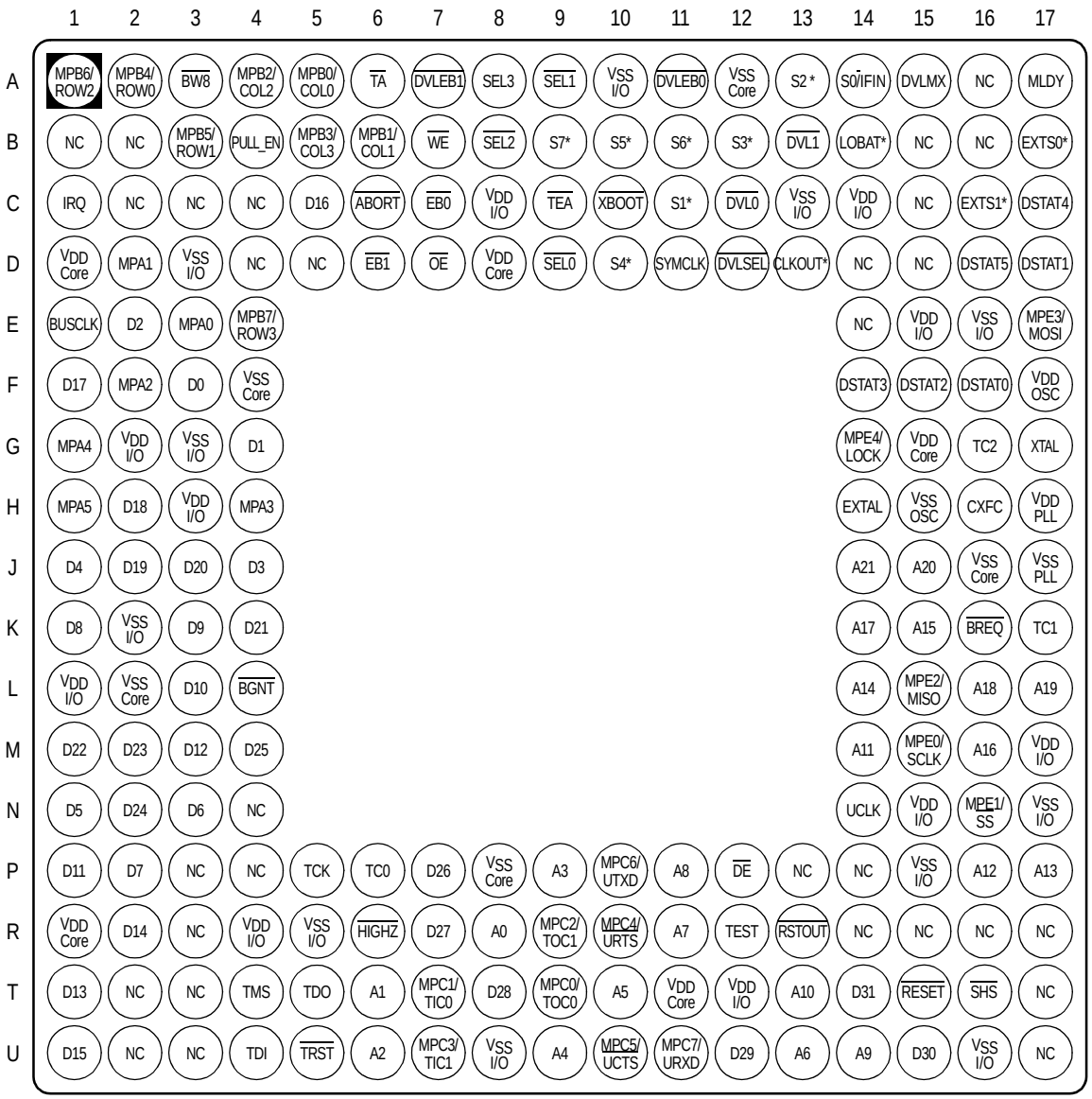
Figure 3. MMC2080/2075 BGA (144-Pin) Top View



Bottom View

* Signal available only in 2080

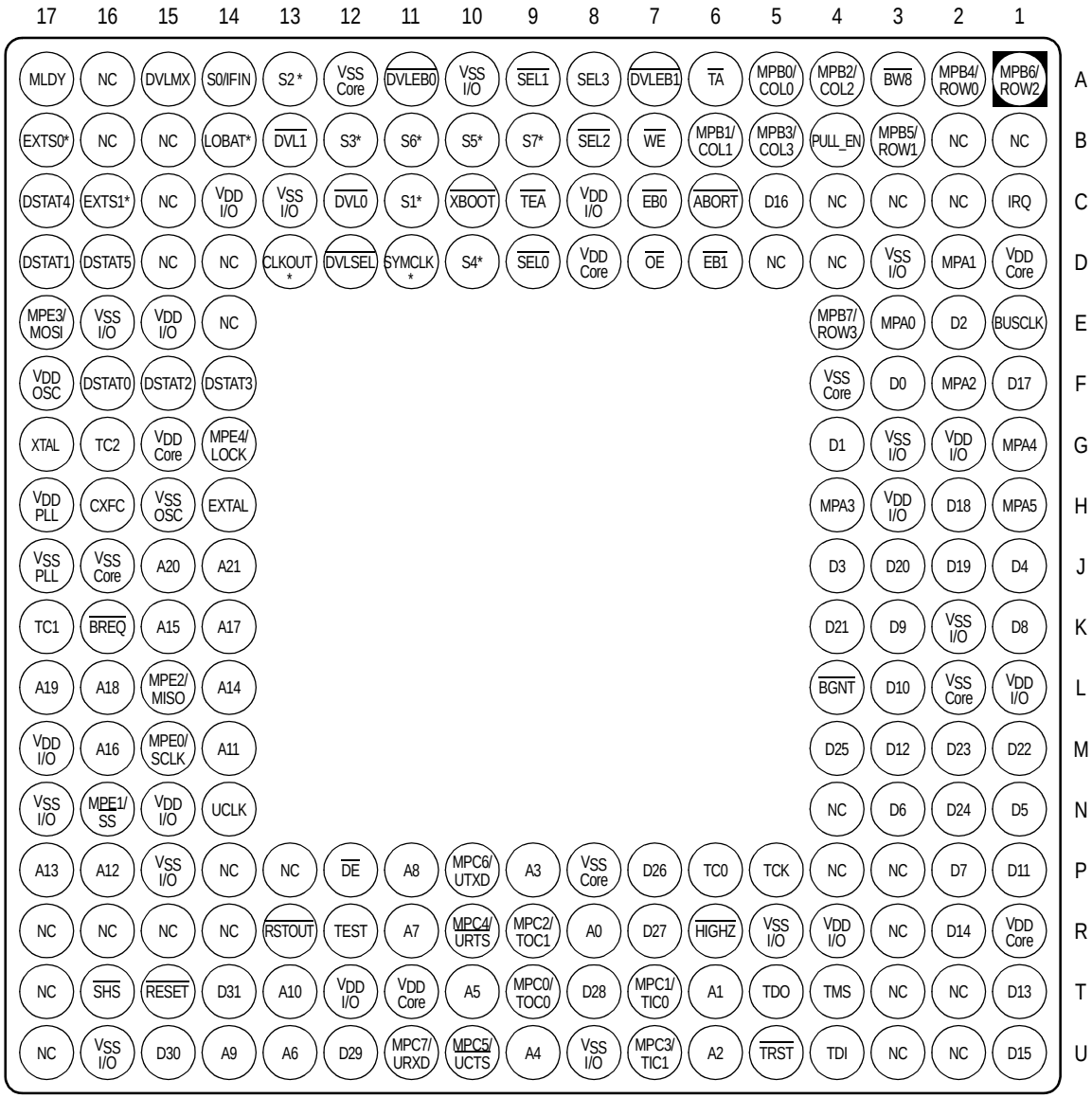
Figure 4. MMC2080/2075 BGA (144-Pin) Bottom View



Top View

* Signal available only in 2080

Figure 5. MMC2080/2075 PGA (208-Pin) Top View



Bottom View

* Signal available only in 2080

Figure 6. MMC2080/2075 PGA (208-Pin) Bottom View

Table 4. MMC2080/2075 BGA (144-Pin) Signal ID by Pin Number (Sheet 1 of 3)

Pin Number	Signal Name	Pin Number	Signal Name
A1	Vss I/O	G10	A20
A2	MPB5/ROW1	G11	A19
A3	$\overline{BW8}$	G12	A18
A4	MPB2/COL2	G13	Vss Core
A5	MPB0/COL0	H1	Vss I/O
A6	Vdd I/O	H2	D8
A7	$\overline{SEL1}$	H3	D9
A8	Vss I/O	H4	Vdd I/O
A9	Vss Core	H10	A16
A10	S2 (2080 Only)	H11	A17
A11	LOBAT (2080 Only)	H12	Vdd I/O
A12	CLKOUT (2080 Only)	H13	$\overline{BREQ}$
A13	Vdd I/O	J1	Vss Core
B1	MPB7/ROW3	J2	D5
B2	MPB6/ROW2	J3	D10
B3	$\overline{BW8}$	J4	$\overline{BGNT}$
B4	$\overline{ABORT}$	J10	MPE1/$\overline{SS}$
B5	$\overline{EB0}$	J11	MPE2/MIS0
B6	Vdd Core	J12	Vss I/O
B7	$\overline{SEL0}$	J13	A15
B8	S7 (2080 Only)	K1	D11
B9	S4 (2080 Only)	K2	D12
B10	S1 (2080 Only)	K3	Vdd Core
B11	Vss I/O	K4	TDI
B12	MLDY	K5	A1
B13	EXTS1 (2080 Only)	K6	MPC0/TOC0
C1	IRQ	K7	MPC5/$\overline{UCTS}$
C2	MPA0	K8	Vdd Core

Table 4. MMC2080/2075 BGA (144-Pin) Signal ID by Pin Number (Sheet 2 of 3)

Pin Number	Signal Name	Pin Number	Signal Name
C3	MPB4/ROW0	K9	A8
C4	MPB3/COL3	K10	A12
C5	MPB1/COL1	K11	MPE0/SCLK
C6	$\overline{TA}$	K12	A13
C7	$\overline{SEL2}$	K13	A14
C8	S6 (2080 Only)	L1	D6
C9	S3 (2080 Only)	L2	D7
C10	SYMCLK (2080 Only)	L3	D13
C11	EXTS0 (2080 Only)	L4	TDO
C12	Vdd I/O	L5	Vss Core
C13	Vss I/O	L6	MPC3/TIC1
D1	Vdd Core	L7	A5
D2	D0	L8	MPC6/UTXD
D3	MPA1	L9	Vdd I/O
D4	Vss CORE	L10	A10
D5	$\overline{OE}$	L11	Vss I/O
D6	WE	L12	Vdd I/O
D7	SEL3	L13	A11
D8	S5 (2080 Only)	M1	D14
D9	$\overline{XBOOT}$	M2	D15
D10	S0/IFIN (2080 only)	M3	Vss I/O
D11	MPE4/LOCK	M4	$\overline{TRST}$
D12	Vdd Core	M5	A2
D13	MPE3/MOSI	M6	MPC2/TOC1
E1	BUSCLK	M7	A3
E2	Vss I/O	M8	MPC7/URXD
E3	D2	M9	A7
E4	D1	M10	TEST

Table 4. MMC2080/2075 BGA (144-Pin) Signal ID by Pin Number (Sheet 3 of 3)

Pin Number	Signal Name	Pin Number	Signal Name
E10	Vdd OSC	M11	$\overline{\text{RSTOUT}}$
E11	EXTAL	M12	Vdd I/O
E12	XTAL	M13	UCLK
E13	Vss OSC	N1	Vdd I/O
F1	Vdd I/O	N2	TCK
F2	MPA3	N3	TMS
F3	MPA2	N4	A0
F4	Vdd I/O	N5	MPC1/TIC0
F10	Vdd PLL	N6	Vss I/O
F11	CXFC	N7	A4
F12	Vss PLL	N8	MPC4/$\overline{\text{URTS}}$
F13	A21	N9	A6
G1	MPA5	N10	A9
G2	MPA4	N11	$\overline{\text{DE}}$
G3	D3	N12	$\overline{\text{RESET}}$
G4	D4	N13	Vss I/O

Table 5. MMC2080/2075 PGA (208-Pin) Signal ID by Pin Number (Sheet 1 of 4)

Pin Number	Signal Name	Pin Number	Signal Name
A1	MPB6/ROW2	J4	D3
A2	MPB4/ROW0	J14	A21
A3	$\overline{BW8}$	J15	A20
A4	MPB2/COL2	J16	Vss Core
A5	MPB0/COL0	J17	Vss PLL
A6	$\overline{TA}$	K1	D8
A7	$\overline{DVLEB1}$	K2	Vss I/O
A8	SEL3	K3	D9
A9	$\overline{SEL1}$	K4	D21
A10	Vss I/O	K14	A17
A11	$\overline{DVLEB0}$	K15	A15
A12	Vss Core	K16	BREQ
A13	S2 (2080 Only)	K17	TC1
A14	S0/$\overline{IFIN}$ (2080 only)	L1	Vdd I/O
A15	DVLMX	L2	Vss Core
A17	MLDY	L3	D10
B3	MPB5/ROW1	L4	$\overline{BGNT}$
B4	PULL_EN	L14	A14
B5	MPB3/COL3	L15	MPE2/MIS0
B6	MPB1/COL1	L16	A18
B7	$\overline{WE}$	L17	A19
B8	$\overline{SEL2}$	M1	D22
B9	S7 (2080 Only)	M2	D23
B10	S5 (2080 Only)	M3	D12
B11	S6 (2080 Only)	M4	D25
B12	S3 (2080 Only)	M14	A11
B13	DVL1	M15	MPE0/SCLK
B14	LOBAT (2080 Only)	M16	A16

Table 5. MMC2080/2075 PGA (208-Pin) Signal ID by Pin Number (Sheet 2 of 4)

Pin Number	Signal Name	Pin Number	Signal Name
B17	EXTS0 (2080 Only)	M17	Vdd I/O
C1	IRQ	N1	D5
C5	D16	N2	D24
C6	$\overline{\text{ABORT}}$	N3	D6
C7	$\overline{\text{EB0}}$	N14	UCLK
C8	Vdd I/O	N15	Vdd I/O
C9	TEA	N16	MPE1/SS
C10	XBOOT	N17	Vss I/O
C11	S1 (2080 Only)	P1	D11
C12	DVLO	P2	D7
C13	Vss I/O	P3	TCK
C14	Vdd I/O	P4	TC0
C16	EXTS1 (2080 Only)	P5	TCK
C17	DSTAT4	P6	TC0
D1	Vdd Core	P7	D26
D2	MPA1	P8	VssCore
D3	Vss I/O	P9	A3
D4	EB1	P10	MPC6/UTXD
D5	OE	P11	A8
D6	Vdd Core	P12	$\overline{\text{DE}}$
D7	$\overline{\text{OE}}$	P15	Vss I/O
D8	VddCORE	P16	A12
D9	$\overline{\text{SEL0}}$	P17	A13
D10	S4 (2080 Only)	R1	Vdd Core
D11	SYMCLK (2080 Only)	R2	D14
D12	DVLSEL	R4	Vdd I/O
D13	CLKOUT (2080 Only)	R5	Vss I/O
D16	DSTAT5	R6	HIGHZ

Table 5. MMC2080/2075 PGA (208-Pin) Signal ID by Pin Number (Sheet 3 of 4)

Pin Number	Signal Name	Pin Number	Signal Name
D17	DSTAT1	R7	D27
E1	BUSCLK	R8	A0
E2	D2	R9	MPC2/TOC1
E3	MPA0	R10	MPC4/$\overline{\text{URTS}}$
E4	MPB7/ROW3	R11	A7
E15	Vdd I/O	R12	TEST
E16	Vss I/O	R13	$\overline{\text{RSTOUT}}$
E17	MPE3/MOSI	T1	D13
F1	D17	T4	TMS
F2	MPA2	T5	TDO
F3	D0	T6	A1
F4	Vss CORE	T7	MPC1/TIC0
F14	DSTAT3	T8	D28
F15	DSTAT2	T9	MPC0/TOC0
F16	DSTAT0	T10	A5
F17	Vdd OSC	T11	Vdd Core
G1	MPA4	T12	Vdd I/O
G2	Vdd I/O	T13	A10
G3	Vss I/O	T14	D31
G4	D1	T15	$\overline{\text{RESET}}$
G14	MPE4/LOCK	T16	SHS
G15	Vdd Core	U1	D15
G16	TC2	U4	TDI
G17	XTAL	U5	$\overline{\text{TRST}}$
H1	MPA5	U6	A2
H2	D18	U7	MPC3/TIC1
H3	Vdd I/O	U8	Vss I/O
H4	MPA3	U9	A4

Table 5. MMC2080/2075 PGA (208-Pin) Signal ID by Pin Number (Sheet 4 of 4)

Pin Number	Signal Name	Pin Number	Signal Name
H14	EXTAL	U10	MPC5/$\overline{\text{UCTS}}$
H15	Vss OSC	U11	MPC7/URXD
H16	CXFC	U12	D29
H17	Vdd PLL	U13	A6
J1	D4	U14	A9
J2	D19	U15	D30
J3	D20	U16	Vss I/O

2.2 Tables of Signals

The MMC2080 input and output signals are organized into functional groups in Table 6 and in Figure 7 on page 21. Table 7 on page 22 displays data relating to I/O cell names, including descriptions and the availability of Hi-Z impedance, pull-up resistors, and high drive-current capability. Table 8 on page 23 through Table 20 on page 27 are organized according to signal type and give a brief description of each signal pin. Package type is indicated as “N” for the 144-pin normal-function package. All pins are available in the 208-pin development extensions package.

Table 6. MMC2080 Signal Functional Group Organization

Functional Group	Number of Signals	Detailed Description
Arbitration signals	2	Table 20 on page 27
External system bus signals	52	Table 8 on page 23
Development extensions (208-pin package only)	34	Table 9 on page 24
FLEX signals	13	Table 10 on page 25
FSC/SPI signals	5	Table 11 on page 25
SCI signals	5	Table 12 on page 25
Timer signals	4	Table 13 on page 26
Melody generator signals	1	Table 14 on page 26
Keypad signals	8	Table 15 on page 26
Dedicated MPIO signals	6	Table 16 on page 26
SIM signals	2	Table 17 on page 26
JTAG/OnCE signals	6	Table 18 on page 27
Clock and power	40	Table 19 on page 27

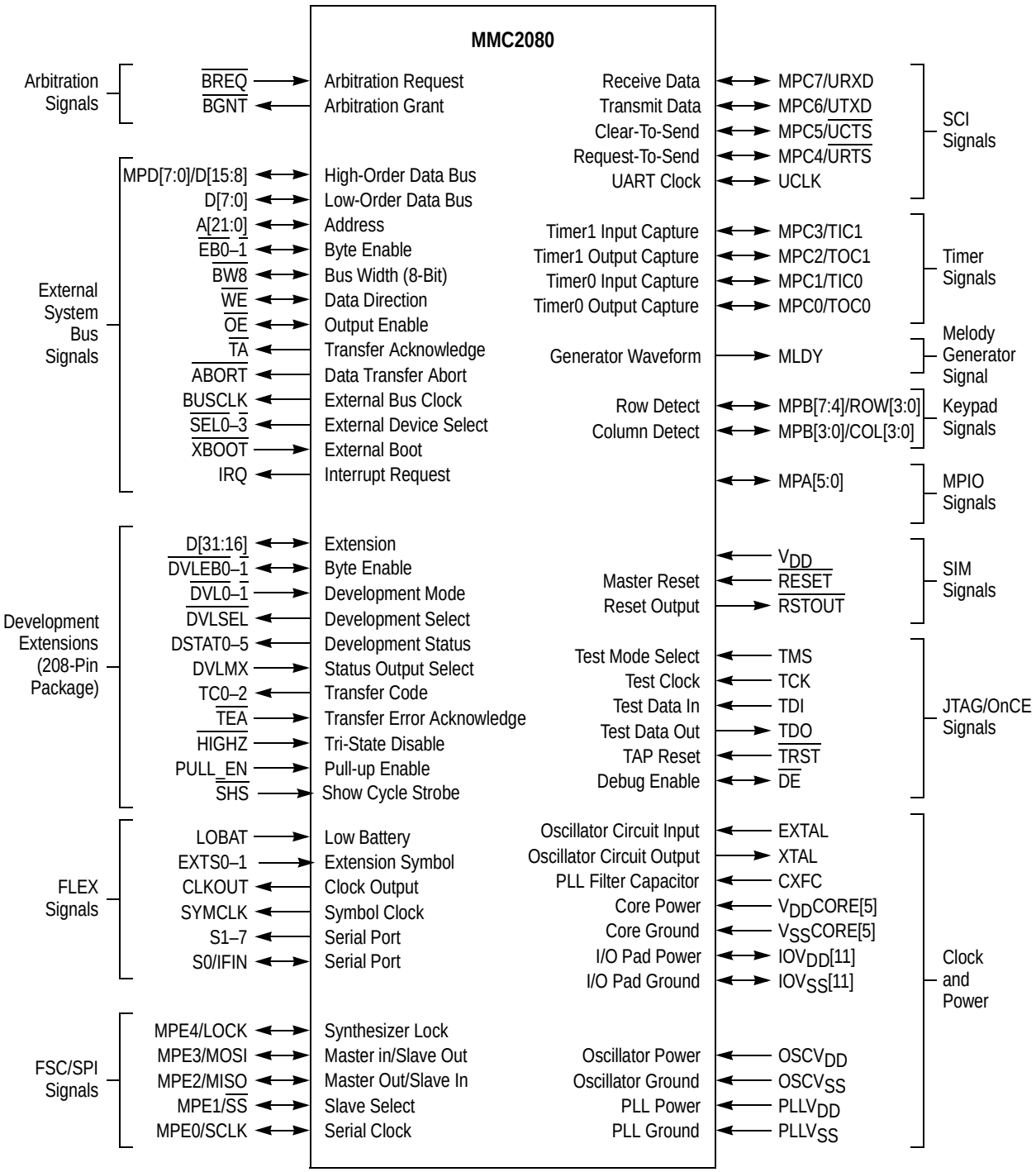


Figure 7. MMC2080 Signal Group Organization

Table 7. I/O Cell Description

I/O Cell Name	Description	Hi-Z	Pull-up	High Drive Capable
OTP	Tri-state output with selectable drive strength; always enabled with strong drive except during JTAG Hi-Z command or unless otherwise stated	Y	N	Y
INHP	Input with hysteresis	N	N	N
INHPP	INHP with selectable pull-up enable	N	Y	N
IOHP	INHP and OTP	Y	N	Y
IOHPPH	INHPP and OTP	Y	Y	Y
SWIOP	High-current IOHPPH	Y	Y	Y
AIN/AOT	Analog input/output (same cell)	N	N	N

Table 8. External System Bus Signals

Signal Name	Dir	N	I/O Cell	Description
MPD[7:0]/D[15:8]	I/O	Y	IOHPPH	**High-Order Data Bus**—May be used as general I/O when the data bus is configured as an 8-bit bus. Output drivers are disabled and pull-up resistors are enabled during reset.
D[7:0]	I/O	Y	IOHPPH	**Low-Order Data Bus**—Output drivers are disabled and pull-up resistors are enabled during reset.
A[21:0]	I/O	Y	IOHP	**Address**—Input when $\overline{\text{BGNT}}$ is low; otherwise output. Twenty-two bits is a 4 Mbyte address space.
$\overline{\text{EB}}$[1:0]	I/O	Y	IOHP	**Byte Enable** (active low)—Input when $\overline{\text{BGNT}}$ is low; otherwise output. $\overline{\text{EB0}}$ enables D[15:8] and $\overline{\text{EB1}}$ enables D[7:0]. When the data bus is configured as an 8-bit bus, $\overline{\text{EB0}}$ is always released (high) and $\overline{\text{EB1}}$ is always asserted (low).
$\overline{\text{BW8}}$	I/O	Y	IOHPPH	**Bus Width 8** (open-drain, active low)—If this pin is driven low either externally or internally, the external bus functions as an 8-bit bus.
$\overline{\text{WE}}$	I/O	Y	IOHP	**Write Enable** (active low)—Input when $\overline{\text{BGNT}}$ is low. When $\overline{\text{WE}}$ is low, data is driven by an external device and received by the MMC2080. Output when $\overline{\text{BGNT}}$ is high. When $\overline{\text{WE}}$ is low, data is driven by the MMC2080 and received by an external device.
$\overline{\text{OE}}$	I/O	Y	IOHP	**Output Enable** (active low)—Input when $\overline{\text{BGNT}}$ is low; when $\overline{\text{OE}}$ is high, D[7:0] (and D[15:8] when in 16-bit mode) external data drivers are disabled. Output when $\overline{\text{BGNT}}$ is high; when $\overline{\text{OE}}$ is high, drivers are disabled.
$\overline{\text{TA}}$	O	Y	OTP	**Transfer Acknowledge** (active low)—An external transaction continues when this pin is high. When low, the external data transfer cycle will complete. When MONITOR mode is set. $\overline{\text{TA}}$ also indicates the end of internal transactions.
$\overline{\text{ABORT}}$	O	Y	OTP	**Data Transfer Abort** (active low)—When a transaction is aborted, this pin is driven low.
BUSCLK	O	Y	OTP	**External Bus Clock**.
$\overline{\text{SEL}}$[3:0]	O	Y	OTP	**External Device Select**—$\overline{\text{SEL0}}$ is always active low; SEL[3:1] may be individually programmed as active low or active high. After reset, SEL3 is active high. $\overline{\text{SEL1}}$ and $\overline{\text{SEL2}}$ are active low after restart.
$\overline{\text{XBOOT}}$	I	Y	INHPP	**External Boot** (active low)—If this pin is low after a reset, the external boot portion of the system memory map is enabled; otherwise the internal boot map is enabled.
IRQ	O	Y	OTP	**Interrupt Request**—This is driven high when either a normal interrupt or a fast interrupt is generated by the interrupt controller.

Table 9. Development Extensions (208-Pin Package)

Signal Name	Dir	N	I/O Cell	Description
D[31:16]	I/O	N	IOHPPH	Extension to provide a 32-bit external bus. The bus is enabled when either DVL0 or _DVL0 is asserted.
DVLEB[1:0]	I/O	N	IOHPPH	**Byte Enable** (active low)—Input when BGNT is low; otherwise output. DVLEB0 enables D[31:24] and DVLEB1 enables D[23:16].
DVL[1:0]	I	N	INHPP	**Development Mode**—When DVL1 is low, the internal ROM is bypassed. If the ROM space is addressed when DVL1 is low and XBOOT is high, the 32-bit extension is enabled and DVLSEL is asserted to select an external memory. When DVL0 is low, the 32-bit bus extension is enabled for external bus masters (BGNT is low) and for debug monitor modes.
DVLSEL	O	N	OTP	**Development Select** (active low)—When DVL1 is low and XBOOT is high, this output is asserted when the internal ROM locations are addressed.
DVLMX	I	N	INHPP	Selects the output of DSTAT[5:0].
DSTAT[5:0]	O	N	OTP	When DVLMX is high, DSTAT is the low-order 6 bits of the interrupt vector. When DVLMX is low, DSTAT[3:0] is the M•CORE pipeline status, PSTAT[3:0], and DSTAT[5:4] is the transfer size in M•CORE format.
TC[2:0]	O	N	OTP	**Processor Transfer Code**.
TEA	I	N	INHPP	**Transfer Error Acknowledge** (active low).
HIGHZ	I	N	INHPP	**Tri-State Disable** (active low)—When asserted (low), all tri-state outputs are disabled (high-z). This performs the same function as the JTAG HIGHZ command.
PULL_EN	I	N	INHPP	**Enable Pull-up Resistors**—When low, all pull-up resistors (except the pull-up resistor on this I/O cell) are disabled.
SHS	O	N	OTP	**Show Cycle Strobe (active low)**— Strobes low when data is valid.

Table 10. FLEX Signals (MMC2080 Only)

Signal Name	Dir	N	I/O Cell	Description
LOBAT	In	Y	INHP	**Low Battery**—LOBAT is an input signal to indicate to the MMC2080 when external battery power is going low. (An external voltage sensing circuit is required.) Polarity is programmable.
EXTS[1:0]	In	Y	IOHP	**External Symbol** —EXTS 1 is the MSB of the current FLEX symbol. EXTS0 is the LSB of the current FLEX symbol. These pins are used when demodulation is being performed externally.
CLKOUT*	O	Y	OTP	**Clock Output**—CLKOUT is programmable as a 38.4 or 40 kHz clock output (derived from oscillator).
SYMCLK	O	Y	OTP	**Recovered Symbol Clock**—Data is synchronized to the internal clock, and this recovered clock output enhances lock-on capability by reducing jitter from cable-induced noise.
S[7:1]	O	Y	OTP	**Control Lines 1–7**—These signals are the seven additional receiver control lines. Selectable polarity.
S0/IFIN	I/O	Y	IOHP	**S0—**This signal is a receiver control output line when the IDE bit is clear (that is, the internal demodulator is disabled). **IFIN—**This signal is a limited IF input when the IDE bit is set (that is, the internal demodulator is enabled).

Table 11. FSC/SPI1 Signals

Signal Name	Dir	N	I/O Cell	Description
MPE4/LOCK	I/O	Y	IOHPPH	**External Synthesizer Lock Input**—PIO when SPI1 is disabled
MPE3/MOSI	I/O	Y	IOHPPH	**Master-out / Slave-in**—PIO when SPI1 is disabled
MPE2/MISO	I/O	Y	IOHPPH	**Master-in / Slave-out**—PIO when SPI1 is disabled
MPE1/$\overline{SS}$	I/O	Y	IOHPPH	**Slave Select** (selectable polarity)—PIO when SPI1 is disabled
MPE0/SCLK	I/O	Y	IOHPPH	**Serial Clock**—PIO when SPI1 is disabled

Table 12. SCI Signals

Signal Name	Dir	N	I/O Cell	Description
MPC7/URXD	I/O	Y	IOHPPH	**Receive Data**—An input when used as URXD; otherwise a PIO
MPC6/UTXD	I/O	Y	IOHPPH	**Transmit Data**—An output when used as UTXD; otherwise a PIO
MPC5/$\overline{UCTS}$	I/O	Y	IOHPPH	**Clear-to-Send** (active low)—An input when used as $\overline{UCTS}$; otherwise a PIO
MPC4/$\overline{URTS}$	I/O	Y	IOHPPH	**Request-to-Send** (active low)—An output when used as $\overline{URTS}$; otherwise a PIO
UCLK	I/O	Y	IOHPPH	**UART Clock**

Table 13. Timer Signals

Signal Name	Dir	N	I/O Cell	Description
MPC3/TIC1	I/O	Y	IOHPPH	**Timer1 Input Capture**—An input when used as TIC1; otherwise a PIO
MPC2/TOC1	I/O	Y	IOHPPH	**Timer1 Output Capture**—An output when used as TOC1; otherwise a PIO
MPC1/TIC0	I/O	Y	IOHPPH	**Timer0 Input Capture**—An input when used as TIC0; otherwise a PIO
MPC0/TOC0	I/O	Y	IOHPPH	**Timer0 Output Capture**—An output when used as TOC0; otherwise a PIO

Table 14. Melody Generator Signal

Signal Name	Dir	N	I/O Cell	Description
MLDY	O	Y	OTP	**Melody Generator Waveform**

Table 15. Keypad Signals

Signal Name	Dir	N	I/O Cell	Description
MPB[7:4]/ ROW[3:0]	I/O	Y	IOHPPH	**Row Detect**—Inputs when used as row detect; otherwise a PIO
MPB[3:0]/ COL[3:0]	I/O	Y	IOHPPH	**Column Select**—Open-drain outputs when used as column select; otherwise a PIO

Table 16. MPIO Signals

Signal Name	Dir	N	I/O Cell	Description
MPA[5:0]	I/O	Y	SWIOP	These bits can be individually programmed as input (with selectable pull-up resistor), output (with selectable drive strength), or external interrupt (with selectable assertion level). Each GPIO input pin is latched at the beginning of a read cycle.
Other pins when configured as PIO	I/O	Y	IOHPPH	These bits can be individually programmed as input (with selectable pull-up resistor) or output (with selectable drive strength). Each MPIO input pin is latched at the beginning of a read cycle.

Table 17. SIM Signals

Signal Name	Dir	N	I/O Cell	Description
RESET	I	Y	INHP	**External Reset** (active low)
RSTOUT	O	Y	OTP	**Reset Output** (active low)

Table 18. JTAG/OnCE™ Signals

Signal Name	Dir	N	I/O Cell	Description
TMS	I	Y	INHPP	**Test Mode Select**—Pull-up resistor always enabled
TCK	I	Y	INHPP	**Test Clock**—Pull-up resistor always enabled
TDI	I	Y	INHPP	**Test Data In**—Pull-up resistor always enabled
TDO	O	Y	OTP	**Test Data Out**
$\overline{\text{TRST}}$	I	Y	INHP	**TAP Reset** (active low)
$\overline{\text{DE}}$	I/O	Y	IOHPPH	**Debug Enable** (open drain, active low)

Table 19. Clock and Power

Signal Name	N	I/O Cell	Description
EXTAL	Y	AIN	Oscillator circuit input—external 76.8 kHz crystal
XTAL	Y	AOT	Oscillator circuit output
CXFC	Y	AIN	PLL filter capacitor
V_{dd}Core (5)	Y	Power	Core power
V_{ss}Core(5)	Y	Power	Core ground
V_{dd}IO (11)	Y	Power	I/O pad power
V_{ss}IO (11)	Y	Power	I/O pad ground
V_{dd}OSC	Y	Power	Oscillator power
V_{ss}OSC	Y	Power	Oscillator ground
V_{dd}PLL	Y	Power	PLL power
V_{ss}PLL	Y	Power	PLL ground

Table 20. Arbitration Signals

Signal Name	Dir	N	I/O Cell	Description
$\overline{\text{BREQ}}$	I	Y	INHPP	**Arbitration Request** (active low)—Request mastership of the internal system bus; pull-up resistor always enabled
$\overline{\text{BGNT}}$	O	Y	OTP	**Arbitration Grant** (active low)—Indicates system bus is granted to external master

Part 3 Specifications

3.1 General Characteristics

The MMC2080/2075 specifications are preliminary, from design simulations, and may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published upon the completion of full characterization and device qualifications.

3.2 Maximum Ratings

WARNING:

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either Vss or Vdd).

NOTE:

In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst-case variation of process parameter values in one direction. The minimum specification is calculated using the worst-case variation for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification will never occur in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 21. DC Absolute Maximum Operating Conditions

Characteristics	Symbol	Min	Typ	Max	Units
Supply (All)	Vdd	1.8	3.0	3.6	V
Input Voltage Range	V_I				V
Input Clamp Current (V_1<0 or V_1>QVDDH)	I_I				mA
Output Clamp Current (V_1<0 or V_1>QVDDH)	I_O				mA
Storage Temperature Range					^oC

Remaining specification information to be provided.

Part 4 Pin-out and Package Information

This section provides information about the available packages for this product. The MMC2080/2075 is available in a 144-pin Ball Grid Array (BGA) package. A 208-pin Pin Grid Array (PGA) is produced for engineering use only. Contact the factory for availability.

4.1 BGA Details

The MMC2080/2075 is offered in the JEDEC-standard, Mold Array Process (MAP), 12 mm x 12 mm BGA with 0.8 mm ball pitch (0.4 mm small solder balls). Refer to Figure 8 for the package drawings and dimensions.

4.1.1 BGA Package Mechanical Drawings

The mechanical drawings for the 144-pin Ball Grid Array package are shown in Figure 8.

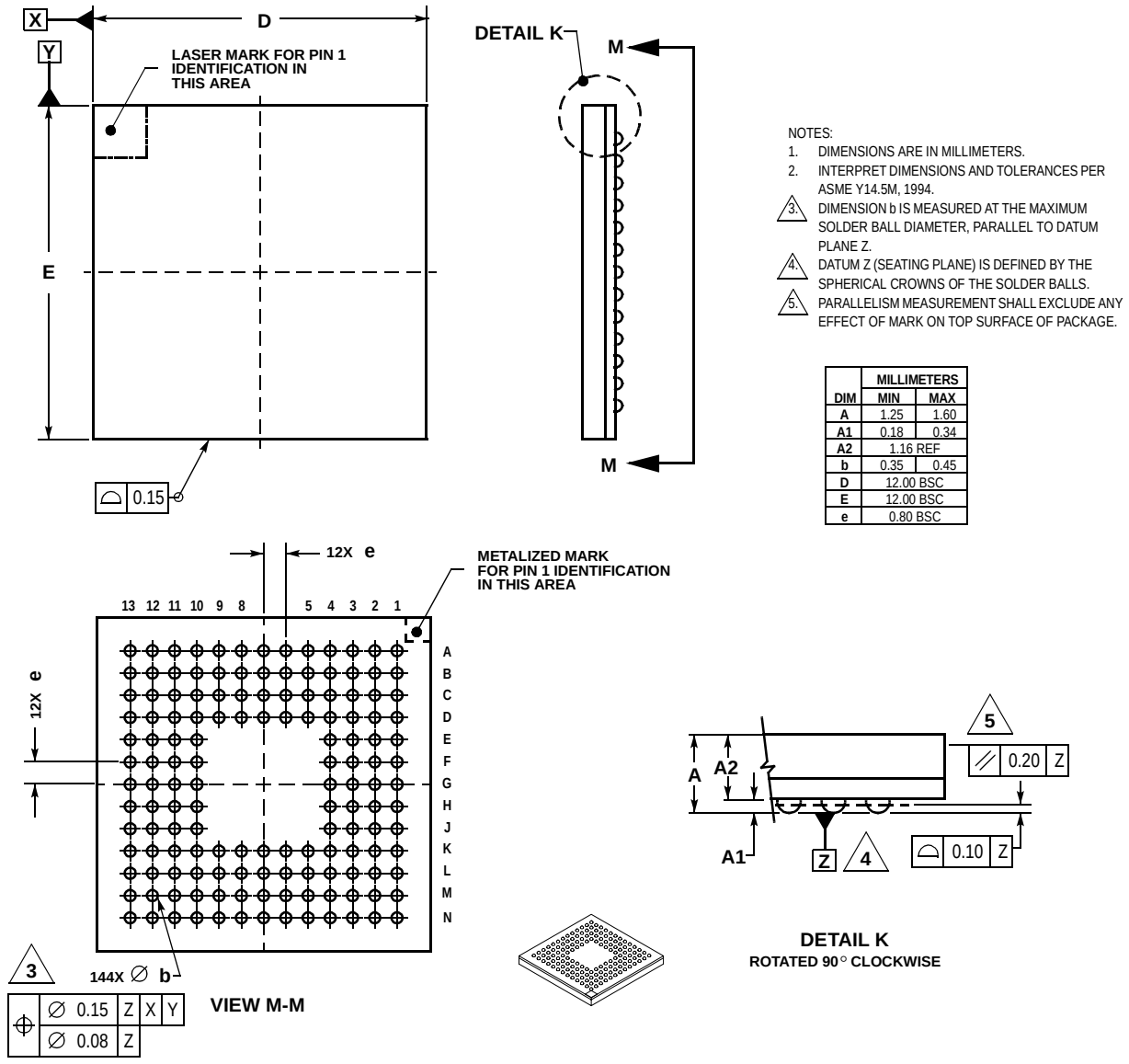


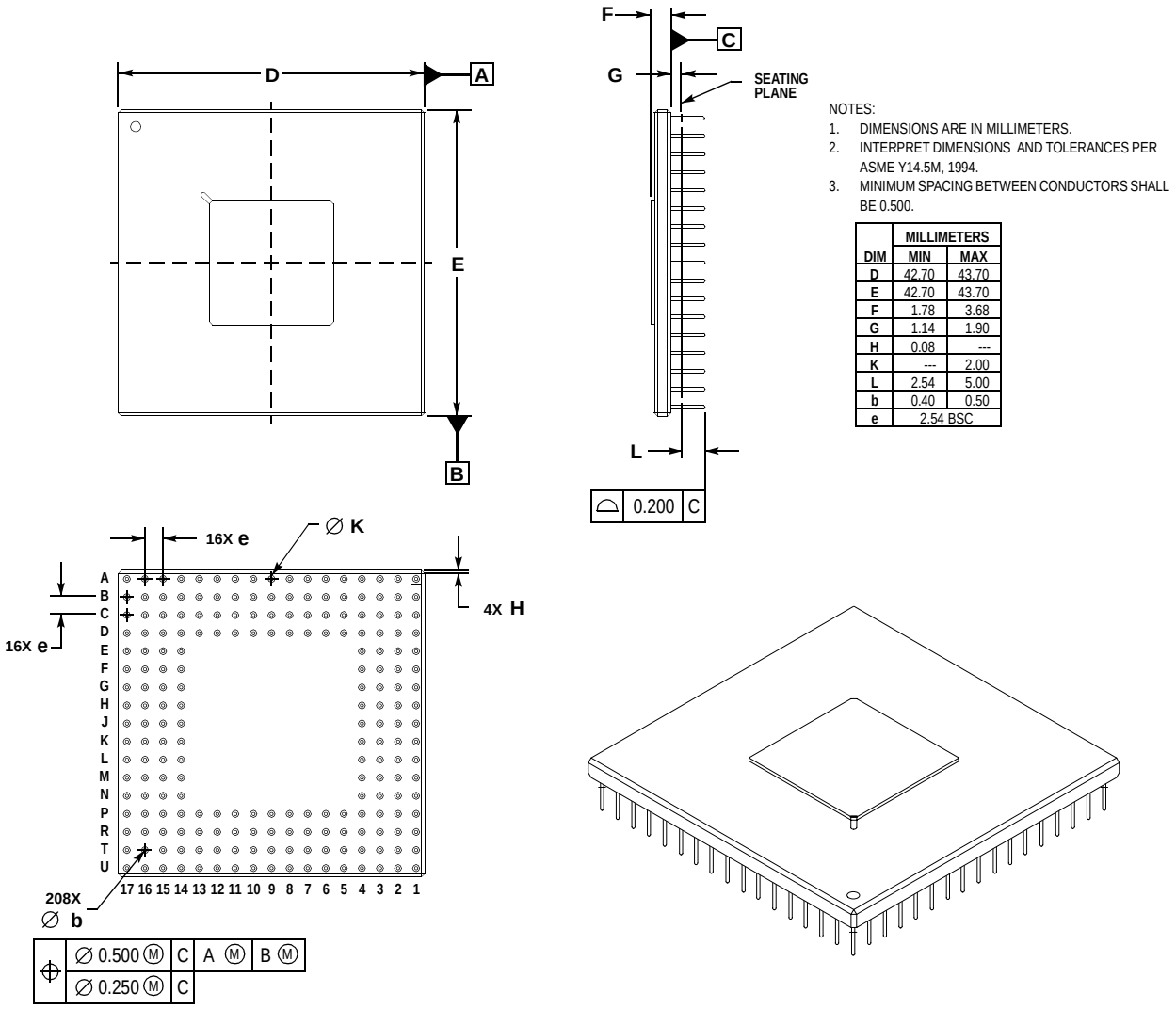
Figure 8. MMC2080/2075 BGA Mechanical Drawings

4.2 PGA Details

The MMC2080/2075 is also offered in a ceramic, 43 mm x 43 mm PGA for engineering use only. Contact the factory for availability. Refer to Figure 9 for the package drawings and dimensions.

4.2.1 PGA Package Mechanical Drawings

The mechanical drawings for the 208-pin Ball Grid PGA package are shown in Figure 9.



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. MINIMUM SPACING BETWEEN CONDUCTORS SHALL BE 0.500.

	MILLIMETERS	
DIM	MIN	MAX
D	42.70	43.70
E	42.70	43.70
F	1.78	3.68
G	1.14	1.90
H	0.08	---
K	---	2.00
L	2.54	5.00
b	0.40	0.50
e	2.54 BSC	

Figure 9. MMC2080/2075 PGA Mechanical Drawings

4.3 Ordering Drawings

Complete mechanical information regarding MMC2080/2075 packaging is available by facsimile through Motorola's MFAX™ system. Call the following number to obtain information by facsimile:

(602) 244-6591

The MFAX automated system requests the following information:

- The receiving facsimile telephone number, including area code or country code
- The caller's personal identification number (PIN)

NOTE:

For first-time callers, the system provides instructions for setting up a PIN, which requires the entry of a name and telephone number.

- The type of information requested:
  - — Instructions for using the system
  - — A literature order form
  - — Specific-part technical information or datasheets
  - — Other information described by the system messages

A total of three documents may be ordered per call.

The MMC2080/2075 144-pin BGA package mechanical drawing is referenced as Case 1248A-01 Rev. 0.

The MMC2080/2075 208-pin BGA package mechanical drawing is referenced as Case 1297-01 Rev. 0.

Part 5 Design Considerations

5.1 Heat Dissipation

An estimate of the MMC2080/2075 chip junction temperature, T_J, in °C can be obtained from the following equation.

$$T_J = T_A + (P_D \times R_{\theta JA})$$

Where:

T_A = ambient temperature °C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance, as follows:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or otherwise change the thermal dissipation capability of the area surrounding the device on a printed circuit board. This model is most useful for ceramic packages with heat sinks; ninety percent of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the printed circuit board, analysis of the device's thermal performance may need the additional modeling capability of a system-level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the printed circuit board to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system-level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages:

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case (T_T) is determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation $(T_J - T_T)/P_D$.

As noted previously, the junction-to-case thermal resistances quoted in this document are determined using the first definition. From a practical standpoint, this value is also suitable for determining the junction

temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than the actual temperature. Hence, the new thermal metric, thermal characterization parameter or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

NOTE:

Section 3, “Specifications,” on page 28 of this document contains the package thermal values for this chip.

5.2 Electrical Design Considerations

WARNING:

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either Vss or V_{DD}).

Use the following list of recommendations to assure correct operation:

- Provide a low-impedance path from the board power supply to each Vdd pin on the MMC2080/2075 and from the board ground to each Vss pin.
- Use at least four 0.1 μF bypass capacitors positioned as close as possible to the four sides of the package to connect the Vdd power source to Vss.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip Vdd and Vss pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer printed circuit board (PCB) with two inner layers for Vdd and Vss.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the Vdd and Vss circuits.
- All inputs must be terminated (that is, not allowed to float) using CMOS levels.

Take special care to minimize noise levels on the PLL supply pins (both Vdd and Vss).

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