



CYPRESS

CY7C385A CY7C386A

Very High Speed 4K (12K) Gate CMOS FPGA

Features

- **Very high speed**
 - Loadable counter frequencies greater than 100 MHz
 - Chip-to-chip operating frequencies up to 85 MHz
 - Input + logic cell + output delays under 7 ns
- **Unparalleled FPGA performance** for counters, data path, state machines, arithmetic, and random logic
- **High usable density**
 - 16 x 24 array of 384 logic cells provides 12,000 total available gates
 - 4,000 typically usable "gate array" gates in 84-pin PLCC/CLCC, 100-pin and 144-pin TQFP, 145-pin CPGA, and 160-pin CQFP packages
- **Low power, high output drive**
 - Standby current typically 2 mA
 - 16-bit counter operating at 100 MHz consumes 50 mA
 - Minimum I_{OL} and I_{OH} of 8 mA
- **Flexible logic cell architecture**
 - Wide fan-in (up to 14 input gates)
 - Multiple outputs in each cell
 - Very low cell propagation delay (1.7 ns)
- **Powerful design tools—Warp3™**
 - Designs entered in VHDL, schematics, or both

- Fast, fully automatic place and route
- Waveform simulation with back annotated net delays
- PC and workstation platforms
- **Robust routing resources**
 - Fully automatic place and route of designs using up to 100 percent of logic resources
 - No hand routing required
- 88 (7C385A) to 122 (7C386A) bidirectional input/output pins
- 6 dedicated input/high-drive pins
- 2 clock/dedicated input pins with fan-out-independent, low-skew nets
 - Clock skew < 1 ns
- **Input hysteresis provides high noise immunity**
- **Thorough testability**
 - Built-in scan path permits 100 percent factory testing of logic and I/O cells
 - Automatic Test Vector Generation (ATVG) software supports user testing after programming
- 0.65μ CMOS process with ViaLink™ programming technology
 - High-speed metal-to-metal link
 - Non-volatile antifuse technology
- 100-pin TQFP is pin compatible with the 1K (CY7C381A/2A) and the 2K (CY7C383A/4A) FPGAs

Functional Description

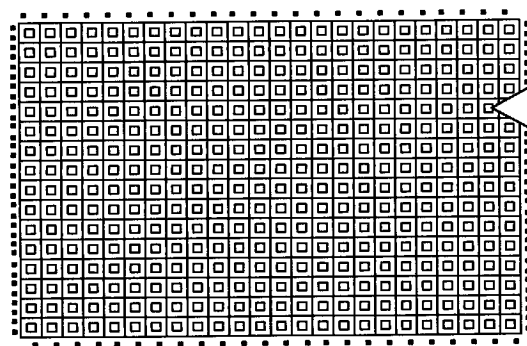
The CY7C385A and CY7C386A are very high speed CMOS user-programmable ASIC (pASIC™) devices. The 384 logic cell field-programmable gate array (FPGA) offers 4,000 typically usable "gate array" gates. This is equivalent to 12,000 EPLD or LCA gates. The CY7C385A is available in a 84-pin PLCC and CPGA and the 100-pin TQFP. The CY7C386A is available in 144-pin TQFP and CPGA packages, and a 160-pin CQFP package.

Low-impedance, metal-to-metal ViaLink interconnect technology provides non-volatile custom logic capable of operating at speeds above 150 MHz with input and output delays under 3 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

Designs are entered into the CY7C385A and CY7C386A using Cypress Warp3 software or one of several third-party tools. Warp3 is a sophisticated CAE package that features schematic entry, waveform-based timing simulation, and VHDL design synthesis. The CY7C385A and CY7C386A feature ample on-chip routing channels for fast, fully automatic place and route of high gate utilization designs.

For detailed information about the pASIC380 architecture, see the pASIC380 Family datasheet.

Logic Block Diagram

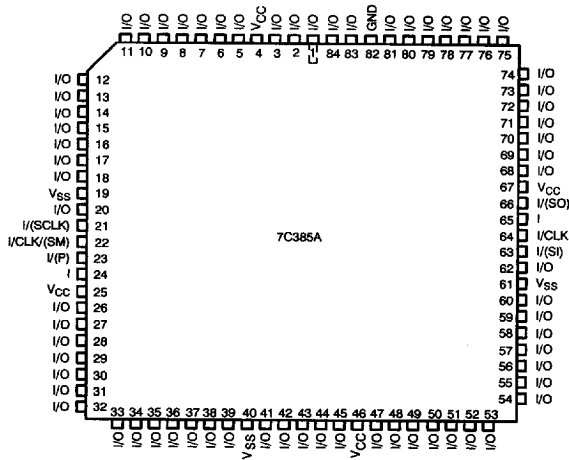


- I/O/HIGH-DRIVE INPUT/
CLOCK CELLS

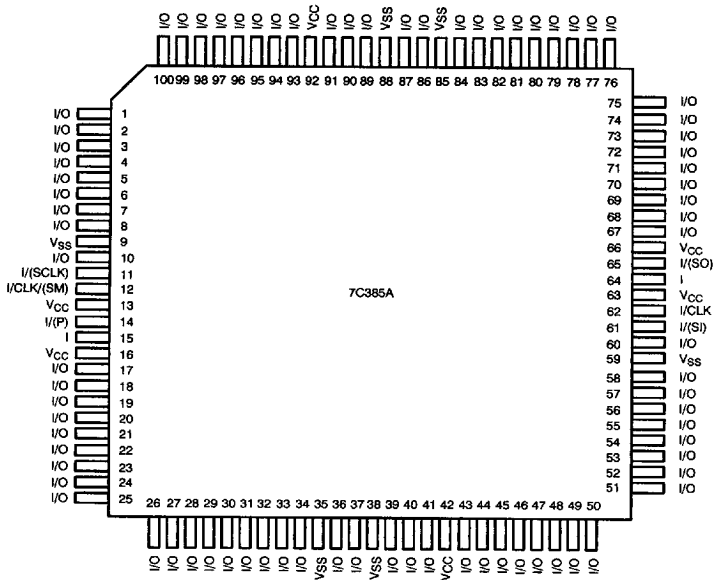
84 and 144 PINS, 114 I/O CELLS, 6 INPUT HIGH DRIVE CELLS, 2 INPUT/CLK (HIGH DRIVE) CELLS

7C385A-1

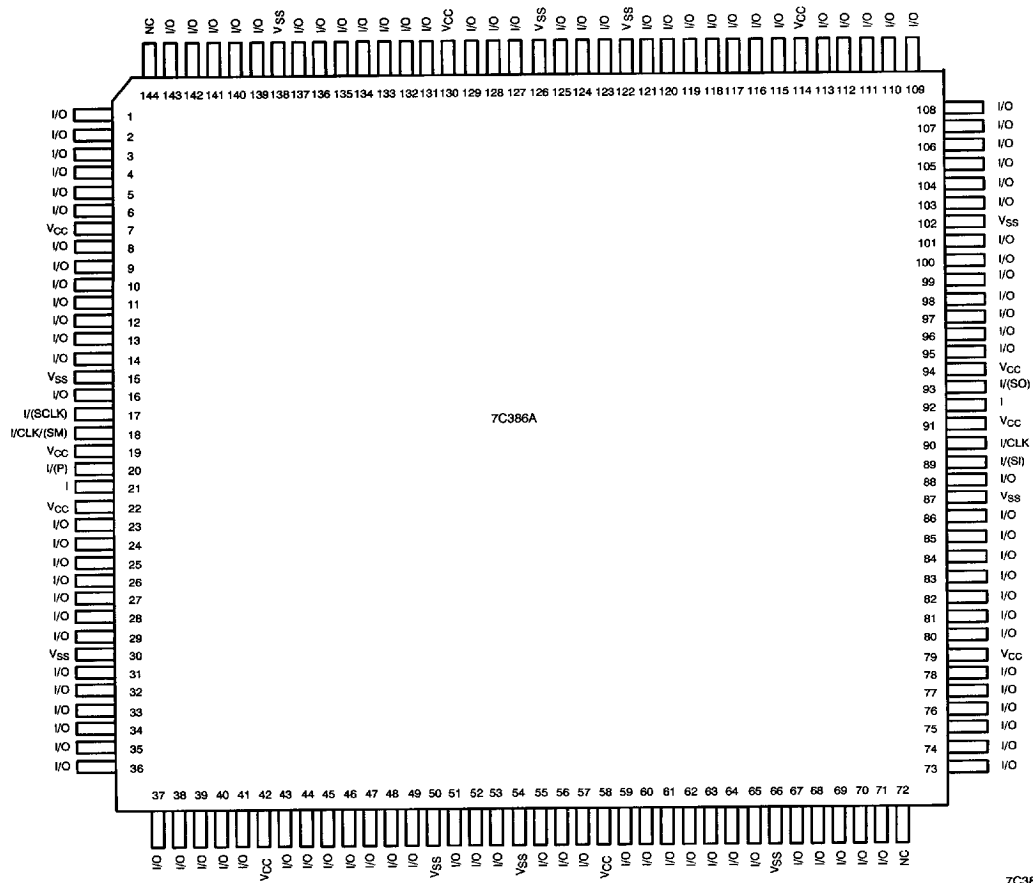
ViaLink and pASIC are trademarks of QuickLogic Corporation.
Warp3 is a trademark of Cypress Semiconductor Corporation.

Pin Configurations
**PLCC/CLCC
Top View**


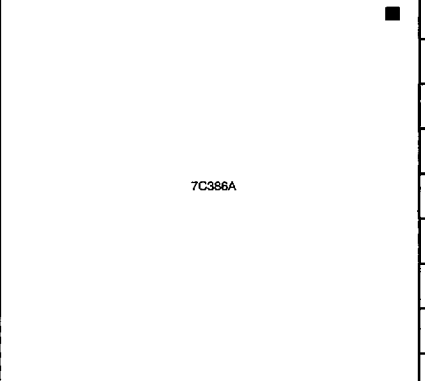
7C385A-2

**TQFP
Top View**


7C385A-3

Pin Configurations (continued)
TQFP
Top View


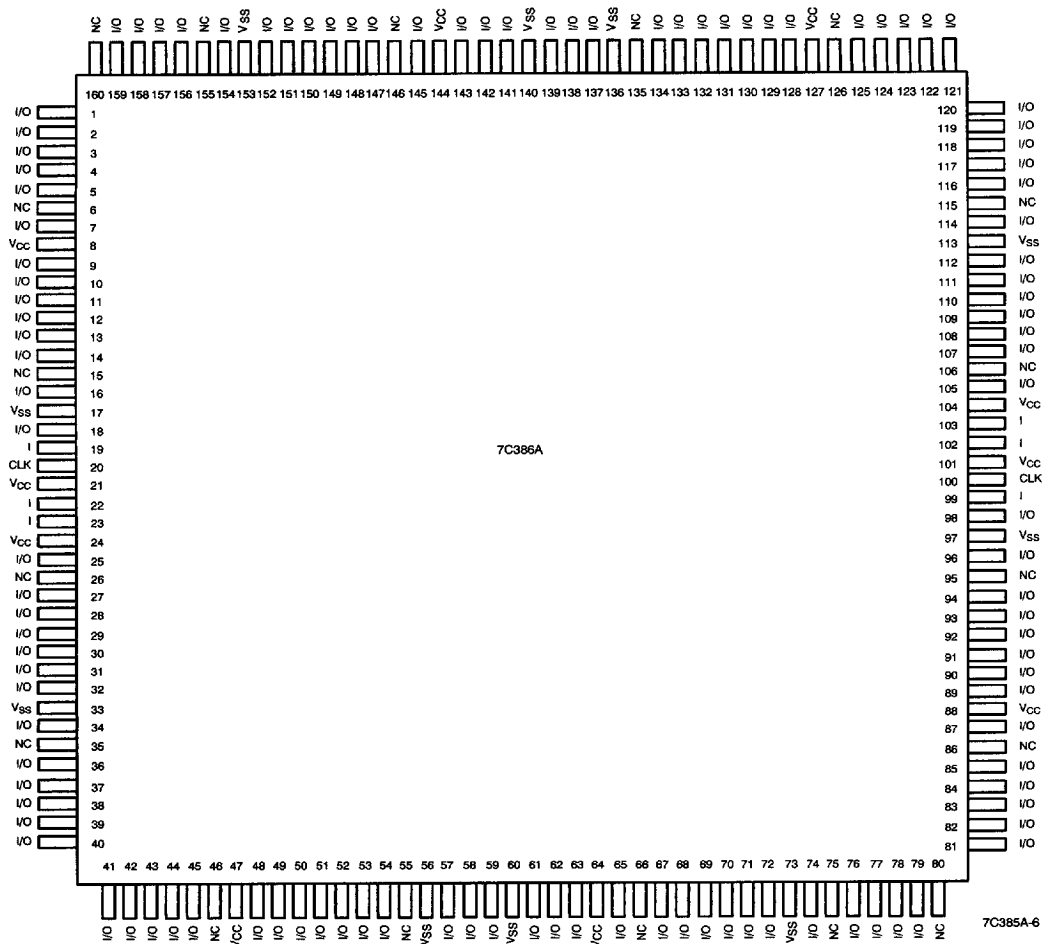
Pin Configurations (continued)
**CPGA
Bottom View**

R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	1
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC	I/O	2
I/O	I/O	V _{SS}	I/O	V _{CC}	I/O	V _{SS}	I/O	V _{CC}	I/O	V _{SS}	I/O	V _{CC}	I/O	I/O	3
I/O	I/O	I/O	 7C386A									I/O	I/O	I/O	4
I/O	I/O	V _{CC}										V _{SS}	I/O	I/O	5
I/O	I/O	I/O										I/O	I/O	I/O	6
I	I/(SO)	V _{SS}										V _{CC}	I/O	I/O	7
I/O	I/(SI)	I/CLK										I/CLK (SM)	I/(SCLK)	I/O	8
I/O	I/O	V _{CC}										V _{SS}	I	I/(P)	9
I/O	I/O	I/O										I/O	I/O	I/O	10
I/O	I/O	V _{SS}										V _{CC}	I/O	I/O	11
I/O	I/O	I/O										I/O	I/O	I/O	12
I/O	I/O	V _{CC}	I/O	V _{SS}	I/O	V _{CC}	I/O	V _{SS}	I/O	V _{CC}	I/O	V _{SS}	I/O	I/O	13
I/O	NC	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	14
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	15

7C385A-5

Pin Configurations (continued)

QFP
Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	
Ceramic	-65°C to +150°C
Plastic	-40°C to +125°C
Lead Temperature	300°C
Supply Voltage	-0.5V to +7.0V
Input Voltage	-0.5V to $V_{CC} + 0.5V$
ESD Pad Protection	$\pm 2000\text{ V}$
DC Input Voltage	-0.5V to 7.0V

Latch-Up Current $\pm 200\text{ mA}$

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V $\pm 5\%$
Industrial	-40°C to +85°C	5V $\pm 10\%$
Military	-55°C to +125°C	5V $\pm 10\%$

Delay Factor (K)

Speed Grade	Military		Industrial		Commercial	
	Min.	Max.	Min.	Max.	Min.	Max.
-0	0.39	1.82	0.4	1.67	0.46	1.55
-1	0.39	1.56	0.4	1.43	0.46	1.33
-2			0.4	1.35	0.46	1.25

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -4.0\text{ mA}$	3.7		V
		$I_{OH} = -8.0\text{ mA}$	2.4		V
		$I_{OH} = -10.0\text{ }\mu\text{A}$	$V_{CC} - 0.1$		V
V_{OL}	Output LOW Voltage	$I_{OL} = 8.0\text{ mA}$ Military/Industrial		0.4	V
		$I_{OL} = 12\text{ mA}$ Commercial			V
		$I_{OL} = 10.0\text{ }\mu\text{A}$		0.1	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_I	Input Leakage Current	$V_{IN} = V_{CC}$ or V_{SS}	-10	+10	μA
I_{OZ}	Three-State Output Leakage Current	$V_{IN} = V_{CC}$ or V_{SS}	-10	+10	μA
I_{OS}	Output Short Circuit Current	$V_{OUT} = V_{SS}$	-10	-80	mA
		$V_{OUT} = V_{CC}$	30	140	mA
I_{CC}	Standby Supply Current	$V_{IN}, V_{IO} = V_{CC}$ or V_{SS}		10	mA

Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance ^[1]	$T_A = 25^\circ\text{C}, f = 1\text{ MHz},$ $V_{CC} = 5.0\text{V}$	10	pF
C_{OUT}	Output Capacitance		20	pF

Notes:

1. $C_I = 45\text{ pF}$ max. on I(SI) and I(P).

Switching Characteristics Over the Operating Range

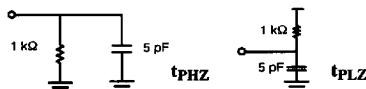
Parameter	Description	Propagation Delays ^[2] with Fanout of					Unit
		1	2	3	4	8	
LOGIC CELLS							
t _{PD}	Combinatorial Delay ^[3]	1.7	2.2	2.6	3.2	5.3	ns
t _{SU}	Set-Up Time ^[3]	2.1	2.1	2.1	2.1	2.1	ns
t _H	Hold Time	0.0	0.0	0.0	0.0	0.0	ns
t _{CLK}	Clock to Q Delay	1.0	1.5	1.9	2.6	4.7	ns
t _{CWHI}	Clock HIGH Time	2.0	2.0	2.0	2.0	2.0	ns
t _{CWLO}	Clock LOW Time	2.0	2.0	2.0	2.0	2.0	ns
t _{SET}	Set Delay	1.7	2.2	2.6	3.2	5.3	ns
t _{RESET}	Reset Delay	1.5	1.9	2.2	2.7	4.4	ns
t _{SW}	Set Width	1.9	1.9	1.9	1.9	1.9	ns
t _{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8	ns

Parameter	Description	Propagation Delays ^[2]						Unit
		1	2	3	4	8	12	
INPUT CELLS								
t _{IN}	Input Delay (HIGH Drive)	2.8	2.9	3.0	3.1	4.0	5.3	ns
t _{INI}	Input, Inverting Delay (HIGH Drive)	3.0	3.1	3.2	3.3	4.1	5.7	ns
t _{IO}	Input Delay (Bidirectional Pad)	1.4	1.9	2.2	2.2	4.7	6.5	ns
t _{GCK}	Clock Buffer Delay ^[4]	2.7	2.8	2.9	3.0	3.1	3.3	ns
t _{GCKHI}	Clock Buffer Min. HIGH ^[4]	2.0	2.0	2.0	2.0	2.0	2.0	ns
t _{GCKLO}	Clock Buffer Min. LOW ^[4]	2.0	2.0	2.0	2.0	2.0	2.0	ns

Parameter	Description	Propagation Delays ^[2] with Output Load Capacitance (pF) of					Unit
		30	50	75	100	150	
OUTPUT CELLS							
t _{OUTLH}	Output Delay LOW to HIGH	2.7	3.4	4.2	5.0	6.7	ns
t _{OUTHL}	Output Delay HIGH to LOW	2.8	3.7	4.7	5.6	7.6	ns
t _{PZH}	Output Delay Three-State to HIGH	4.0	4.9	6.1	7.3	9.7	ns
t _{PZL}	Output Delay Three-State to LOW	3.6	4.2	5.0	5.8	7.3	ns
t _{PHZ}	Output Delay HIGH to Three-State ^[5]	2.9					ns
t _{PLZ}	Output Delay LOW to Three-State ^[5]	3.3					ns

Notes:

- Worst-case propagation delay times over process variation at V_{CC} = 5.0V and T_A = 25°C. Multiply by the appropriate delay factor, K_d, for speed grade to get worst-case parameters over full V_{CC} and temperature range as specified in the operating range. All inputs are TTL with 3-ns linear transition time between 0 and 3 volts.
- These limits are derived from worst-case values for a representative selection of the slowest paths through the pASIC logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.
- Clock buffer fanout refers to the maximum number of flip-flops per half column. The number of half columns used does not affect clock buffer delay.
- The following loads are used for t_{PHZ}:

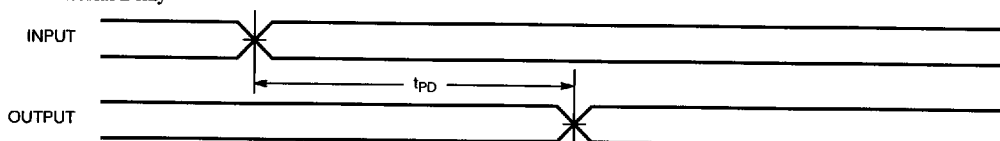


High Drive Buffer

Parameter	Description	# High Drives Wired Together	Propagation Delays ^[2] with Fanout of					Unit
			12	24	48	72	96	
t_{IN}	High Drive Input Delay	1	5.3	6.7				ns
		2		4.5	6.6			ns
		3			5.3	6.2	7.2	ns
		4				5.4	6.2	ns
t_{INI}	High Drive Input, Inverting Delay	1	5.7	7.2				ns
		2		4.6	6.8			ns
		3			5.5	6.4	7.4	ns
		4				5.6	6.4	ns

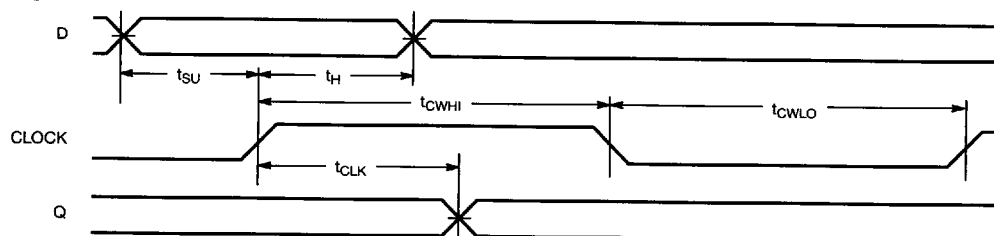
Switching Waveforms

Combinatorial Delay



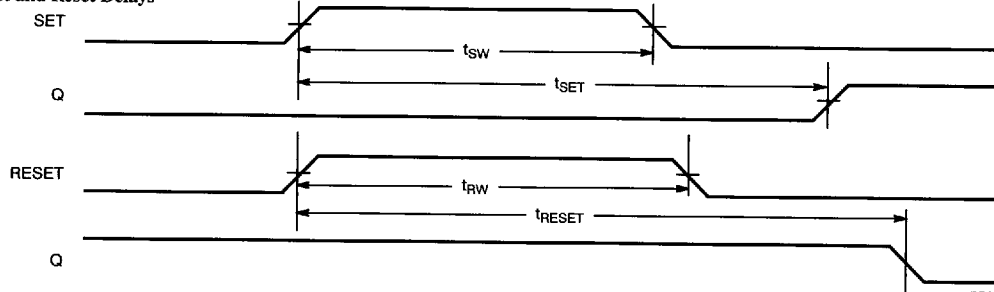
7C385A-7

Set-Up and Hold Times



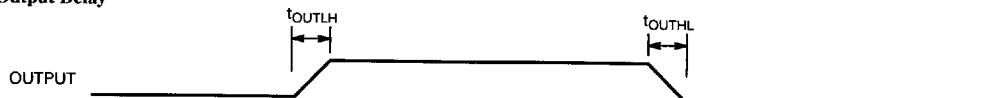
7C385A-8

Set and Reset Delays



7C385A-9

Output Delay



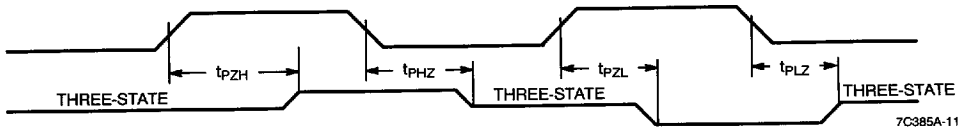
7C385A-10

Switching Waveforms (continued)

Three-State Delay

OUTPUT
BUFFER
ENABLE

OUTPUT

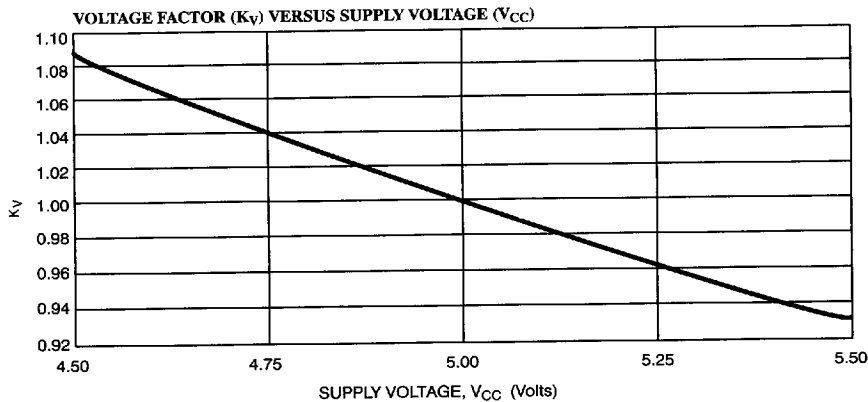


7C385A-11

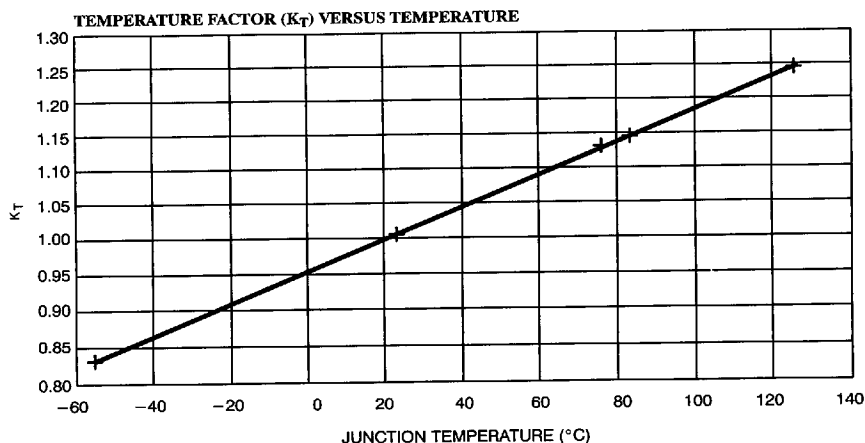
Typical AC Characteristics

Propagation delays depend on routing, fanout, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst-case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K , as specified by the speed grade in the Delay

Factor table. The effects of voltage and temperature variation are illustrated in the graphs below. *Warp3* incorporates datasheet AC Characteristics into the design database for pre-place-and-route simulations. The *Warp3* Delay Modeler extracts specific timing parameters for precise simulation results following place and route.

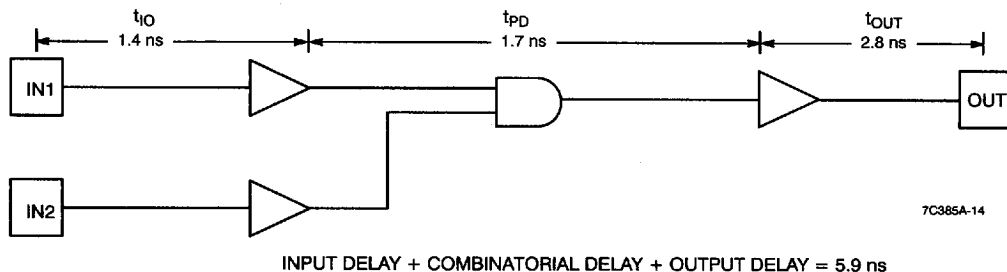
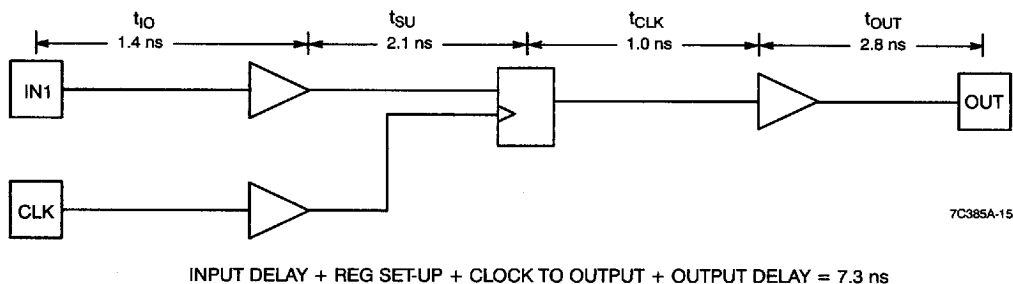


7C385A-12



7C385A-13

* $\theta_{JA} = 45^{\circ}\text{C/WATT}$ FOR PLCC

Combinatorial Delay Example (Load = 30 pF)

Sequential Delay Example (Load = 30 pF)

Ordering Information

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C385A-2AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C385A-2JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C385A-2AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C385A-2JI	J83	84-Lead Plastic Leaded Chip Carrier	
1	CY7C385A-1AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C385A-1JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C385A-1AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C385A-1JI	J83	84-Lead Plastic Leaded Chip Carrier	
0	CY7C385A-0AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C385A-0JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C385A-0AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C385A-0JI	J83	84-Lead Plastic Leaded Chip Carrier	

Ordering Information (continued)

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C386A-2AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C386A-2GC	G145	145-Pin Grid Array (Cavity Up)	
	CY7C386A-2UC	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	
	CY7C386A-2AI	A144	144-Pin Thin Quad Flat Pack	Industrial
	CY7C386A-2GI	G145	145-Pin Grid Array (Cavity Up)	
	CY7C386A-2UI	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	
1	CY7C386A-1AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C386A-1GC	G145	145-Pin Grid Array (Cavity Up)	
	CY7C386A-1UC	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	
	CY7C386A-1AI	A144	144-Pin Thin Quad Flat Pack	Industrial
	CY7C386A-1GI	G145	145-Pin Grid Array (Cavity Up)	
	CY7C386A-1UI	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	
	CY7C386A-1GMB	G145	145-Pin Grid Array (Cavity Up)	Military
	CY7C386A-1UMB	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	
0	CY7C386A-0AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C386A-0GC	G145	145-Pin Grid Array (Cavity Up)	
	CY7C386A-0UC	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	
	CY7C386A-0AI	A144	144-Pin Thin Quad Flat Pack	Industrial
	CY7C386A-0GI	G145	145-Pin Grid Array (Cavity Up)	
	CY7C386A-0UI	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	
	CY7C386A-0GMB	G145	145-Pin Grid Array (Cavity Up)	Military
	CY7C386A-0UMB	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	

Shaded area contains advanced information.

Military Specifications
Group A Subgroup Testing
DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC1}	1, 2, 3

Document #: 38-00209-C