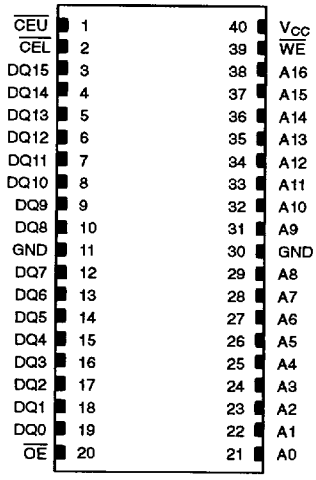
DALLAS SEMICONDUCTOR

DS1758Y
3–Volt Partitionable 128K x 16 NV SRAM

FEATURES

- 10 year minimum data retention in the absence of external power
- Data is automatically write protected during power loss
- Write protects selected blocks of memory when programmed
- Separate upper–byte and lower–byte chip selection inputs
- Low–power CMOS
- Unlimited write cycles
- Read and write access times as fast as 150 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% V_{CC} operating range
- Optional industrial temperature range of –40°C to 85°C (designated IND)

PIN ASSIGNMENT



40–PIN ENCAPSULATED PACKAGE
740 MIL EXTENDED

PIN DESCRIPTION

A0–A16	–	Address Inputs
DQ0–DQ15	–	Data In/Data Out
$\overline{CEU}$	–	Chip Enable Upper Byte
$\overline{CEL}$	–	Chip Enable Lower Byte
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
V_{CC}	–	Power Supply
GND	–	Ground

DESCRIPTION

The DS1758 128K x 16 NV SRAMs are 2,097,152 bit, fully static, nonvolatile SRAMs, organized as 131,072 words by 16 bits. Each NV SRAM has a self contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out–of–tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. In addition, the DS1758 has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt programs or important data. DS1758 devices can be used in place of solutions which build nonvolatile 128K x 16 memory by utilizing a variety of discrete components. There is no limit on the number of write cycles that can be executed, and no additional support circuitry is required for microprocessor interfacing.

READ MODE

The DS1758 devices execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high), either/both of $\overline{CEU}$ or $\overline{CEL}$ (Chip Enables) are active (low) and $\overline{OE}$ (Output Enable) is active low. The unique address specified by the 17 address inputs (A0–A16) defines which of the 131,072 words of data is to be accessed. The status of $\overline{CEU}$ and $\overline{CEL}$ determines whether all or part of the addressed word is accessed. If $\overline{CEU}$ is active with $\overline{CEL}$ inactive, then only the upper byte of the addressed word is accessed. If $\overline{CEU}$ is inactive with $\overline{CEL}$ active, then only the lower byte of the addressed word is accessed. If both the $\overline{CEU}$ and $\overline{CEL}$ inputs are active (low), then the entire 16 bit word is accessed. Valid data will be available to the 16 data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CEU}$, $\overline{CEL}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$, $\overline{CEU}$, and $\overline{CEL}$ access times are not satisfied, then data access must be measured from the later occuring signal, and the limiting parameter is either t_{CO} for $\overline{CEU}$, $\overline{CEL}$, or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1758 devices execute a write cycle whenever $\overline{WE}$ and either/both of $\overline{CEU}$ or $\overline{CEL}$ are active (low) after address inputs are stable. The unique address specified by the 17 address inputs (A0–A16) defines which of the 131,072 words of data is accessed. The status of $\overline{CEU}$ and $\overline{CEL}$ determines whether all or part of the addressed word is accessed. If $\overline{CEU}$ is active with $\overline{CEL}$ inactive, then only the upper byte of the addressed word is accessed. If $\overline{CEU}$ is inactive with $\overline{CEL}$ active, then only the lower byte of the addressed word is accessed. If both the $\overline{CEU}$ and $\overline{CEL}$ inputs are active (low), then the entire 16–bit word is accessed. The write cycle is terminated by the earlier rising edge of $\overline{CEU}$ and/or $\overline{CEL}$, or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CEU}$ and/or $\overline{CEL}$, and $\overline{OE}$ active) then $\overline{WE}$ will disable outputs in t_{ODW} from its falling edge.

READ/WRITE FUNCTION Table 1

$\overline{OE}$	$\overline{WE}$	$\overline{CEL}$	$\overline{CEU}$	V_{CC} CURRENT	DQ0–DQ7	DQ8–DQ15	CYCLE PERFORMED
H	H	X	X	I_{CCO}	High–Z	High–Z	Output Disabled
L	H	L	L	I_{CCO}	Output	Output	Read Cycle
L	H	L	H		Output	High–Z	
L	H	H	L		High–Z	Output	
X	L	L	L	I_{CCO}	Input	Input	Write Cycle
X	L	L	H		Input	High–Z	
X	L	H	L		High–Z	Input	
X	X	H	H	I_{CCS}	High–Z	High–Z	Output Disabled

DATA RETENTION MODE

The DS1758Y provides full functional capability for V_{CC} greater than 2.7 volts, and write protects by 2.5 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs to the RAM become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 2.6 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 2.70 volts.

FRESHNESS SEAL

Each DS1758 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is applied and remains at a level of greater than V_{TP} first, the lithium energy source is enabled for battery backup operation.

PARTITION PROGRAMMING MODE

The register controlling the partitioning logic is selected by recognition of a specific binary pattern which is sent on address lines A13–A16. These address lines are the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles, using both $\overline{CEU}$ and $\overline{CEL}$, with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycles will load the partition register. Since there are 16 protectable partitions, the size of each partition is 128K/16 or 8K x 16. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycles as defined by A13 through A16 and shown in Table 2. A logical 1 in a bit location write protects the corresponding partition. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A14 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1758 devices to inhibit $\overline{WE}$ internally when A16 A15 A14 A13=0101. Note that while programming the partition register, data which is being accessed from the RAM should be ignored since the purpose of the 24 read cycles is to program the partition register, not to access data from RAM.

PATTERN MATCH TO WRITE PARTITION REGISTER Table 2

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A13	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A14	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A15	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A16	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

FIRST BITS ENTERED

LAST BITS ENTERED

PARTITION REGISTER MAPPING Table 3

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_{16} A_{15} A_{14} A_{13})
A13	BIT 21	PARTITION 0	0000
A14	BIT 21	PARTITION 1	0001
A15	BIT 21	PARTITION 2	0010
A16	BIT 21	PARTITION 3	0011
A13	BIT 22	PARTITION 4	0100
A14	BIT 22	PARTITION 5	0101
A15	BIT 22	PARTITION 6	0110
A16	BIT 22	PARTITION 7	0111
A13	BIT 23	PARTITION 8	1000
A14	BIT 23	PARTITION 9	1001
A15	BIT 23	PARTITION 10	1010
A16	BIT 23	PARTITION 11	1011
A13	BIT 24	PARTITION 12	1100
A14	BIT 24	PARTITION 13	1101
A15	BIT 24	PARTITION 14	1110
A16	BIT 24	PARTITION 15	1111

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C, –40°C to +85°C for IND parts
Storage Temperature	–40°C to +70°C, –40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1758Y Power Supply Voltage	V_{CC}	2.7	3.0	4.0	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.4	V	

DC ELECTRICAL CHARACTERISTICS

(t_A: See Note 10) (V_{CC}=2.7V to 3.6V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-2.0		+2.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.2V	I_{OH}	-0.5			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CEU}$, $\overline{CEL}$=2.2V	I_{CCS1}		4.0	8.0	mA	
Standby Current $\overline{CEU}$, $\overline{CEL}$ = V_{CC} - 0.5V	I_{CCS2}		2.0	3.0	mA	
Operating Current	I_{CCO}			80	mA	
Write Protection Voltage	V_{TP}	2.50	2.60	2.70	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		20	25	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(t_A: See Note 10) (V_{CC}=2.7V to 3.6V)

PARAMETER	SYMBOL	DS1758Y–150		DS1758Y–200		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	150		200		ns	
Access Time	t_{ACC}		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		50		50	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	150		200		ns	
Write Pulse Width	t_{WP}	120		150		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	10 10		10 10		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		50		50	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	60		80		ns	4
Data Hold Time	t_{DH1} t_{DH2}	10 10		10 10		ns ns	12 13

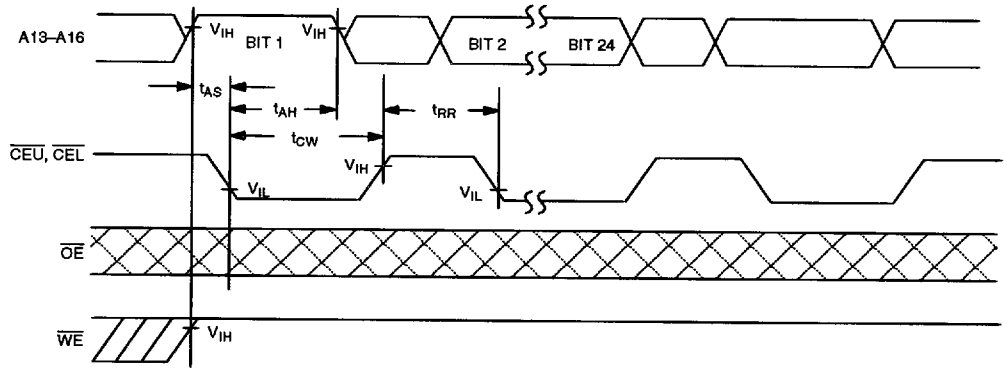
AC ELECTRICAL CHARACTERISTICS

(t_A: See Note 10) (V_{CCI}=2.7V to 3.6V)*

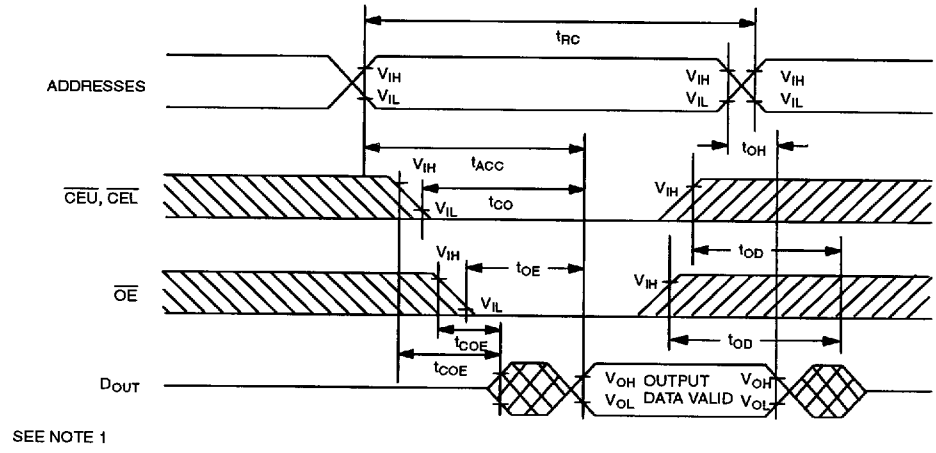
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	20			ns	
$\overline{CE}$ Pulse Width	t_{CW}	75			ns	

*For loading partition register

TIMING DIAGRAM: LOADING PARTITION REGISTER

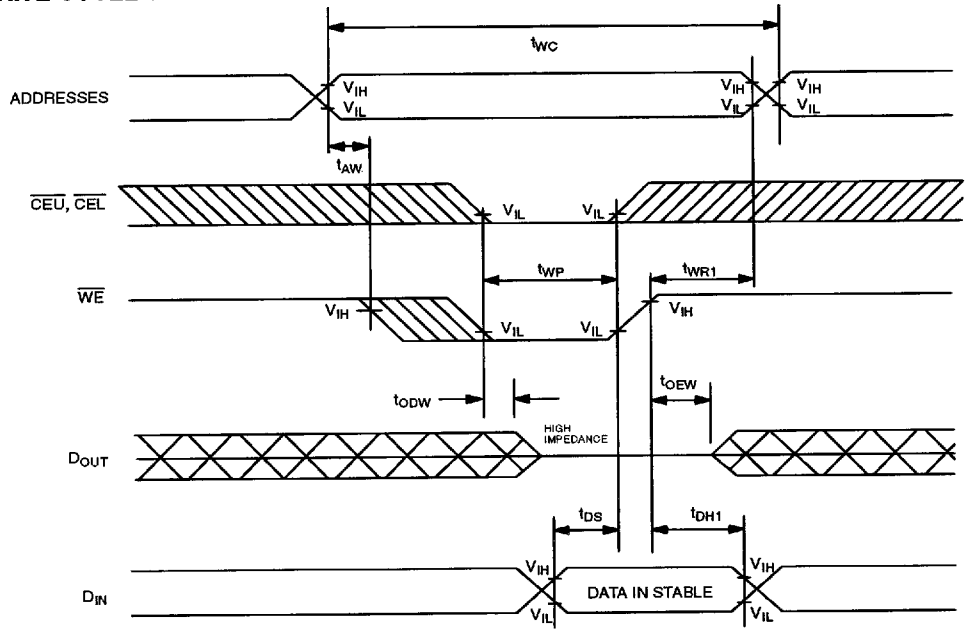


READ CYCLE



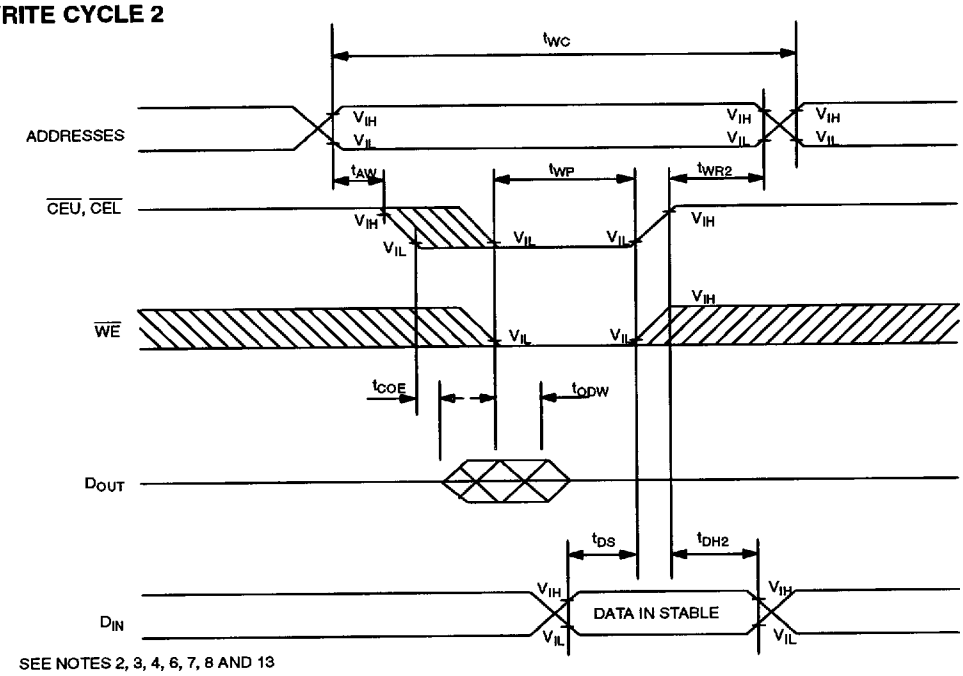
SEE NOTE 1

WRITE CYCLE 1



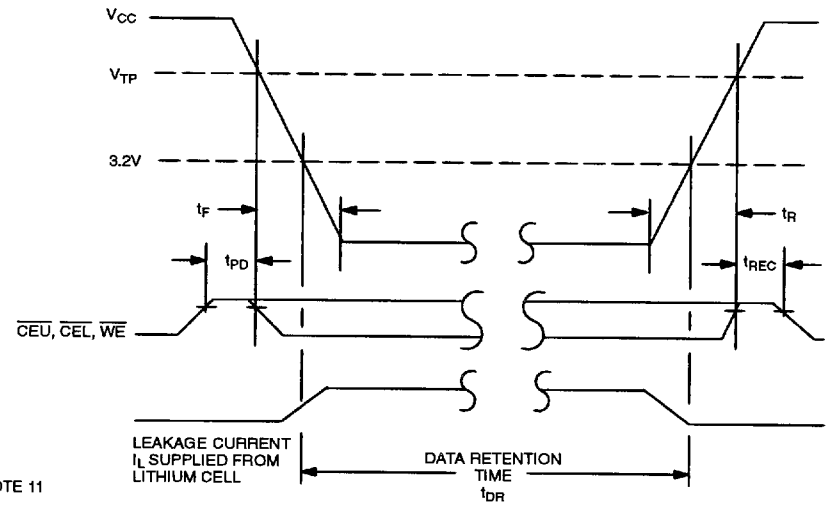
SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7, 8 AND 13

POWER-DOWN/POWER-UP CONDITION



SEE NOTE 11

POWER-DOWN/POWER-UP TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CEU}$, $\overline{CEL}$, $\overline{WE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	11
V_{CC} Slew from V_{TP} to 0V ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} Slew from 0V to V_{TP} ($\overline{CE}$ at V_{IH})	t_R	0			µs	
$\overline{CEU}$, $\overline{CEL}$, $\overline{WE}$ at V_{IH} after Power-Up	t_{REC}	100		200	ms	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CEU}$ or $\overline{CEL}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CEU}$, $\overline{CEL}$ or $\overline{WE}$ going low to the earlier of $\overline{CEU}$, $\overline{CEL}$ or $\overline{WE}$ going high.

4. t_{DS} is measured from the earlier of $\overline{CEU}$ or $\overline{CEL}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CEU}$ or $\overline{CEL}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CEU}$ or $\overline{CEL}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CEU}$ or $\overline{CEL}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1758 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is –40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2}, t_{DH2} are measured from $\overline{CEU}$ OR $\overline{CEL}$ going high.

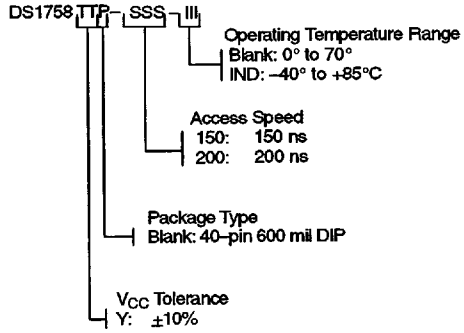
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns
All voltages are referenced to ground

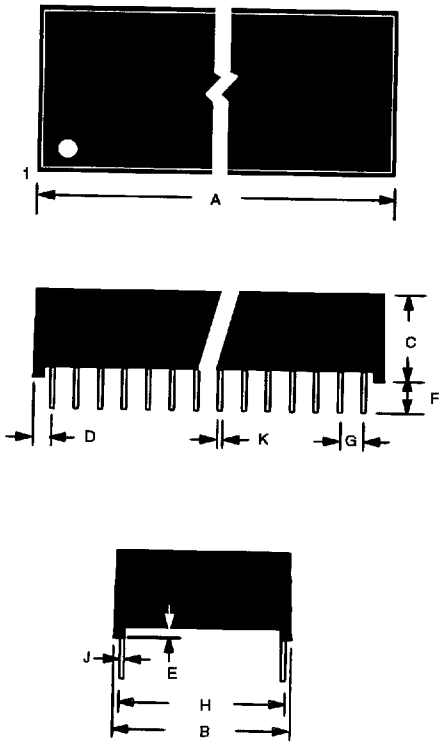
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels:
0.0 to 2.7 volts
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

ORDERING INFORMATION



DS1758Y NONVOLATILE SRAM, 40–PIN 740 MIL EXTENDED MODULE



PKG	40-PIN	
DIM	MIN	MAX
A IN.	2.080	21.00
MM	52.83	53.34
B IN.	0.715	0.740
MM	18.16	18.80
C IN.	0.345	0.365
MM	8.76	9.27
D IN.	0.085	0.115
MM	2.16	2.92
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.025
MM	0.43	0.58