

□ MN103S77N

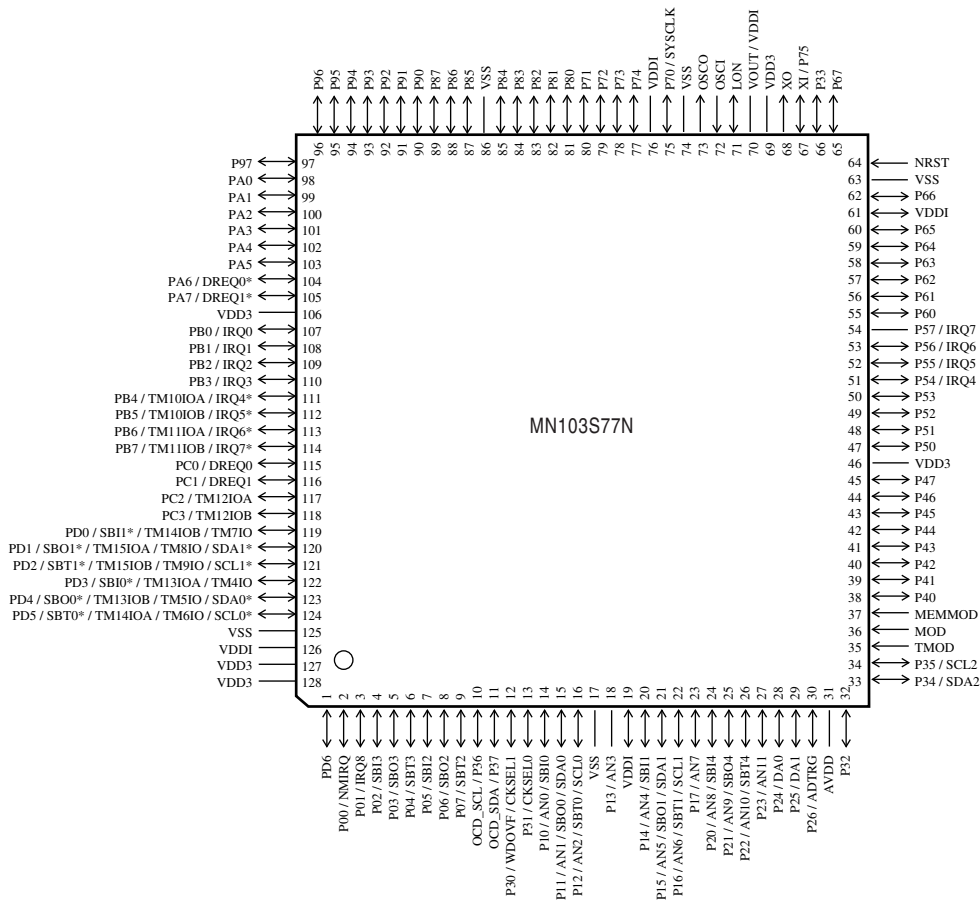
Type	MN103S77N (under development)		
Command ROM (×64-bit)	512 K-byte		
Data RAM (×32-bit)	32 K-byte		
Package	LQFP128-P-1818C *Lead-free		
Minimum Instruction Execution Time	16.7 ns (at 2.7 V to 3.6 V, 60 MHz)		
Interrupts	• RESET • IRQ × 9 • NMI • Timer × 28 • SIF × 10 • I ² C × 3 • Time base timer × 1 • DMA × 12 • WDT • A/D • System error		
Timer Counter	8-bit timer × 10 Reload-down count Cascade connection possible (usable as a 16-bit to 32-bit timer) 16-bit timer × 6 Up-down count Input capture function PWM generating function Compare/capture register 2-ch. Time base timer × 1 Watchdog timer × 1		
DMA Controller	Number of channels: 4 Unit of transfer: 8/16/32 bits Max. Transfer cycles: 65535 Starting factor: external interrupt, timer factor, serial transmission/reception factor, I ² C transmission/reception factor, external transmission request factor, A/D conversion finish, software factor Transfer method: 2-bus cycle transfer Addressing modes: fixed, increment, decrement Transfer modes: word transfer, burst transfer, intermittent transfer		
Serial Interface	UART/synchronous/multi-master I ² C interface selective: 3 UART/synchronous interface selective: 2		
I/O Pins	I/O	104	• Common use
A/D Inputs	10-bit × 12-ch.		
D/A Outputs	8-bit × 4-ch.		
ROM Collection	8-ch.		

Electrical Characteristics

A/D conversion performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Resolution					10	Bits
Non-linear error		AVDD = 3.3 V			± 4	LSB
Differential non-linearity error		VSS = 0 V			± 4	LSB

Pin Assignment



LQFP128-P-1818C *Lead-free

Support Tool

In-circuit Emulator	PX-ICE103S77	
On-board Development Tools	PX-ODB103-DO	
Flash Memory Built-in Type	Type	MN103SF77R (under development)
	Command ROM (× 64-bit)	1024 K-byte
	Data RAM (× 32-bit)	32 K-byte
	Minimum instruction execution time	16.7 ns (at 2.7 V to 3.6 V, 60 MHz)
	Package	LQFP128-P-1818C *Lead-free

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