FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-20882-2E

FLASH MEMORY

CMOS

64M (4M × 16) BIT

MBM29LV650UE/651UE -90/12

■ DESCRIPTION

The MBM29LV650UE/651UE is a 64M-bit, 3.0 V-only Flash memory organized as 4M words of 16 bits each. The device is designed to be programmed in system with the standard system 3.0 V V_{CC} supply. 12.0 V V_{PP} and 5.0 V V_{CC} are not required for write or erase operations. The devices can also be reprogrammed in standard EPROM programmers.

To eliminate bus contention the devices have separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls.

The MBM29LV650UE/651UE is entirely command set compatible with JEDEC single-power-supply Flash standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations.

Typically, each sector can be programmed and verified in about 0.5 seconds.

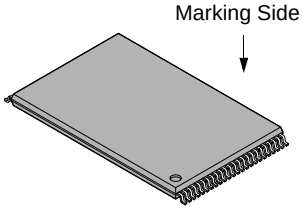
(Continued)

■ PRODUCT LINEUP

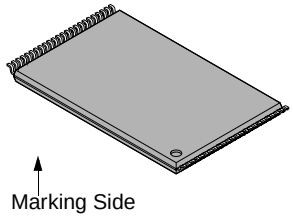
Part No.		MBM29LV650UE/651UE	
Ordering Part No.	V_{CC} = 3.3 V $^{+0.3\ V}_{-0.3\ V}$	90	—
	V_{CC} = 3.0 V $^{+0.6\ V}_{-0.3\ V}$	—	12
Max. Address Access Time (ns)		90	120
Max. $\overline{CE}$ Access Time (ns)		90	120
Max. $\overline{OE}$ Access Time (ns)		35	50

■ PACKAGES

48-pin plastic TSOP (I)



(FPT-48P-M19)



(FPT-48P-M20)

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A sector is typically erased and verified in 1.0 second. (If already completely preprogrammed.)
The device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The MBM29LV650UE/651UE is erased when shipped from the factory.

Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ_7, by the Toggle Bit feature on DQ_6. Once the end of a program or erase cycle has been completed, the devices internally reset to the read mode.
The devices electrically erase all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The words are programmed one word at a time using the EPROM programming mechanism of hot electron injection.

■ FEATURES

- **0.23 μm Process Technology**
- **Single 3.0 V read, program and erase**
  Minimizes system level power requirements
- **Compatible with JEDEC-standards**
  Uses same software commands with single-power supply Flash
- **Address don't care during the command sequence**
- **Industry-standard pinouts**
  48-pin TSOP (I) (Package suffix: TN - Normal Bend Type, TR - Reversed Bend Type)
- **Minimum 100,000 program/erase cycles**
- **High performance**
  90 ns maximum access time
- **Flexible sector architecture**
  One hundred twenty-eight 32K word sectors
  Any combination of sectors can be concurrently erased. Also supports full chip erase
- **Hidden ROM (Hi-ROM) region**
  128 word of Hi-ROM, accessible through a new "Hi-ROM Enable" command sequence
  Factory serialized and protected to provide a secure electronic serial number (ESN)
- **$\overline{\text{WP}}$ input pin**
  At V_{IL}, allows protection of first or last 32K word sector, regardless of sector protection/unprotection status
  At V_{IH}, allows removal of protection
  MBM29LV650UE: has the function to protect the last 32K word sector (SA 127)
  MBM29LV651UE: has the function to protect the first 32K word sector (SA 0)
- **ACC input pin**
  At V_{ACC}, increases program performance
- **Embedded Erase™* Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded program™* Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Automatic sleep mode**
  When addresses remain stable, automatically switches themselves to low power mode
- **Low V_{CC} write inhibit ≤ 2.5 V**
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data and/or program in another sector within the same device
- **Sector group protection**
  Hardware method disables any combination of sector groups from program or erase operations

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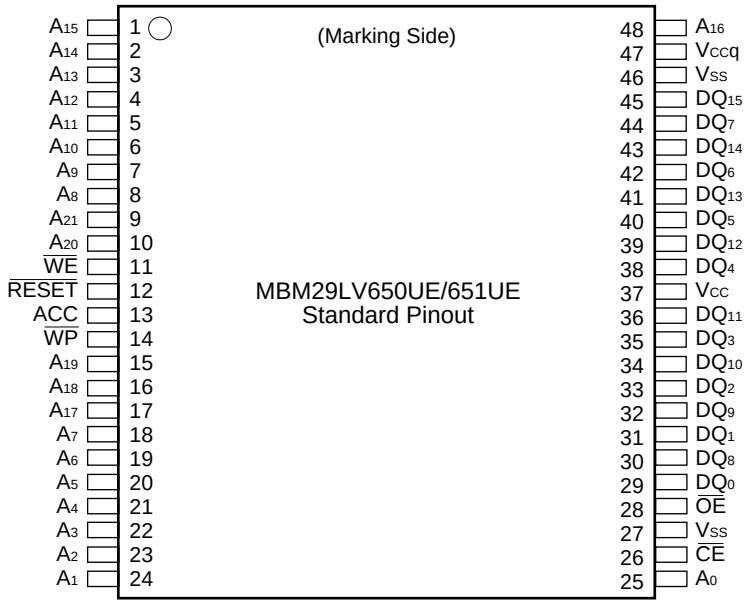
- **Sector Group Protection Set function by Extended sector protect command**
- **Fast Programming Function by Extended Command**
- **Temporary sector group unprotection**
  Temporary sector group unprotection via the $\overline{\text{RESET}}$ pin
  This feature allows code changes in previously locked sectors
- **In accordance with CFI (Common Flash Memory Interface)**

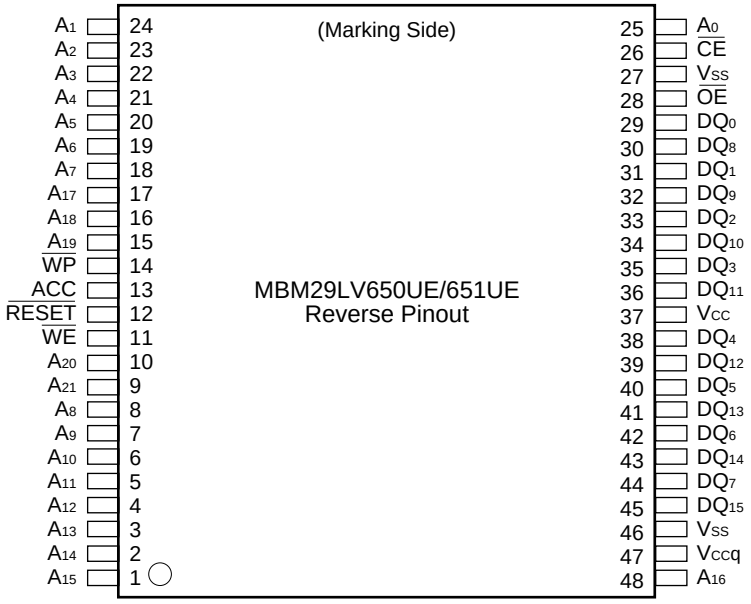
*: Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

■ PIN ASSIGNMENTS

TSOP(I)



FPT-48P-M19



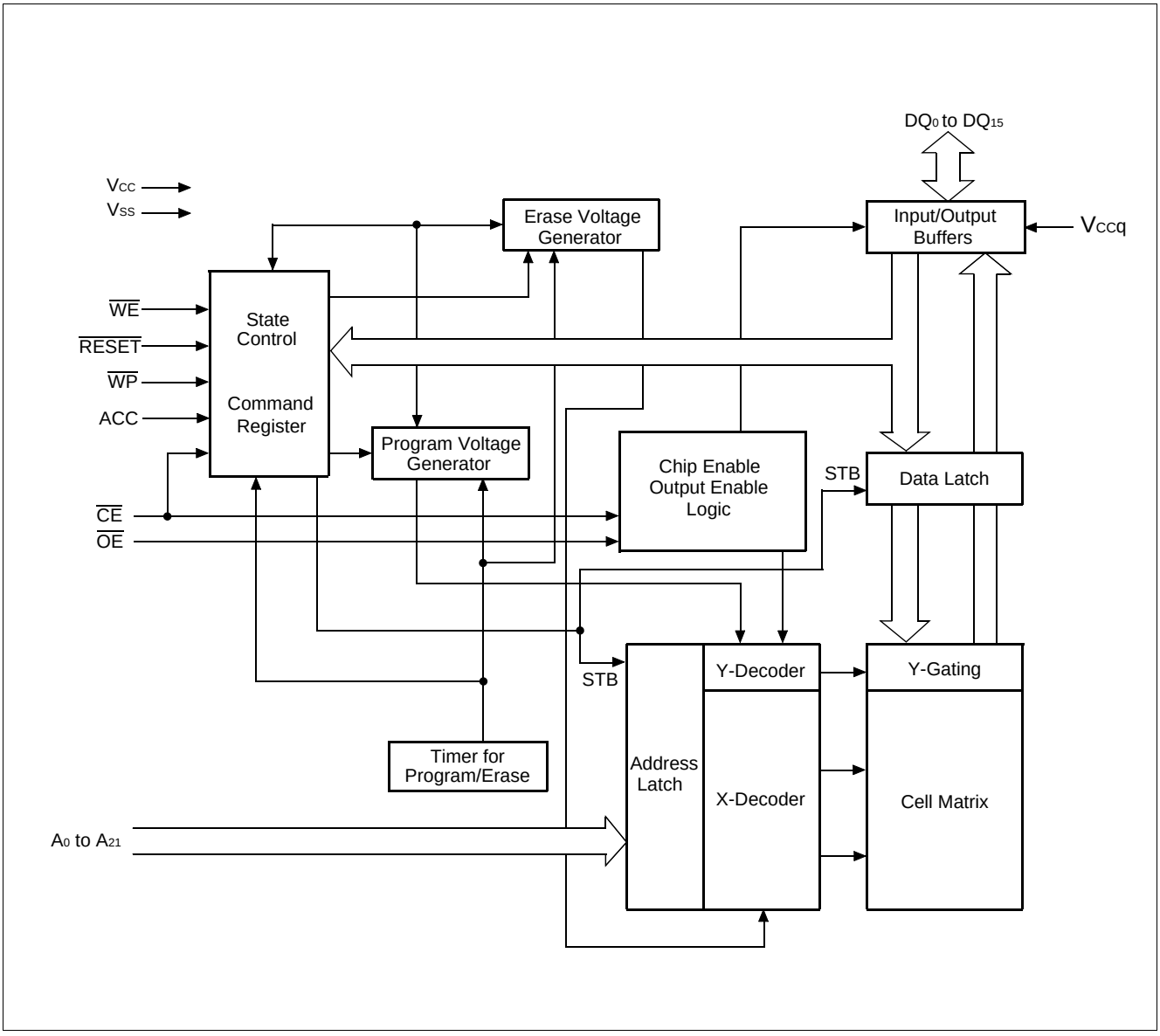
FPT-48P-M20

■ PIN DESCRIPTION

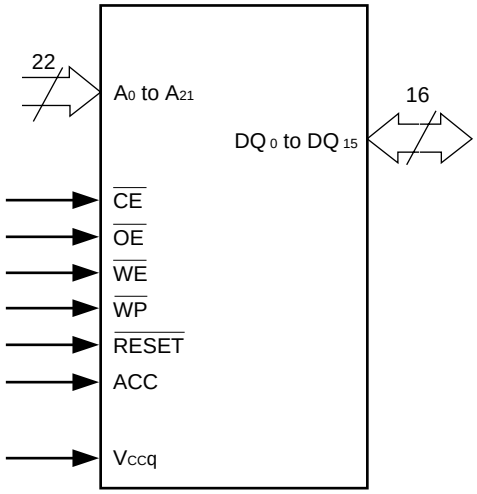
Table1 MBM29LV650UE/651UE Pin Configuration

Pin	Function
A_0 to A_{21}	Address Inputs
DQ_0 to DQ_{15}	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Hardware Write Protection
$\overline{RESET}$	Hardware Reset Pin/Temporary Sector Group Unprotection
ACC	Program Acceleration
$V_{CC}q$	Output Buffer Power
V_{SS}	Device Ground
V_{CC}	Device Power Supply

■ BLOCK DIAGRAM



■ LOGIC SYMBOL



■ DEVICE BUS OPERATION

Table2 MBM29LV650UE/651UE User Bus Operations

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0	A_1	A_6	A_9	DQ_0 to DQ_{15}	$\overline{RESET}$	$\overline{WP}$
Auto-Select Manufacture Code (1)	L	L	H	L	L	L	V_{ID}	Code	H	X
Auto-Select Device Code (1)	L	L	H	H	L	L	V_{ID}	Code	H	X
Read (3)	L	L	H	A_0	A_1	A_6	A_9	D_{OUT}	H	X
Standby	H	X	X	X	X	X	X	HIGH-Z	H	X
Output Disable	L	H	H	X	X	X	X	HIGH-Z	H	X
Write (Program/Erase)	L	H	L	A_0	A_1	A_6	A_9	D_{IN}	H	X
Enable Sector Group Protection (2), (4)	L	V_{ID}	⊓⊔	L	H	L	V_{ID}	X	H	X
Verify Sector Group Protection (2), (4)	L	L	H	L	H	L	V_{ID}	Code	H	X
Temporary Sector Group Unprotection (5)	X	X	X	X	X	X	X	X	V_{ID}	X
Reset (Hardware)/Standby	X	X	X	X	X	X	X	HIGH-Z	L	X
Outermost Sector Write Protection	X	X	X	X	X	X	X	X	X	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. ⊓⊔ = Pulse input. See DC Characteristics for voltage levels.

Notes: 1. Manufacturer and device codes may also be accessed via a command register write sequence. See Table 3.
2. Refer to the section on Sector Group Protection.
3. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.
4. V_{CC} = 3.3 V ±10%
5. It is also used for the extended sector group protection.

Table 3 MBM29LV650UE/651UE Command Definitions

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
Read/Reset	3	XXXh	AAh	XXXh	55h	XXXh	F0h	RA	RD	—	—	—	—
Autoselect	3	XXXh	AAh	XXXh	55h	XXXh	90h	—	—	—	—	—	—
Program	4	XXXh	AAh	XXXh	55h	XXXh	A0h	PA	PD	—	—	—	—
Chip Erase	6	XXXh	AAh	XXXh	55h	XXXh	80h	XXXh	AAh	XXXh	55h	XXXh	10h
Sector Erase	6	XXXh	AAh	XXXh	55h	XXXh	80h	XXXh	AAh	XXXh	55h	SA	30h
Erase Suspend	1	XXXh	B0h	—	—	—	—	—	—	—	—	—	—
Erase Resume	1	XXXh	30h	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	3	XXXh	AAh	XXXh	55h	XXXh	20h	—	—	—	—	—	—
Fast Program *1	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—
Reset from Fast Mode *1	2	XXXh	90h	XXXh	F0h	—	—	—	—	—	—	—	—
Extended Sector Group Protection *2	4	XXXh	60h	SPA	60h	SPA	40h	SPA	SD	—	—	—	—
Query *3	1	XXh	98h	—	—	—	—	—	—	—	—	—	—
Hi-ROM Entry	3	XXXh	AAh	XXXh	55h	XXXh	88h	—	—	—	—	—	—
Hi-ROM Program *4	4	XXXh	AAh	XXXh	55h	XXXh	A0h	PA	PD	—	—	—	—
Hi-ROMExit *4	4	XXXh	AAh	XXXh	55h	XXXh	90h	XXXh	00h	—	—	—	—

*1: This command is valid while Fast Mode.

*2: This command is valid while $\overline{RESET} = V_{ID}$.

*3: The valid addresses are A_6 to A_0.

*4: This command is valid while Hi-ROM mode.

Note:1. Address bits = X = "H" or "L" for all address commands except or Program Address (PA) and Sector Address (SA).

2.Bus operations are defined in Table 2.

3.RA = Address of the memory location to be read.
PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the write pulse.
SA = Address of the sector to be erased. The combination of A_{21}, A_{20}, A_{19}, A_{18}, A_{17},A_{16}, and A_{15} will uniquely select any sector.

4.RD = Data read from location RA during read operation.
PD = Data to be programmed at location PA. Data is latched on the falling edge of write pulse.

5.SPA = Sector group address to be protected. Set sector group address (SGA) and (A_6, A_1, A_0) = (0, 1, 0).
SD = Sector group protection verify data. Output 01h at protected sector group addresses and output 00h at unprotected sector group addresses.

6.Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

Table 4 .1 MBM29LV650UE/651UE Sector Group Protection Verify Autoselect Codes

Type		A_{17} to A_{21}	A_6	A_1	A_0	Code (HEX)
Manufacturer's Code		X	V_{IL}	V_{IL}	V_{IL}	04h
Device Code	MBM29LV650UE/651UE	X	V_{IL}	V_{IL}	V_{IH}	22D7h
Sector Group Protection		Sector Group Addresses	V_{IL}	V_{IH}	V_{IL}	01h *
Extended Code	MBM29LV650UE	X	V_{IL}	V_{IH}	V_{IH}	0010h
	MBM29LV651UE					0000h

*: Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

Table 4 .2 Expanded Autoselect Code Table

Type		Code	DQ_{15}	DQ_{14}	DQ_{13}	DQ_{12}	DQ_{11}	DQ_{10}	DQ_9	DQ_8	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer's Code		04h	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	MBM29LV650UE/651UE	22D7h	0	0	1	0	0	0	1	0	1	1	0	1	0	1	1	1
Sector Group Protection		01h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Extend Code	MBM29LV650UE	0010h	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	MBM29LV651UE	0000h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

Table 5 Sector Address Tables

Sector Address	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	Sector Size	Address Range
SA0	0	0	0	0	0	0	0	32K words	000000h to 007FFFh
SA1	0	0	0	0	0	0	1	32K words	008000h to 00FFFFh
SA2	0	0	0	0	0	1	0	32K words	010000h to 017FFFh
SA3	0	0	0	0	0	1	1	32K words	018000h to 01FFFFh
SA4	0	0	0	0	1	0	0	32K words	020000h to 027FFFh
SA5	0	0	0	0	1	0	1	32K words	028000h to 02FFFFh
SA6	0	0	0	0	1	1	0	32K words	030000h to 037FFFh
SA7	0	0	0	0	1	1	1	32K words	038000h to 03FFFFh
SA8	0	0	0	1	0	0	0	32K words	040000h to 047FFFh
SA9	0	0	0	1	0	0	1	32K words	048000h to 04FFFFh
SA10	0	0	0	1	0	1	0	32K words	050000h to 057FFFh
SA11	0	0	0	1	0	1	1	32K words	058000h to 05FFFFh
SA12	0	0	0	1	1	0	0	32K words	060000h to 067FFFh
SA13	0	0	0	1	1	0	1	32K words	068000h to 06FFFFh
SA14	0	0	0	1	1	1	0	32K words	070000h to 077FFFh
SA15	0	0	0	1	1	1	1	32K words	078000h to 07FFFFh
SA16	0	0	1	0	0	0	0	32K words	080000h to 087FFFh
SA17	0	0	1	0	0	0	1	32K words	088000h to 08FFFFh
SA18	0	0	1	0	0	1	0	32K words	090000h to 097FFFh
SA19	0	0	1	0	0	1	1	32K words	098000h to 09FFFFh
SA20	0	0	1	0	1	0	0	32K words	0A0000h to 0A7FFFh
SA21	0	0	1	0	1	0	1	32K words	0A8000h to 0AFFFFh
SA22	0	0	1	0	1	1	0	32K words	0B0000h to 0B7FFFh
SA23	0	0	1	0	1	1	1	32K words	0B8000h to 0BFFFFh
SA24	0	0	1	1	0	0	0	32K words	0C0000h to 0C7FFFh
SA25	0	0	1	1	0	0	1	32K words	0C8000h to 0CFFFFh
SA26	0	0	1	1	0	1	0	32K words	0D0000h to 0D7FFFh
SA27	0	0	1	1	0	1	1	32K words	0D8000h to 0DFFFFh
SA28	0	0	1	1	1	0	0	32K words	0E0000h to 0E7FFFh
SA29	0	0	1	1	1	0	1	32K words	0E8000h to 0EFFFFh
SA30	0	0	1	1	1	1	0	32K words	0F0000h to 0F7FFFh
SA31	0	0	1	1	1	1	1	32K words	0F8000h to 0FFFFFh

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Sector Address	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	Sector Size	Address Range
SA32	0	1	0	0	0	0	0	32K words	100000h to 107FFFh
SA33	0	1	0	0	0	0	1	32K words	108000h to 10FFFFh
SA34	0	1	0	0	0	1	0	32K words	110000h to 117FFFh
SA35	0	1	0	0	0	1	1	32K words	118000h to 11FFFFh
SA36	0	1	0	0	1	0	0	32K words	120000h to 127FFFh
SA37	0	1	0	0	1	0	1	32K words	128000h to 12FFFFh
SA38	0	1	0	0	1	1	0	32K words	130000h to 137FFFh
SA39	0	1	0	0	1	1	1	32K words	138000h to 13FFFFh
SA40	0	1	0	1	0	0	0	32K words	140000h to 147FFFh
SA41	0	1	0	1	0	0	1	32K words	148000h to 14FFFFh
SA42	0	1	0	1	0	1	0	32K words	150000h to 157FFFh
SA43	0	1	0	1	0	1	1	32K words	158000h to 15FFFFh
SA44	0	1	0	1	1	0	0	32K words	160000h to 167FFFh
SA45	0	1	0	1	1	0	1	32K words	168000h to 16FFFFh
SA46	0	1	0	1	1	1	0	32K words	170000h to 177FFFh
SA47	0	1	0	1	1	1	1	32K words	178000h to 17FFFFh
SA48	0	1	1	0	0	0	0	32K words	180000h to 187FFFh
SA49	0	1	1	0	0	0	1	32K words	188000h to 18FFFFh
SA50	0	1	1	0	0	1	0	32K words	190000h to 197FFFh
SA51	0	1	1	0	0	1	1	32K words	198000h to 19FFFFh
SA52	0	1	1	0	1	0	0	32K words	1A0000h to 1A7FFFh
SA53	0	1	1	0	1	0	1	32K words	1A8000h to 1AFFFFh
SA54	0	1	1	0	1	1	0	32K words	1B0000h to 1B7FFFh
SA55	0	1	1	0	1	1	1	32K words	1B8000h to 1BFFFFh
SA56	0	1	1	1	0	0	0	32K words	1C0000h to 1C7FFFh
SA57	0	1	1	1	0	0	1	32K words	1C8000h to 1CFFFFh
SA58	0	1	1	1	0	1	0	32K words	1D0000h to 1D7FFFh
SA59	0	1	1	1	0	1	1	32K words	1D8000h to 1DFFFFh
SA60	0	1	1	1	1	0	0	32K words	1E0000h to 1E7FFFh
SA61	0	1	1	1	1	0	1	32K words	1E8000h to 1EFFFFh
SA62	0	1	1	1	1	1	0	32K words	1F0000h to 1F7FFFh
SA63	0	1	1	1	1	1	1	32K words	1F8000h to 1FFFFFh

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Sector Address	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	Sector Size	Address Range
SA64	1	0	0	0	0	0	0	32K words	200000h to 207FFFh
SA65	1	0	0	0	0	0	1	32K words	208000h to 20FFFFh
SA66	1	0	0	0	0	1	0	32K words	210000h to 217FFFh
SA67	1	0	0	0	0	1	1	32K words	218000h to 21FFFFh
SA68	1	0	0	0	1	0	0	32K words	220000h to 227FFFh
SA69	1	0	0	0	1	0	1	32K words	228000h to 22FFFFh
SA70	1	0	0	0	1	1	0	32K words	230000h to 237FFFh
SA71	1	0	0	0	1	1	1	32K words	238000h to 23FFFFh
SA72	1	0	0	1	0	0	0	32K words	240000h to 247FFFh
SA73	1	0	0	1	0	0	1	32K words	248000h to 24FFFFh
SA74	1	0	0	1	0	1	0	32K words	250000h to 257FFFh
SA75	1	0	0	1	0	1	1	32K words	258000h to 25FFFFh
SA76	1	0	0	1	1	0	0	32K words	260000h to 267FFFh
SA77	1	0	0	1	1	0	1	32K words	268000h to 26FFFFh
SA78	1	0	0	1	1	1	0	32K words	270000h to 277FFFh
SA79	1	0	0	1	1	1	1	32K words	278000h to 27FFFFh
SA80	1	0	1	0	0	0	0	32K words	280000h to 287FFFh
SA81	1	0	1	0	0	0	1	32K words	288000h to 28FFFFh
SA82	1	0	1	0	0	1	0	32K words	290000h to 297FFFh
SA83	1	0	1	0	0	1	1	32K words	298000h to 29FFFFh
SA84	1	0	1	0	1	0	0	32K words	2A0000h to 2A7FFFh
SA85	1	0	1	0	1	0	1	32K words	2A8000h to 2AFFFFh
SA86	1	0	1	0	1	1	0	32K words	2B0000h to 2B7FFFh
SA87	1	0	1	0	1	1	1	32K words	2B8000h to 2BFFFFh
SA88	1	0	1	1	0	0	0	32K words	2C0000h to 2C7FFFh
SA89	1	0	1	1	0	0	1	32K words	2C8000h to 2CFFFFh
SA90	1	0	1	1	0	1	0	32K words	2D0000h to 2D7FFFh
SA91	1	0	1	1	0	1	1	32K words	2D8000h to 2DFFFFh
SA92	1	0	1	1	1	0	0	32K words	2E0000h to 2E7FFFh
SA93	1	0	1	1	1	0	1	32K words	2E8000h to 2EFFFFh
SA94	1	0	1	1	1	1	0	32K words	2F0000h to 2F7FFFh
SA95	1	0	1	1	1	1	1	32K words	2F8000h to 2FFFFFh

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Sector Address	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	Sector Size	Address Range
SA96	1	1	0	0	0	0	0	32K words	300000h to 307FFFh
SA97	1	1	0	0	0	0	1	32K words	308000h to 30FFFFh
SA98	1	1	0	0	0	1	0	32K words	310000h to 317FFFh
SA99	1	1	0	0	0	1	1	32K words	318000h to 31FFFFh
SA100	1	1	0	0	1	0	0	32K words	320000h to 327FFFh
SA101	1	1	0	0	1	0	1	32K words	328000h to 32FFFFh
SA102	1	1	0	0	1	1	0	32K words	330000h to 337FFFh
SA103	1	1	0	0	1	1	1	32K words	338000h to 33FFFFh
SA104	1	1	0	1	0	0	0	32K words	340000h to 347FFFh
SA105	1	1	0	1	0	0	1	32K words	348000h to 34FFFFh
SA106	1	1	0	1	0	1	0	32K words	350000h to 357FFFh
SA107	1	1	0	1	0	1	1	32K words	358000h to 35FFFFh
SA108	1	1	0	1	1	0	0	32K words	360000h to 367FFFh
SA109	1	1	0	1	1	0	1	32K words	368000h to 36FFFFh
SA110	1	1	0	1	1	1	0	32K words	370000h to 377FFFh
SA111	1	1	0	1	1	1	1	32K words	378000h to 37FFFFh
SA112	1	1	1	0	0	0	0	32K words	380000h to 387FFFh
SA113	1	1	1	0	0	0	1	32K words	388000h to 38FFFFh
SA114	1	1	1	0	0	1	0	32K words	390000h to 397FFFh
SA115	1	1	1	0	0	1	1	32K words	398000h to 39FFFFh
SA116	1	1	1	0	1	0	0	32K words	3A0000h to 3A7FFFh
SA117	1	1	1	0	1	0	1	32K words	3A8000h to 3AFFFFh
SA118	1	1	1	0	1	1	0	32K words	3B0000h to 3B7FFFh
SA119	1	1	1	0	1	1	1	32K words	3B8000h to 3BFFFFh
SA120	1	1	1	1	0	0	0	32K words	3C0000h to 3C7FFFh
SA121	1	1	1	1	0	0	1	32K words	3C8000h to 3CFFFFh
SA122	1	1	1	1	0	1	0	32K words	3D0000h to 3D7FFFh
SA123	1	1	1	1	0	1	1	32K words	3D8000h to 3DFFFFh
SA124	1	1	1	1	1	0	0	32K words	3E0000h to 3E7FFFh
SA125	1	1	1	1	1	0	1	32K words	3E8000h to 3EFFFFh
SA126	1	1	1	1	1	1	0	32K words	3F0000h to 3F7FFFh
SA127	1	1	1	1	1	1	1	32K words	3F8000h to 3FFFFFh

Table 6 Sector Group Address

Sector Group Address	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	Sector Group Size	Sectors
SGA0	0	0	0	0	0	128K words	SA0 to SA3
SGA1	0	0	0	0	1	128K words	SA4 to SA7
SGA2	0	0	0	1	0	128K words	SA8 to SA11
SGA3	0	0	0	1	1	128K words	SA12 to SA15
SGA4	0	0	1	0	0	128K words	SA16 to SA19
SGA5	0	0	1	0	1	128K words	SA20 to SA23
SGA6	0	0	1	1	0	128K words	SA24 to SA27
SGA7	0	0	1	1	1	128K words	SA28 to SA31
SGA8	0	1	0	0	0	128K words	SA32 to SA35
SGA9	0	1	0	0	1	128K words	SA36 to SA39
SGA10	0	1	0	1	0	128K words	SA40 to SA43
SGA11	0	1	0	1	1	128K words	SA44 to SA47
SGA12	0	1	1	0	0	128K words	SA48 to SA51
SGA13	0	1	1	0	1	128K words	SA52 to SA55
SGA14	0	1	1	1	0	128K words	SA56 to SA59
SGA15	0	1	1	1	1	128K words	SA60 to SA63
SGA16	1	0	0	0	0	128K words	SA64 to SA67
SGA17	1	0	0	0	1	128K words	SA68 to SA71
SGA18	1	0	0	1	0	128K words	SA72 to SA75
SGA19	1	0	0	1	1	128K words	SA76 to SA79
SGA20	1	0	1	0	0	128K words	SA80 to SA83
SGA21	1	0	1	0	1	128K words	SA84 to SA87
SGA22	1	0	1	1	0	128K words	SA88 to SA91
SGA23	1	0	1	1	1	128K words	SA92 to SA95
SGA24	1	1	0	0	0	128K words	SA96 to SA99
SGA25	1	1	0	0	1	128K words	SA100 to SA103
SGA26	1	1	0	1	0	128K words	SA104 to SA107
SGA27	1	1	0	1	1	128K words	SA108 to SA111
SGA28	1	1	1	0	0	128K words	SA112 to SA115
SGA29	1	1	1	0	1	128K words	SA116 to SA119
SGA30	1	1	1	1	0	128K words	SA120 to SA123
SGA31	1	1	1	1	1	128K words	SA124 to SA127

Table 7 Common Flash Memory Interface Code

Description	A_0 to A_6	DQ_0 to DQ_{15}
Query-unique ASCII string "QRY"	10h 11h 12h	0051h 0052h 0059h
Primary OEM Command Set 2h: AMD/FJ standard type	13h 14h	0002h 0000h
Address for Primary Extended Table	15h 16h	0040h 0000h
Alternate OEM Command Set (00h = not applicable)	17h 18h	0000h 0000h
Address for Alternate OEM Extended Table	19h 1Ah	0000h 0000h
V_{CC} Min. (write/erase) D7-4: volt, D3-0: 100 mvolt	1Bh	0027h
V_{CC} Max. (write/erase) D7-4: volt, D3-0: 100 mvolt	1Ch	0036h
V_{PP} Min. voltage	1Dh	0000h
V_{PP} Max. voltage	1Eh	0000h
Typical timeout per single byte/word write 2^N µs	1Fh	0004h
Typical timeout for Min. size buffer write 2^N µs	20h	0000h
Typical timeout per individual block erase 2^N ms	21h	000Ah
Typical timeout for full chip erase 2^N ms	22h	0000h
Max. timeout for byte/word write 2^N times typical	23h	0005h
Max. timeout for buffer write 2^N times typical	24h	0000h
Max. timeout per individual block erase 2^N times typical	25h	0004h
Max. timeout for full chip erase 2^N times typical	26h	0000h
Device Size = 2^N byte	27h	0017h
Flash Device Interface description	28h 29h	0001h 0000h
Max. number of byte in multi-byte write = 2^N	2Ah 2Bh	0000h 0000h
Number of Erase Block Regions within device	2Ch	0001h
Erase Block Region 1 Information	2Dh 2Eh 2Fh 30h	007Fh 0000h 0000h 0001h
Erase Block Region 2 Information	31h 32h 33h 34h	0000h 0000h 0000h 0000h
Query-unique ASCII string "PRI"	40h 41h 42h	0050h 0052h 0049h
Major version number, ASCII	43h	0031h
Minor version number, ASCII	44h	0031h
Address Sensitive Unlock 0h = Required 1h = Not Required	45h	0001h
Erase Suspend 0h = Not Supported 1h = To Read Only 2h = To Read & Write	46h	0002h
Sector Protection 0h = Not Supported X = Number of sectors in per group	47h	0004h
Sector Temporary Unprotection 00h = Not Supported 01h = Supported	48h	0001h
Sector Protection Algorithm	49h	0004h
Number of Sector for Bank 2 00h = Not Supported	4Ah	0000h
Burst Mode Type 00h = Not Supported	4Bh	0000h
Page Mode Type 00h = Not Supported	4Ch	0000h
ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-4: volt, D3-0: 100 mvolt	4Dh	00B5h
ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-4: volt, D3-0: 100 mvolt	4Eh	00C5h
Boot Type 04h = MBM29LV651UE 05h = MBM29LV650UE	4Fh	00XXh

■ FUNCTIONAL DESCRIPTION

Read Mode

The MBM29LV650UE/651UE has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for a device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins. (Assuming the addresses have been stable for at least t_{ACC}-t_{OE} time.) When reading out a data without changing addresses after power-up, it is necessary to input hardware reset or to change $\overline{CE}$ pin from “H” or “L”.

Standby Mode

There are two ways to implement the standby mode on the MBM29LV650UE/651UE devices, one using both the $\overline{CE}$ and $\overline{RESET}$ pins; the other via the $\overline{RESET}$ pin only.

When using both pins, a CMOS standby mode is achieved with $\overline{CE}$ and $\overline{RESET}$ inputs both held at V_{CC} ±0.3 V. Under this condition the current consumed is less than 5 μA max. During Embedded Algorithm operation, V_{CC} active current (I_{CC2}) is required even $\overline{CE}$ = “H”. The device can be read with standard access time (t_{CE}) from either of these standby modes.

When using the $\overline{RESET}$ pin only, a CMOS standby mode is achieved with $\overline{RESET}$ input held at V_{SS} ±0.3 V ($\overline{CE}$ = “H” or “L”). Under this condition the current consumed is less than 5 μA max. Once the $\overline{RESET}$ pin is taken high, the device requires t_{RH} of wake up time before outputs are valid for read access.

In the standby mode the outputs are in the high impedance state, independent of the $\overline{OE}$ input.

Automatic Sleep Mode

There is a function called automatic sleep mode to restrain power consumption during read-out of MBM29LV650UE/651UE data. This mode can be used effectively with an application requesting low power consumption such as handy terminals.

To activate this mode, MBM29LV650UE/651UE automatically switch themselves to low power mode when MBM29LV650UE/651UE addresses remain stable during access fine of 150 ns. It is not necessary to control $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ on the mode. Under the mode, the current consumed is typically 1 μA (CMOS Level).

Since the data are latched during this mode, the data are read-out continuously. If the addresses are changed, the mode is canceled automatically and MBM29LV650UE/651UE read-out the data for changed addresses.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the devices are disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the devices and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the devices to be programmed with its corresponding programming algorithm. The Autoselect command may also be used to check the status of write-protected sectors (see Tables 4.1 and 4.2). This mode is functional over the entire temperature range of the devices.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A_9. Two identifier bytes may then be sequenced from the devices outputs by toggling address A_0 from V_{IL} to V_{IH}. All addresses are DON’T CARES except A_0, A_1, and A_6. (See Table 2.)

The manufacturer and device codes may also be read via the command register, for instances when the MBM29LV650UE/651UE is erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in Table 3. (Refer to Autoselect Command section.)

Word 0 ($A_0 = V_{IL}$) represents the manufacturer's code (Fujitsu = 04h) and word 1 ($A_0 = V_{IH}$) represents the device identifier code (MBM29LV650UE/651UE = 22D7h). Word 3 ($A_0 = A_1 = V_{IH}$) represents the Extended Code (MBM29LV650UE = 2201h, MBM29LV651UE = 2200h). These three words are given in the tables 4.1 to 4.2. All identifiers for manufactures and device will exhibit odd parity with DQ_7 defined as the parity bit. In order to read the proper device codes when executing the autoselect, A_1 must be V_{IL}. (See Tables 4.1 to 4.2.)

In order to determine which sectors are write protected, A_1 must be at V_{IH} while running through the sector addresses; if the selected sector is protected, a logical '1' will be output on DQ_0 ($DQ_0 = 1$).

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Group Protection

The MBM29LV650UE/651UE features hardware sector group protection. This feature will disable both program and erase operations in any combination of twenty five sector groups of memory. (See Table 6). The sector group protection feature is enabled using programming equipment at the user's site. The device is shipped with all sector groups unprotected.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, (suggest $V_{ID} = 11.5$ V), $\overline{CE} = V_{IL}$ and $A_0 = A_6 = V_{IL}$, $A_1 = V_{IH}$. The sector group addresses (A_{21}, A_{20}, A_{19}, A_{18}, and A_{17}) should be set to the sector to be protected. Table 5 defines the sector address for each of the one hundred twenty-eight (128) individual sectors, and tables 2 defines the sector group address for each of the thirty-two (32) individual group sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector group addresses must be held constant during the $\overline{WE}$ pulse. See figures 12 and 20 for sector group protection waveforms and algorithm.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector group addresses (A_{21}, A_{20}, A_{19}, A_{18}, and A_{17}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical "1" code at device output DQ_0 for a protected sector. Otherwise the device will produce "0" for unprotected sector. In this mode, the lower order addresses, except for A_0, A_1, and A_6 are DON'T CARES. Address locations with $A_1 = V_{IL}$ are reserved for Autoselect manufacturer and device codes.

It is also possible to determine if a sector group is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02h, where the higher order addresses (A_{21}, A_{20}, A_{19}, A_{18}, and A_{17}) are the desired sector group address will produce a logical "1" at DQ_0 for a protected sector group. See Tables 4.1 and 4.2 for Autoselect codes.

Temporary Sector Group Unprotection

This feature allows temporary unprotection of previously protected sector groups of the MBM29LV650UE/651UE devices in order to change data. The Sector Group Unprotection mode is activated by setting the $\overline{RESET}$ pin to high voltage (V_{ID}). During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once the V_{ID} is taken away from the $\overline{RESET}$ pin, all the previously protected sector groups will be protected again. Refer to Figures 13 and 21.

This temporary sector group unprotect mode is disabled whenever the chip is in the Hidden ROM (Hi-ROM) mode. This area can not be programmed within this mode. Moreover once this area is programmed, it is always protected no matter in which mode.

$\overline{\text{RESET}}$

Hardware Reset Pin

The MBM29LV650UE/651UE devices may be reset by driving the $\overline{\text{RESET}}$ pin to V_{IL}. The $\overline{\text{RESET}}$ pin has a pulse requirement and has to be kept low (V_{IL}) for at least "t_{RP}" in order to properly reset the internal state machine. Any operation in the process of being executed will be terminated and the internal state machine will be reset to the read mode "t_{READY}" after the $\overline{\text{RESET}}$ pin is driven low. Furthermore, once the $\overline{\text{RESET}}$ pin goes high, the devices require an additional "t_{RH}" before it will allow read access. When the $\overline{\text{RESET}}$ pin is low, the devices will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be corrupted.

Write Protect ($\overline{\text{WP}}$)

The Write Protection function provides a hardware method of protecting certain "outermost" 32K word sector without using V_{ID}.

If the system asserts V_{IL} on the $\overline{\text{WP}}$ pin, the device disables program and erase functions in the "outermost" 32K word sector independently of whether this sector was protected or unprotected using the method described in "Sector Protection/Unprotection". The outermost 32K word sector is the highest addresses in MBM29LV650UE, or the lowest addresses in MBM29LV651UE.

(MBM29LV650UE: SA127, MBM29LV651UE: SA0)

If the system asserts V_{IH} on the $\overline{\text{WP}}$ pin, the device reverts to whether the outermost 32K word sector was last set to be protected or unprotected. That is, sector protection or unprotection for this sector depends on whether this was last protected or unprotected using the method described in "Sector protection/unprotection".

Accelerated Program Operation

MBM29LV650UE/651UE offers accelerated program operation which enables the programming in high speed. If the system asserts V_{ACC} to the ACC pin, the device automatically enters the acceleration mode and the time required for program operation will reduce to about 50%. This function is primarily intended to allow high speed program, so caution is needed as the sector group will temporarily be unprotected.

The system would use a fast program command sequence when programming during acceleration mode. Set command to fast mode and reset command from fast mode is not necessary. When the device enters the acceleration mode, the device automatically set to fast mode. Therefore, the present sequence could be used for programming and detection of completion during acceleration mode.

Removing V_{ACC} from the ACC pin returns the device to normal operation. Do not remove V_{ACC} from the ACC pin while programming. (See Figure 15.)

■ COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect data values or writing them in the improper sequence will reset the devices to the read mode. Table 3 defines the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Moreover both Read/Reset commands are functionally equivalent, resetting the device to the read mode. Please note that commands are always written at DQ_0 to DQ_7 and DQ_8 to DQ_{15} bits are ignored.

Read/Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits (DQ_5 = 1) to Read/Reset mode, the Read/Reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The devices remain enabled for reads until the command register contents are altered.

The devices will automatically power-up in the Read/Reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the devices reside in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register.

The Autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the address and the Autoselect command. Then the manufacture and device codes can be read from the address, and an actual data of memory cell can be read from the another address.

Following the command write, a read cycle from address XX00h retrieves the manufacture code of 04h. A read cycle from address XX01h returns the device code (MBM29LV650UE/651UE = 22D7h). A read cycle from address XX03h returns the Extended Code (MBM29LV650UE = 0010h, MBM29LV651UE = 0000h). (See Tables 4.1 and 4.2.)

All manufacturer and device codes will exhibit odd parity with DQ_7 defined as the parity bit. Sector state (protection or unprotection) will be informed by address XX02h. Scanning the sector group addresses (A_{21}, A_{20}, A_{19}, A_{18}, and A_{17}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical “1” at device output DQ_0 for a protected sector group. The programming verification should be performed by verify sector group protection on the protected sector. (See Table 2.)

To terminate the operation, it is necessary to write the Read/Reset command sequence into the register, and also to write the Autoselect command during the operation, execute it after writing Read/Reset command sequence.

Word Programming

The devices are programmed on a word-by-word basis. Programming is a four bus cycle operation. There are two “unlock” write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The system can determine the status of the program operation by using DQ_7 ($\overline{Data}$ Polling), and DQ_6 (Toggle Bit). The $\overline{Data}$ Polling and Toggle Bit must be performed at the memory location which is being programmed.

The automatic programming operation is completed when the data on DQ_7 is equivalent to data written to this bit at which time the devices return to the read mode and addresses are no longer latched. (See Table 8, Hardware Sequence Flags.) Therefore, the devices require that a valid address to the devices be supplied by the system at this particular instance of time. Hence, $\overline{Data}$ Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored. If hardware reset occurs during the programming operation, it is impossible to guarantee the data are being written.

Programming is allowed in any sequence and across sector boundaries. Beware that a data “0” cannot be programmed back to a “1” Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from Read/Reset mode will show that the data is still “0” Only erase operations can convert “0”s to “1”s.

Figure 16 illustrates the Embedded Program™ Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the devices will automatically program and verify the entire memory for an all zero data pattern prior to electrical erase (Preprogram function). The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{Data}$ Polling), and DQ_6 (Toggle Bit). The chip erase begins on the rising edge of the last $\overline{CE}$ or $\overline{WE}$, whichever happens first in the command sequence and terminates when the data on DQ_7 is “1” (See Write Operation Status section.) at which time the device returns to read the mode.

Chip Erase Time; Sector Erase Time $\times$ All sectors + Chip Program Time (Preprogramming)

Figure 17 illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ whichever happens later, while the command (Data = 30h) is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$ which happens first. After time-out of “t_{TOW}” from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased concurrently by writing the six bus cycle operations on Table 3. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than "t_{TOW}" otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of "t_{TOW}" from the rising edge of last $\overline{CE}$ or $\overline{WE}$ whichever happens first will initiate the execution of the Sector Erase command(s). If another falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first occurs within the "t_{TOW}" time-out window the timer is reset. (Monitor DQ_3 to determine if the sector erase timer window is still open, see section DQ_3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this time-out period will reset the devices to the read mode, ignoring the previous command string. Resetting the devices once execution has begun will corrupt the data in the sector. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 127).

Sector erase does not require the user to program the devices prior to erase. The devices automatically program all memory locations in the sector(s) to be erased prior to electrical erase (Preprogram function). When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{Data}$ Polling), and DQ_6 (Toggle Bit).

The sector erase begins after the "t_{TOW}" time out from the rising edge of $\overline{CE}$ or $\overline{WE}$ whichever happens first for the last sector erase command pulse and terminates when the data on DQ_7 is "1" (See Write Operation Status section.) at which time the devices return to the read mode. $\overline{Data}$ polling and Toggle Bit must be performed at an address within any of the sectors being erased.

Multiple Sector Erase Time; [Sector Erase Time + Sector Program Time (Preprogramming)] × Number of Sector Erase

Figure 17 illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Erase Suspend/Resume

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads from or programs to a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time-out period for sector erase. The Erase Suspend command will be ignored if written during the Chip Erase operation or Embedded Program Algorithm. Writting the Erase Suspend command (B0h) during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the Erase Resume command (30h) resumes the erase operation. The addresses are "Don't Care" when writting the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of "t_{SPD}" to suspend the erase operation. When the devices have entered the erase-suspended mode, the DQ_7 bit will be at logic "1" and DQ_6 will stop toggling. The user must use the address of the erasing sector for reading DQ_6 and DQ_7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the devices default to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ_2 to toggle. (See the section on DQ_2.)

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Program. This program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the devices are in the erase-suspend-program mode will cause DQ_2 to toggle. The end of the erase-suspended Program operation is detected by the $\overline{\text{Data}}$ polling of $\overline{DQ_7}$ or by the Toggle Bit I (DQ_6) which is the same as the regular Program operation. Note that DQ_7 must be read from the Program address while DQ_6 can be read from any address.

To resume the operation of Sector Erase, the Resume command (30h) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Extended Command

(1) Fast Mode

MBM29LV650UE/651UE has Fast Mode function. This mode dispenses with the initial two unclock cycles required in the standard program command sequence by writing Fast Mode command into the command register. In this mode, the required bus cycle for programming is two cycles instead of four bus cycles in standard program command. (Do not write erase command in this mode.) The read operation is also executed after exiting this mode. To exit this mode, it is necessary to write Fast Mode Reset command into the command register. (Refer to the Figure 22.) The V_{CC} active current is required even $\overline{CE}$ = V_{IH} during Fast Mode.

(2) Fast Programming

During Fast Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0h) and data write cycles (PA/PD). (Refer to the Figure 22.)

(3) Extended Sector Group Protection

In addition to normal sector group protection, the MBM29LV650UE/651UE has Extended Sector Group Protection as extended function. This function enable to protect sector group by forcing V_{ID} on $\overline{\text{RESET}}$ pin and write a command sequence. Unlike conventional procedure, it is not necessary to force V_{ID} and control timing for control pins. The only $\overline{\text{RESET}}$ pin requires V_{ID} for sector group protection in this mode. The extended sector group protection requires V_{ID} on $\overline{\text{RESET}}$ pin. With this condition, the operation is initiated by writing the set-up command (60h) into the command register. Then, the sector group addresses pins (A_{21}, A_{20}, A_{19}, A_{18}, and A_{17}) and (A_6, A_1, A_0) = (0, 1, 0) should be set to the sector group to be protected (recommend to set V_{IL} for the other addresses pins), and write extended sector group protection command (60h). A sector group is typically protected in 250 µs. To verify programming of the protection circuitry, the sector group addresses pins (A_{21}, A_{20}, A_{19}, A_{18}, and A_{17}) and (A_6, A_1, A_0) = (0, 1, 0) should be set and write a command (40h). Following the command write, a logical “1” at device output DQ_0 will produce for protected sector in the read operation. If the output data is logical “0”, please repeat to write extended sector group protection command (60h) again. To terminate the operation, it is necessary to set $\overline{\text{RESET}}$ pin to V_{IH}. (Refer to the Figures 14 and 23.)

(4) CFI (Common Flash Memory Interface)

The CFI (Common Flash Memory Interface) specification outlines device and host system software interrogation handshake which allows specific vendor-specified software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward-and backward-compatible software support for the specified flash device families. Refer to CFI specification in detail.

The operation is initiated by writing the query command (98h) into the command register. Following the command write, a read cycle from specific address retrieves device information. Please note that output data of upper byte (DQ_8 to DQ_{15}) is “0” in word mode (16 bit) read. Refer to the CFI code table. To terminate operation, it is necessary to write the read/reset command sequence into the register. (See Table 7.)

Hidden ROM (Hi-ROM) Region

The Hi-ROM feature provides a Flash memory region that the system may access through a new command sequence. This is primarily intended for customers who wish to use an Electronic Serial Number (ESN) in the device with the ESN protected against modification. Once the Hi-ROM region is programmed, any further modification of that region is impossible. This ensures the security of the ESN once the product is shipped to the field.

The Hi-ROM region is 128 words in length. After the system has written the Enter Hi-ROM command sequence, it may read the Hidden ROM region by using device addresses A_0 to A_6 (A_7 to A_{14} are “00”, A_{15} to A_{21} are don’t care). That is, the device sends only program command that would normally be sent to the address to the Hi-ROM region. This mode of operation continues until the system issues the Exit Hi-ROM command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the address.

If you request Fujitsu to program the ESN in the device, please contact a Fujitsu representative for more information.

Write Operation Status

Detailed in Table 8 are all the status flags that can be used to check the status of the device for current mode operation. During sector erase, the part provides the status flags automatically to the I/O ports. The information on DQ_2 is address sensitive. This means that if an address from an erasing sector is consecutively read, then the DQ_2 bit will toggle. However, DQ_2 will not toggle if an address from a non-erasing sector is consecutively read. This allows the user to determine which sectors are erasing and which are not.

Once erase suspend is entered, address sensitivity still applies. If the address of a non-erasing sector (that is, one available for read) is provided, then stored data can be read from the device. If the address of an erasing sector (that is, one unavailable for read) is applied, the device will output its status bits.

Table 8 Hardware Sequence Flags

Status			DQ_7	DQ_6	DQ_5	DQ_3	DQ_2
In Progress	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	0	0	1
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle*
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	0	0	1*
Exceeded Time Limits	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	1	0	1
	Embedded Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	1	0	N/A

*: Successive reads from the erasing or erase-suspend sector will cause DQ_2 to toggle. Reading from non-erase suspend sector address will indicate logic “1” at the DQ_2 bit.

Notes: 1. DQ_0 and DQ_1 are reserve pins for future use.
2. DQ_4 is Fujitsu internal use only.

DQ_7

$\overline{\text{Data}}$ Polling

The MBM29LV650UE/651UE devices feature $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read the devices will produce the complement of the data last written to DQ_7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ_7. During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ_7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a "1" at the DQ_7 output. The flowchart for $\overline{\text{Data}}$ Polling (DQ_7) is shown in Figure 18.

For programming, the $\overline{\text{Data}}$ Polling is valid after the rising edge of fourth write pulse in the four write pulse sequence.

For chip erase and sector erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth write pulse in the six write pulse sequence. $\overline{\text{Data}}$ Polling must be performed at sector address within any of the sectors being erased and not a protected sector. Otherwise, the status may not be valid.

Once the Embedded Algorithm operation is close to being completed, the MBM29LV650UE/651UE data pins (DQ_7) may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that the devices are driving status information on DQ_7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ_7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and DQ_7 has a valid data, the data outputs on DQ_0 to DQ_6 may be still invalid. The valid data on DQ_0 to DQ_7 will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out. (See Table 8.)

See Figure 9 for the $\overline{\text{Data}}$ Polling timing specifications and diagram.

DQ_6

Toggle Bit I

The MBM29LV650UE/651UE also feature the "Toggle Bit I" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{OE}}$ toggling) data from the devices will result in DQ_6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ_6 will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth write pulse in the four write pulse sequence. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth write pulse in the six write pulse sequence. The Toggle Bit I is active during the sector time out.

In programming, if the sector being written to is protected, the toggle bit will toggle for about 1 µs and then stop toggling without the data having changed. In erase, the devices will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 400 µs and then drop back into read mode, having changed none of the data.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause the DQ_6 to toggle. In addition, an Erase Suspend/Resume command will cause the DQ_6 to toggle.

See Figure 10 for the Toggle Bit I timing specifications and diagram.

DQ_5

Exceeded Timing Limits

DQ_5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ_5 will produce a “1”. This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the devices under this condition. The $\overline{\text{CE}}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in Table 2.

The DQ_5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the devices lock out and never complete the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ_7 bit and DQ_6 never stops toggling. Once the devices have exceeded timing limits, the DQ_5 bit will indicate a “1”. Please note that this is not a device failure condition since the devices were incorrectly used. If this occurs, reset the device with command sequence.

DQ_3

Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ_3 will remain low until the time-out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit I indicates the device has been written with a valid erase command, DQ_3 may be used to determine if the sector erase timer window is still open. If DQ_3 is high (“1”) the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit I. If DQ_3 is low (“0”), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ_3 prior to and following each subsequent Sector Erase command. If DQ_3 were high on the second status check, the command may not have been accepted.

See Table 8 : Hardware Sequence Flags.

DQ_2

Toggle Bit II

This toggle bit II, along with DQ_6, can be used to determine whether the devices are in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ_2 to toggle during the Embedded Erase Algorithm. If the devices are in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ_2 to toggle. When the devices are in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic “1” at the DQ_2 bit.

DQ_6 is different from DQ_2 in that DQ_6 toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ_7, is summarized as follows:

For example, DQ_2 and DQ_6 can be used together to determine if the erase-suspend-read mode is in progress. (DQ_2 toggles while DQ_6 does not.) See also Table 9 and Figure 11.

Furthermore, DQ_2 can also be used to determine which sector is being erased. When the device is in the erase mode, DQ_2 toggles if this bit is read from an erasing sector.

Table 9 Toggle Bit Status

Mode	DQ_7	DQ_6	DQ_2
Program	$\overline{DQ_7}$	Toggle	1
Erase	0	Toggle	Toggle *
Erase-Suspend Read (Erase-Suspended Sector)	1	1	Toggle
Erase-Suspend Program	$\overline{DQ_7}$	Toggle	1 *

*: Successive reads from the erasing or erase-suspend sector will cause DQ_2 to toggle. Reading from non-erase suspend sector address will indicate logic “1” at the DQ_2 bit.

Data Protection

The MBM29LV650UE/651UE is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the devices automatically reset the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences. The devices also incorporate several features to prevent inadvertent write cycles resulting form V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than V_{LKO} (min). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above V_{LKO} (min).

If Embedded Erase Algorithm is interrupted, there is possibility that the erasing sector(s) cannot be used.

Write Pulse “Glitch” Protection

Noise pulses of less than 3 ns (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$, or $\overline{WE} = V_{IH}$. To initiate a write, $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-up Write Inhibit

Power-up of the devices with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to read mode on power-up.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	T_A	–40	+85	°C
Voltage with Respect to Ground All Pins Except A_9, $\overline{OE}$, ACC, and $\overline{RESET}$ (Note 1)	V_{IN}, V_{OUT}	–0.5	V_{CC} +0.5	V
Power Supply Voltage (Note 1)	V_{CC}	–0.5	+4.0	V
A_9, $\overline{OE}$, ACC, and $\overline{RESET}$ (Note 2)	V_{IN}	–0.5	+13.0	V
Power Supply Voltage	$V_{CC}q$	–0.2	+7.0	V

Notes: 1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

2. Minimum DC input voltage on A_9, $\overline{OE}$, ACC, and $\overline{RESET}$ pins is –0.5 V. During voltage transitions, A_9, $\overline{OE}$, ACC, and $\overline{RESET}$ pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V_{IN}–V_{CC}) does not exceed 9.0 V. Maximum DC input voltage on A_9, $\overline{OE}$, ACC, and $\overline{RESET}$ pins is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Value		Unit
			Min.	Max.	
Ambient Temperature	(-90/-12)	T_A	–40	+85	°C
Power Supply Voltage (V_{CC})	(-90)	V_{CC}	+3.0	+3.6	V
	(-12)		+2.7	+3.6	V
Power Supply Voltage ($V_{CC}q$)	(-90/-12)	$V_{CC}q$	+2.7	+3.6	V

Note: Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses , operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ MAXIMUM OVERSHOOT/UNDERSHOOT

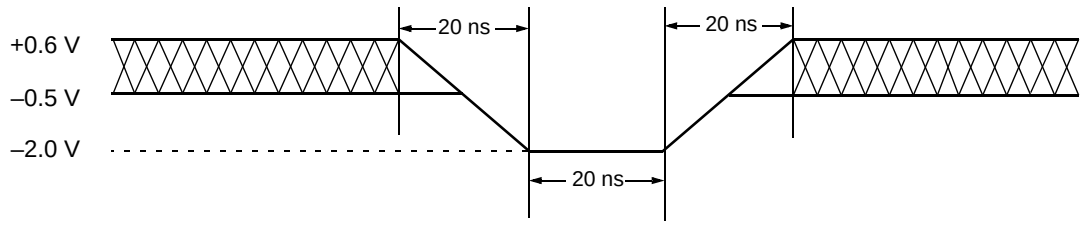


Figure 1 Maximum Undershoot Waveform

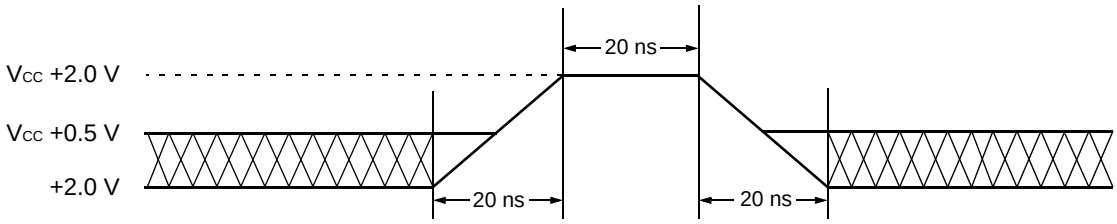
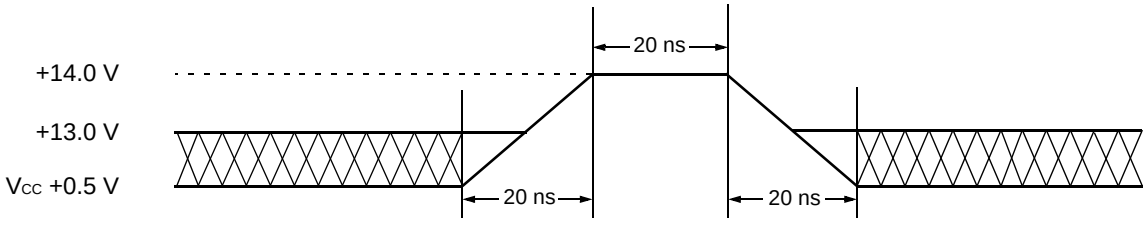


Figure 2 Maximum Overshoot Waveform 1



Note: This waveform is applied for A_9, $\overline{OE}$, ACC, and $\overline{RESET}$.

Figure 3 Maximum Overshoot Waveform 2

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max., V_{CCq} = V_{CCq} Max.	–1.0	+1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max., V_{CCq} = V_{CCq} Max.	–1.0	+1.0	µA
I_{LIT}	A_9, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	V_{CC} = V_{CC} Max., A_9, $\overline{OE}$, $\overline{RESET}$ = 12.5 V	—	35	µA
I_{ACC}	ACC Accelerated Program Current	V_{CC} = V_{CC} Max., ACC = V_{ACC} Max.	—	20	mA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, V_{CC} = V_{CC} Max., V_{CCq} = V_{CCq} Max., f = 5 MHz	—	16	mA
		$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, V_{CC} = V_{CC} Max., V_{CCq} = V_{CCq} Max., f = 1 MHz	—	7	mA
I_{CC2}	V_{CC} Active Current (Note 2)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, V_{CC} = V_{CC} Max., V_{CCq} = V_{CCq} Max.	—	40	mA
I_{CC3}	V_{CC} Current (Standby)	V_{CC} = V_{CC} Max., V_{CCq} = V_{CCq} Max., $\overline{CE}$ = V_{CC} ±0.3 V, $\overline{RESET}$ = V_{CC} ±0.3 V	—	5	µA
I_{CC4}	V_{CC} Current (Standby, $\overline{RESET}$)	V_{CC} = V_{CC} Max., V_{CCq} = V_{CCq} Max., $\overline{RESET}$ = V_{SS} ±0.3 V	—	5	µA
I_{CC5}	V_{CC} Current (Automatic Sleep Mode) (Note 3)	V_{CC} = V_{CC} Max., V_{CCq} = V_{CCq} Max., $\overline{CE}$ = V_{SS} ±0.3 V, $\overline{RESET}$ = V_{CC} ±0.3 V, V_{IN} = V_{CC} ±0.3 V or V_{SS} ±0.3 V	—	5	µA
V_{IL}	Input Low Level	—	–0.5	0.6	V
V_{IH}	Input High Level	—	2.0	V_{CC} + 0.5	V
V_{ACC}	Voltage for Program Acceleration	—	11.5	12.5	V
V_{ID}	Voltage for Autoselect, Sector Protection (A_9, $\overline{OE}$, $\overline{RESET}$) (Note 4)	—	11.5	12.5	V
V_{OL}	Output Low Voltage Level	I_{OL} = 4.0 mA, V_{CC} = V_{CC} Min., V_{CCq} = V_{CCq} Min.	—	0.45	V
V_{OH1}	Output High Voltage Level	I_{OH} = –2.0 mA, V_{CC} = V_{CC} Min., V_{CCq} = V_{CCq} Min.	2.4	—	V
V_{OH2}		I_{OH} = –100 µA, V_{CC} Min., V_{CCq} = V_{CCq} Min.	V_{CCq} – 0.4	—	V
V_{LKO}	Low V_{CC} Lock-Out Voltage	—	2.3	2.5	V

Notes: 1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component.
2. I_{CC} active while Embedded Erase or Embedded Program is in progress.
3. Automatic sleep mode enables the low power mode when address remain stable for 150 ns.
4. Applicable for only V_{CC} applying.

2. AC Characteristics

- **Read Only Operations Characteristics**

Parameter Symbols		Description	Test Setup		90 (Note)	12 (Note)	Unit
JEDEC	Standard						
t_{AVAV}	t_{RC}	Read Cycle Time	—	Min.	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max.	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Max.	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	—	Max.	35	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output HIGH-Z	—	Max.	30	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output HIGH-Z	—	Max.	30	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Address, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First	—	Min.	0	0	ns
—	t_{READY}	$\overline{RESET}$ Pin Low to Read Mode	—	Max.	20	20	µs

Note: Test Conditions:

Output Load: 1 TTL gate and 30 pF (MBM29LV650UE/651UE-90)
1 TTL gate and 100 pF (MBM29LV650UE/651UE-12)
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to 3.0 V
Timing measurement reference level
Input: 1.5 V
Output: 1.5 V

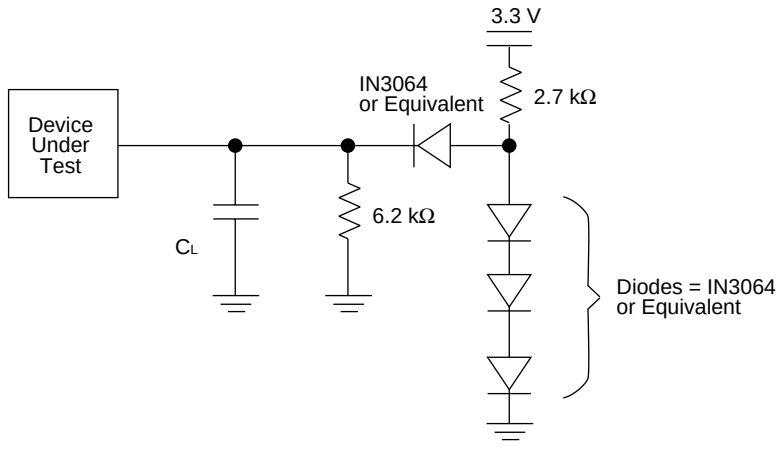


Figure 4 Test Conditions

• **Write (Erase/Program) Operations**

Parameter Symbols		Description			90	12	Unit
JEDEC	Standard						
t_{AVAV}	t_{WC}	Write Cycle Time		Min.	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min.	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min.	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min.	35	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min.	0	0	ns
—	t_{OES}	Output Enable Setup Time		Min.	0	0	ns
—	t_{OEH}	Output Enable Hold Time	Read	Min.	0	0	ns
			Toggle and $\overline{\text{Data}}$ Polling	Min.	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write		Min.	0	0	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write		Min.	0	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time		Min.	0	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time		Min.	0	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time		Min.	0	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		Min.	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min.	35	50	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width		Min.	35	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min.	30	30	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High		Min.	30	30	ns
t_{WHWH1}	t_{WHWH1}	Word Programming Operation		Typ.	16	16	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)		Typ.	1	1	s
—	t_{VCS}	V_{CC} Setup Time		Min.	50	50	µs
—	t_{VIDR}	Rise Time to V_{ID} (Note 2)		Min.	500	500	ns
—	t_{VACCR}	Rise Time to V_{ACC} (Note 3)		Min.	500	500	ns
—	t_{VLHT}	Voltage Transition Time (Note 2)		Min.	4	4	µs
—	t_{WPP}	Write Pulse Width (Note 2)		Min.	100	100	µs
—	t_{OESP}	$\overline{OE}$ Setup Time to $\overline{WE}$ Active (Note 2)		Min.	4	4	µs
—	t_{CSP}	$\overline{CE}$ Setup Time to $\overline{WE}$ Active (Note 2)		Min.	4	4	µs
—	t_{RP}	$\overline{RESET}$ Pulse Width		Min.	500	500	ns
—	t_{RH}	$\overline{RESET}$ Hold Time Before Read		Min.	200	200	ns

(Continued)

(Continued)

Parameter Symbols		Description		90	12	Unit
JEDEC	Standard					
—	t_{EOE}	Delay Time from Embedded Output Enable	Max.	90	120	ns
—	t_{TOW}	Erase Time-out Time	Min.	50	50	µs
—	t_{SPD}	Erase Suspend Transition Time	Max.	20	20	µs

Notes: 1. This does not include the preprogramming time.
2. This timing is for Sector Group Protection operation.
3. This timing is for Accelerated Program operation.

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Sector Erase Time	—	1	10	s	Excludes programming time prior to erasure
Programming Time	—	16	360	µs	Excludes system-level overhead
Chip Programming Time	—	—	200	s	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycle	—

■ PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	8	10	pF
C_{IN3}	ACC Pin Capacitance	V_{IN} = 0	15	20	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ TIMING DIAGRAM

- **Key to Switching Waveforms**

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	"H" or "L" Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

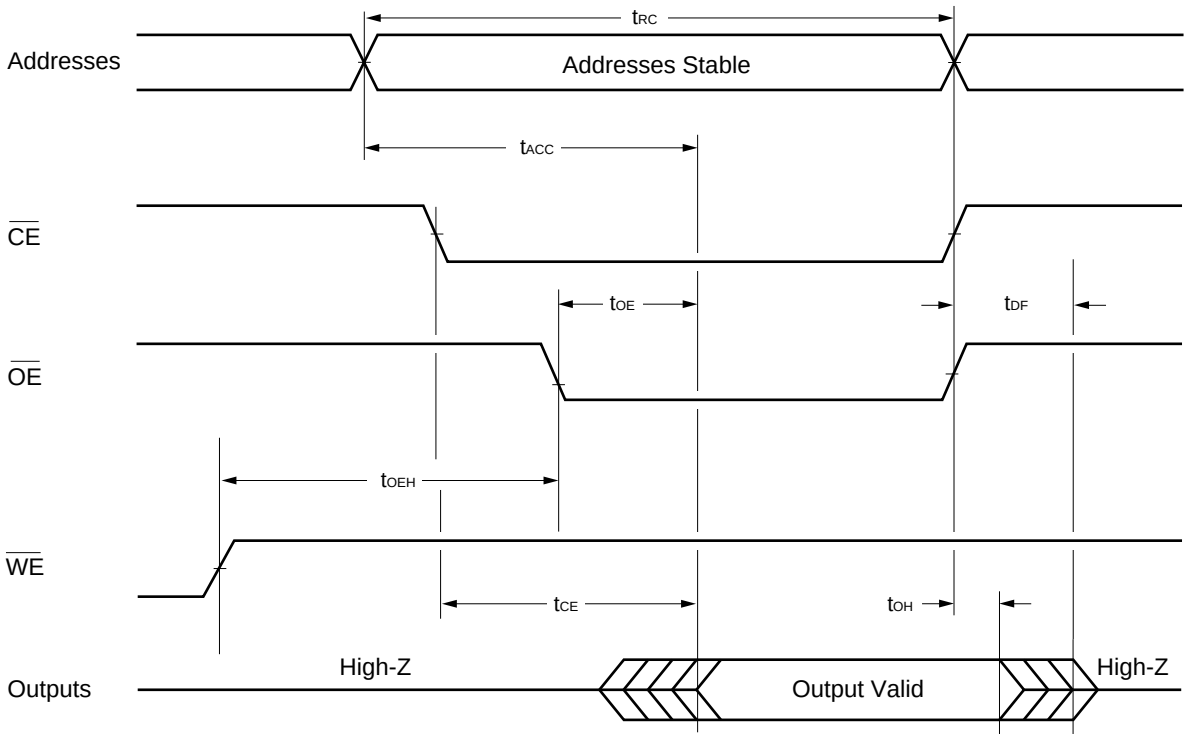


Figure 5.1 Read Operation Timing Diagram

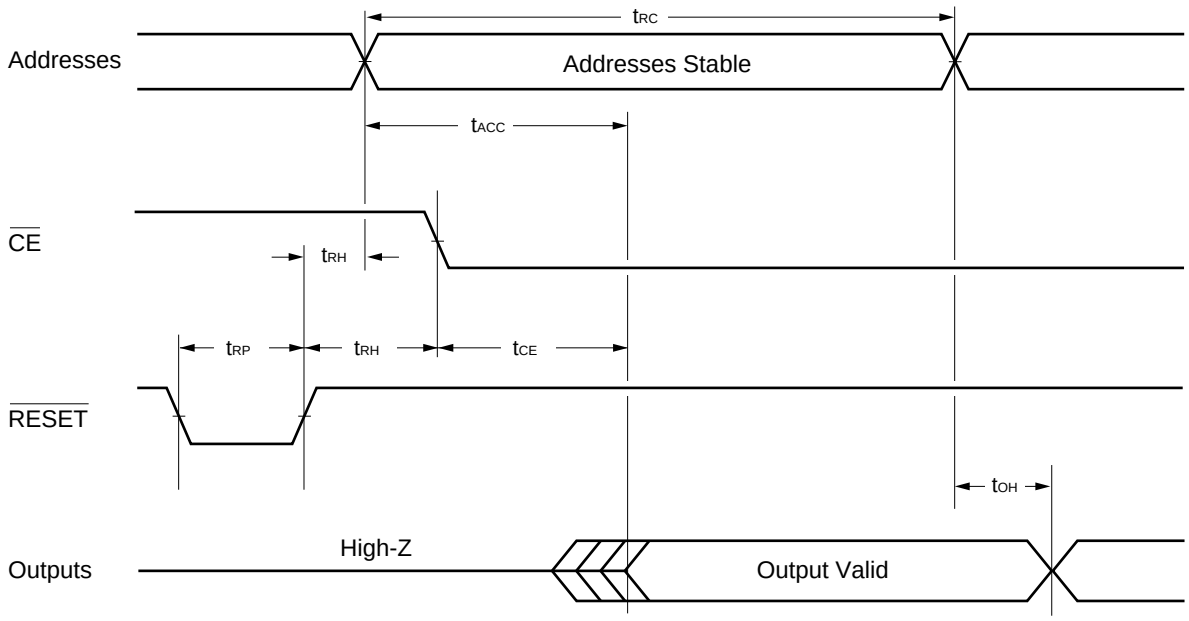
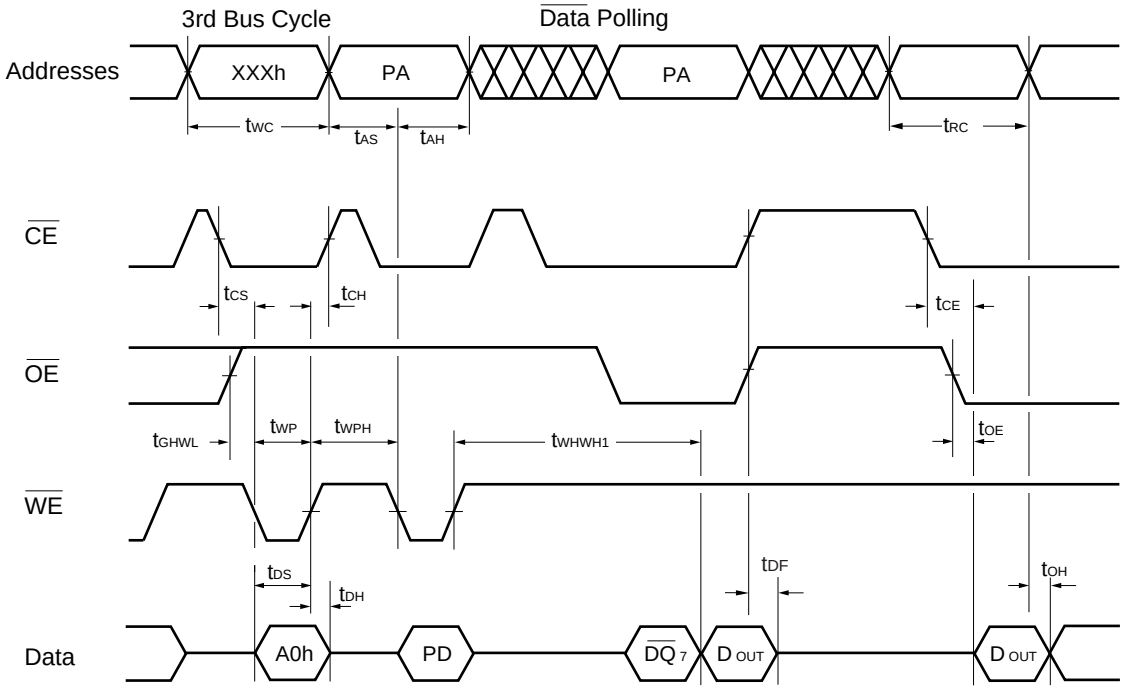
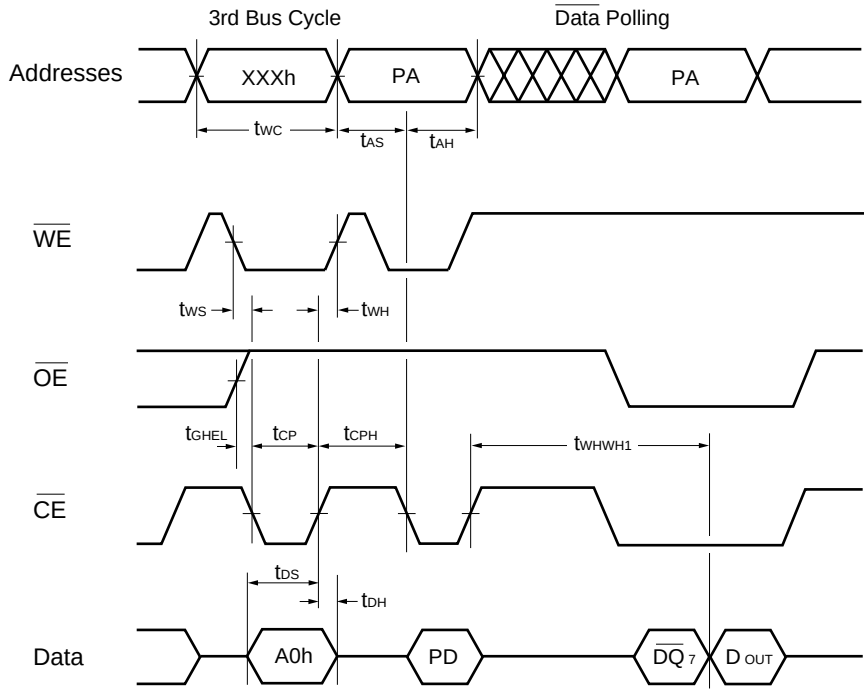


Figure 5.2 Hardware Reset/Read Operation Timing Diagram



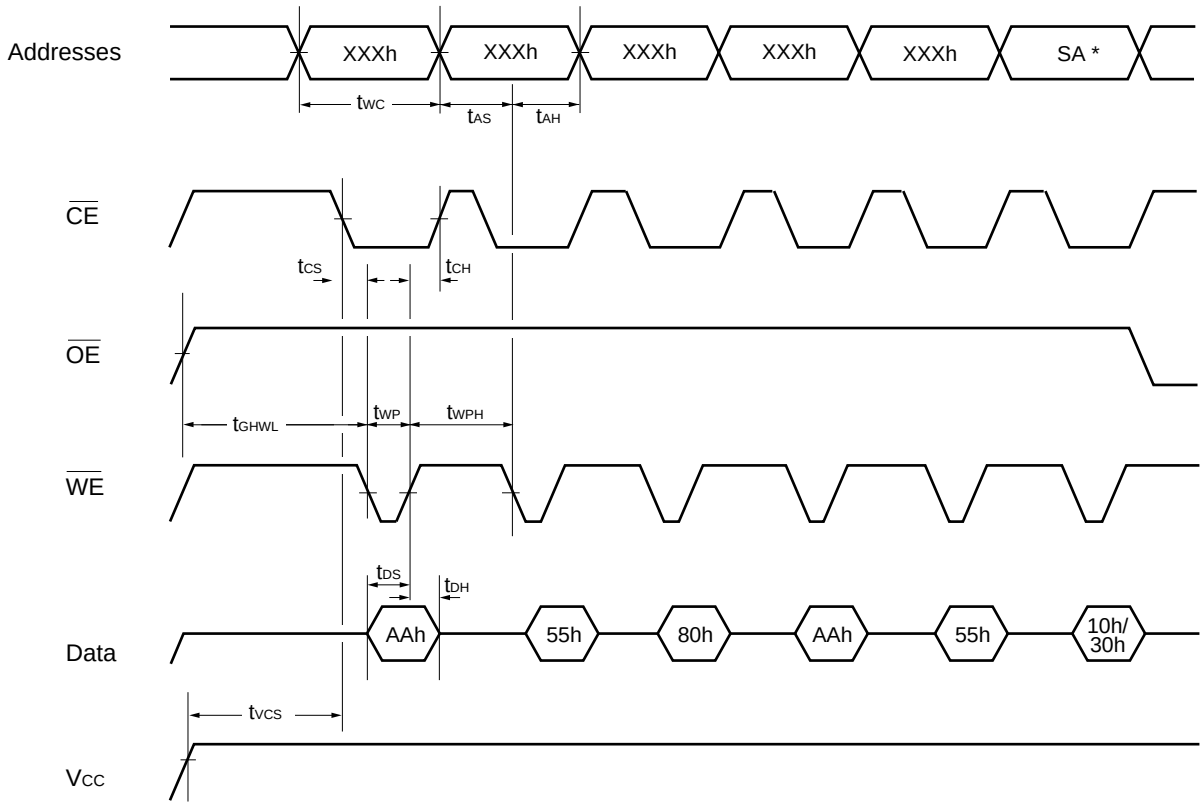
Notes: 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.

Figure 6 Alternate $\overline{WE}$ Controlled Program Operation Timing Diagram



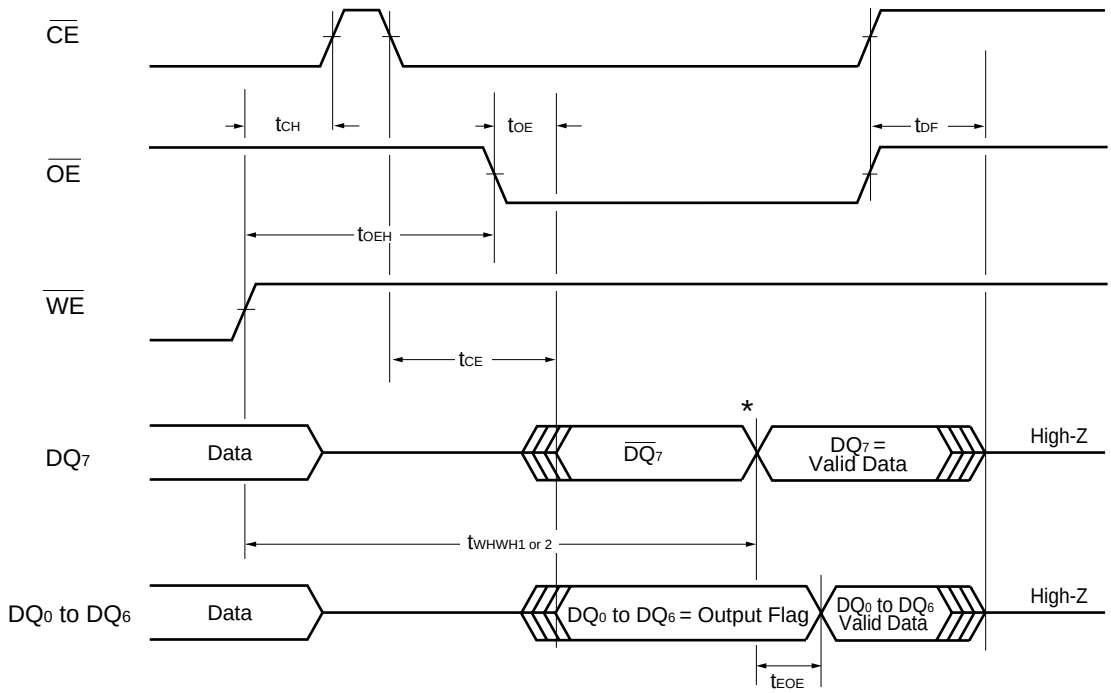
Notes: 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ}_7$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.

Figure 7 Alternate $\overline{CE}$ Controlled Program Operation Timing Diagram



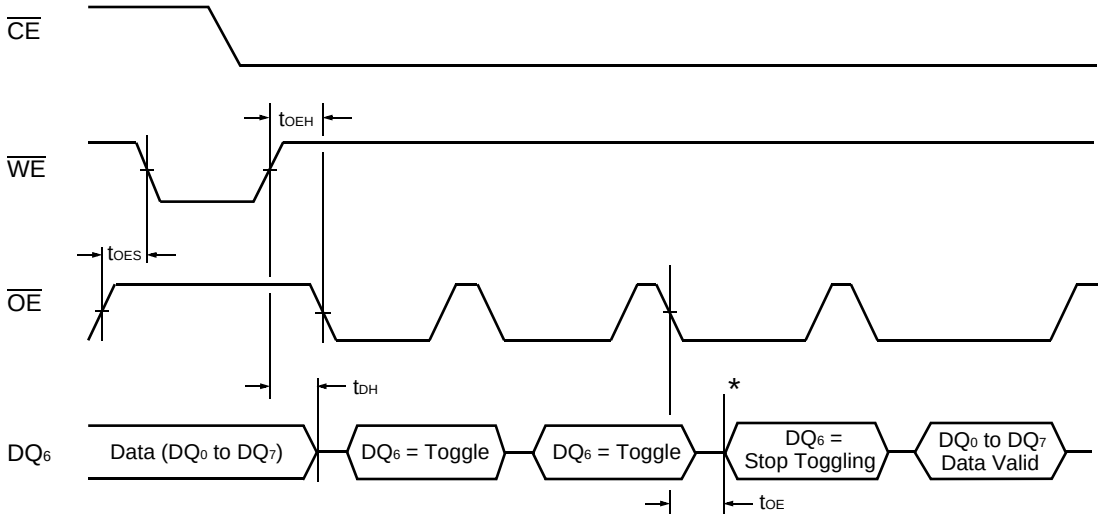
* : SA is the sector address for Sector Erase. Addresses = XXXh for Chip Erase.

Figure 8 Chip/Sector Erase Operation Timing Diagram



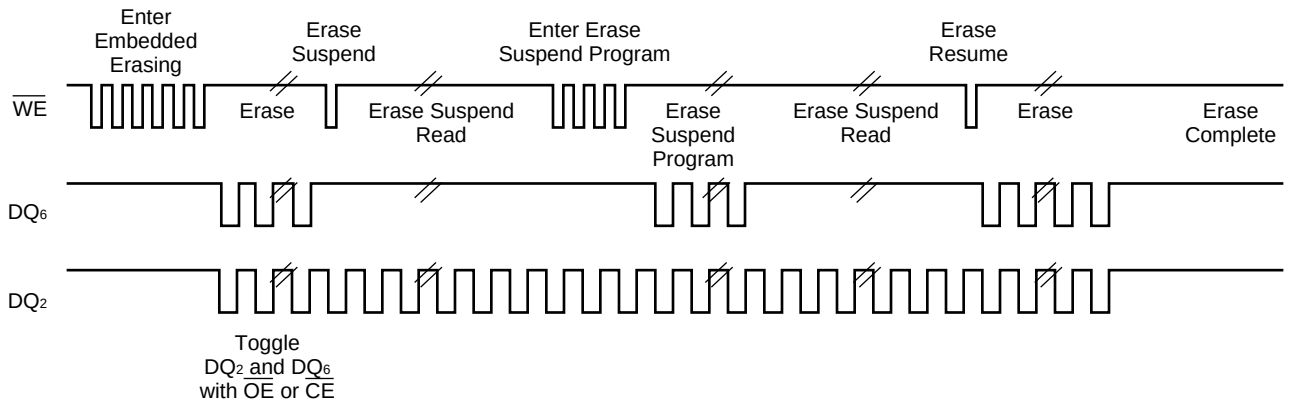
* : DQ_7 = Valid Data (The device has completed the Embedded operation.)

Figure 9 $\overline{\text{Data}}$ Polling during Embedded Algorithm Operation Timing Diagram



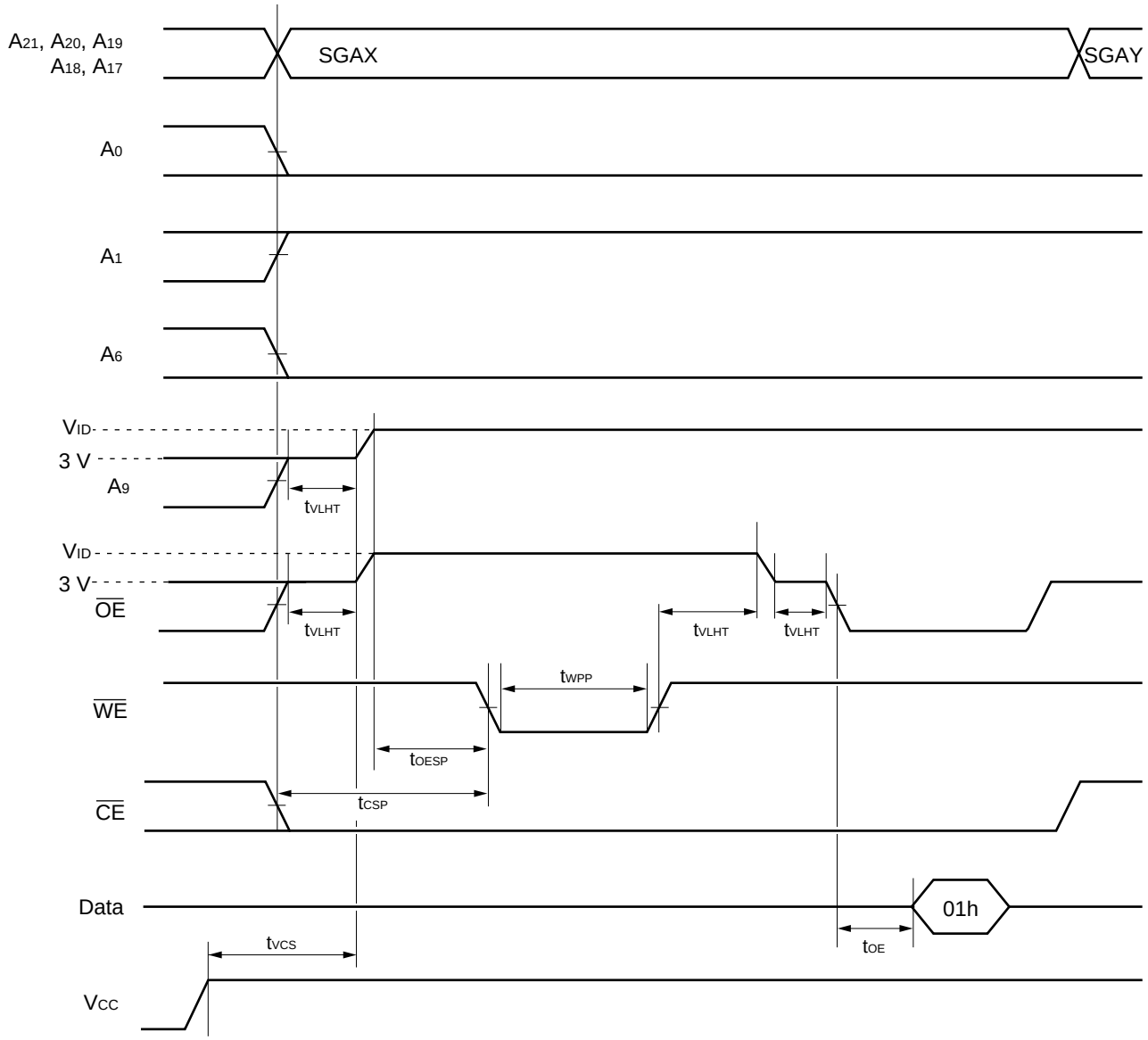
* : DQ_6 = Stops toggling. (The device has completed the Embedded operation.)

Figure 10 Toggle Bit I during Embedded Algorithm Operation Timing Diagram



Note: DQ_2 is read from the erase-suspended sector.

Figure 11 DQ_2 vs. DQ_6



SGAX = Sector Group Address for initial sector
SGAY = Sector Group Address for next sector

Figure 12 Sector Group Protection Timing Diagram

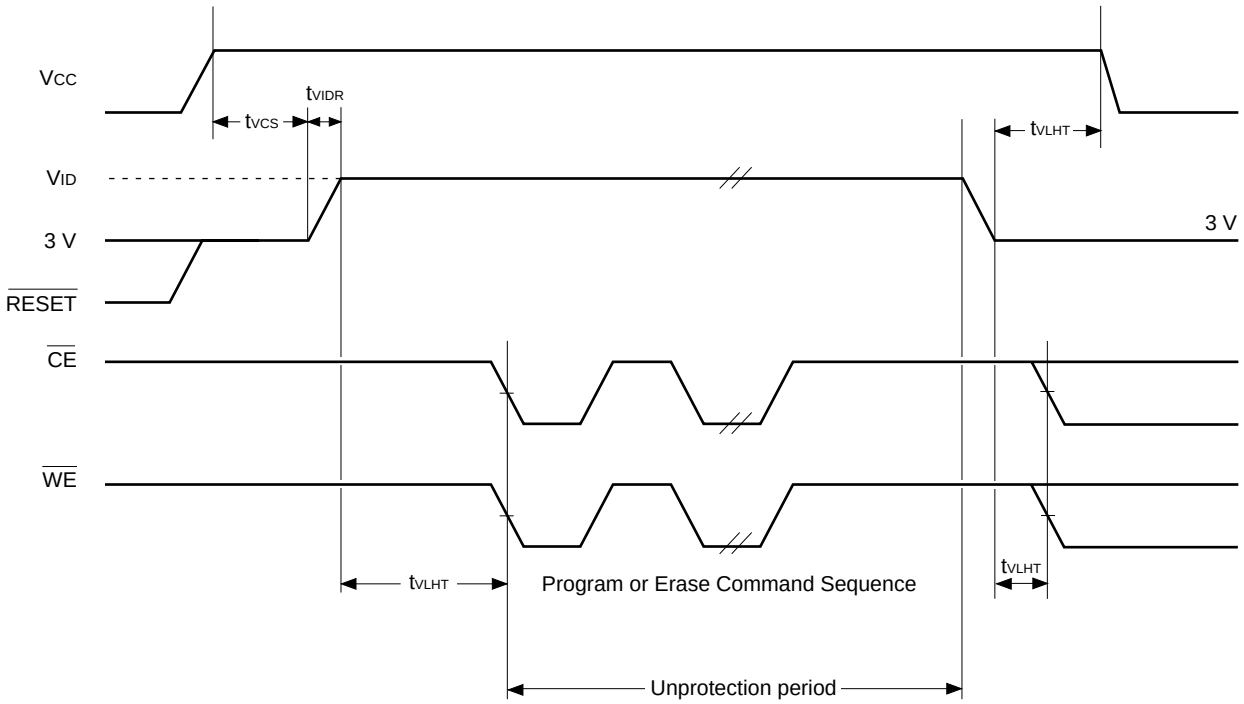
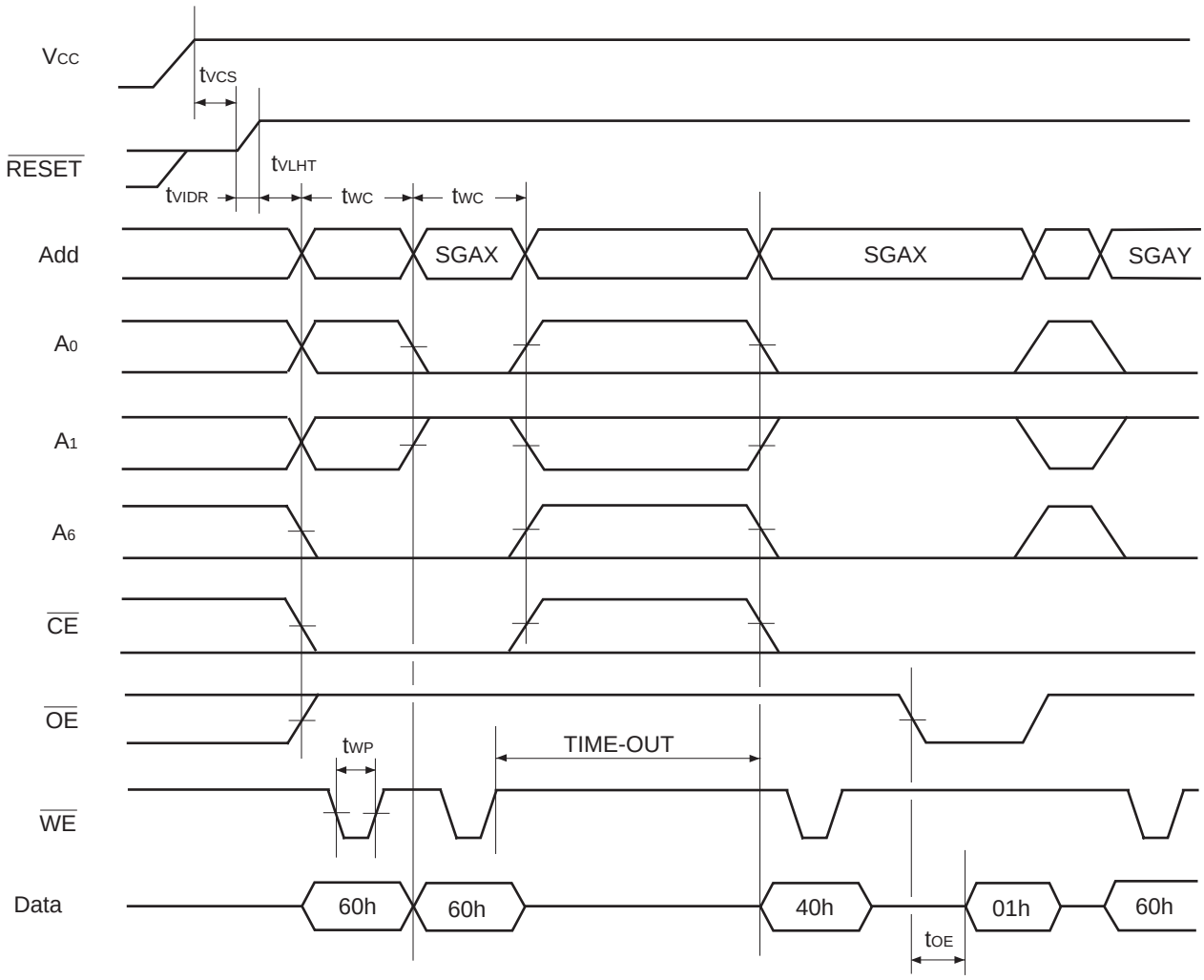


Figure 13 Temporary Sector Group Unprotection Timing Diagram



SGAX: Sector Group Address to be protected
SGAY : Next Sector Group Address to be protected
TIME-OUT : Time-Out window = 250 μs (min)

Figure 14 Extended Sector Group Protection Timing Diagram

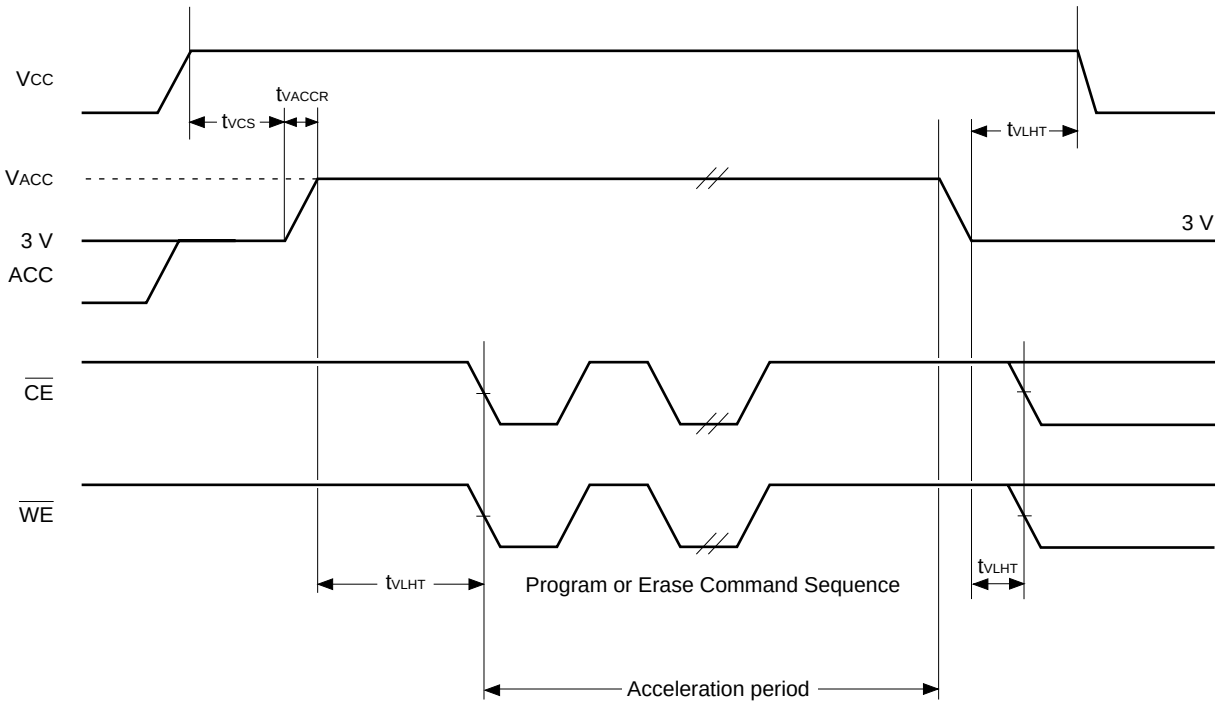
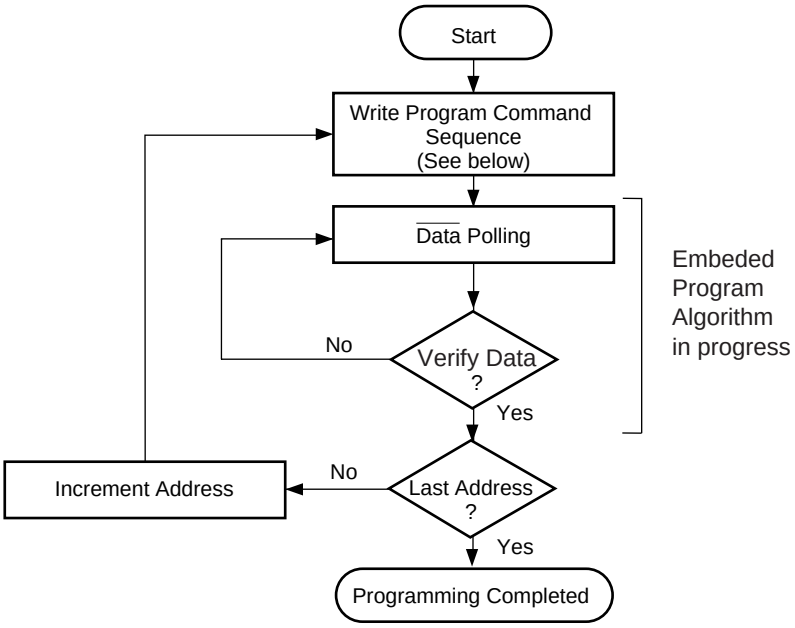


Figure 15 Accelerated Program Timing Diagram

■ FLOW CHART

EMBEDDED ALGORITHMS



Program Command Sequence (Address/Command):

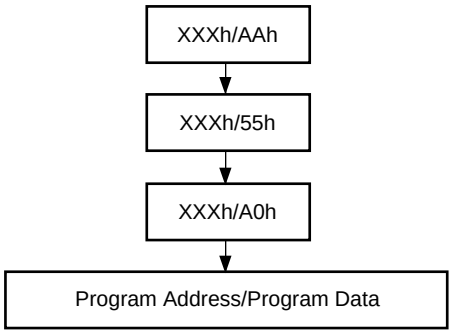


Figure 16 Embedded Program™ Algorithm

EMBEDDED ALGORITHMS

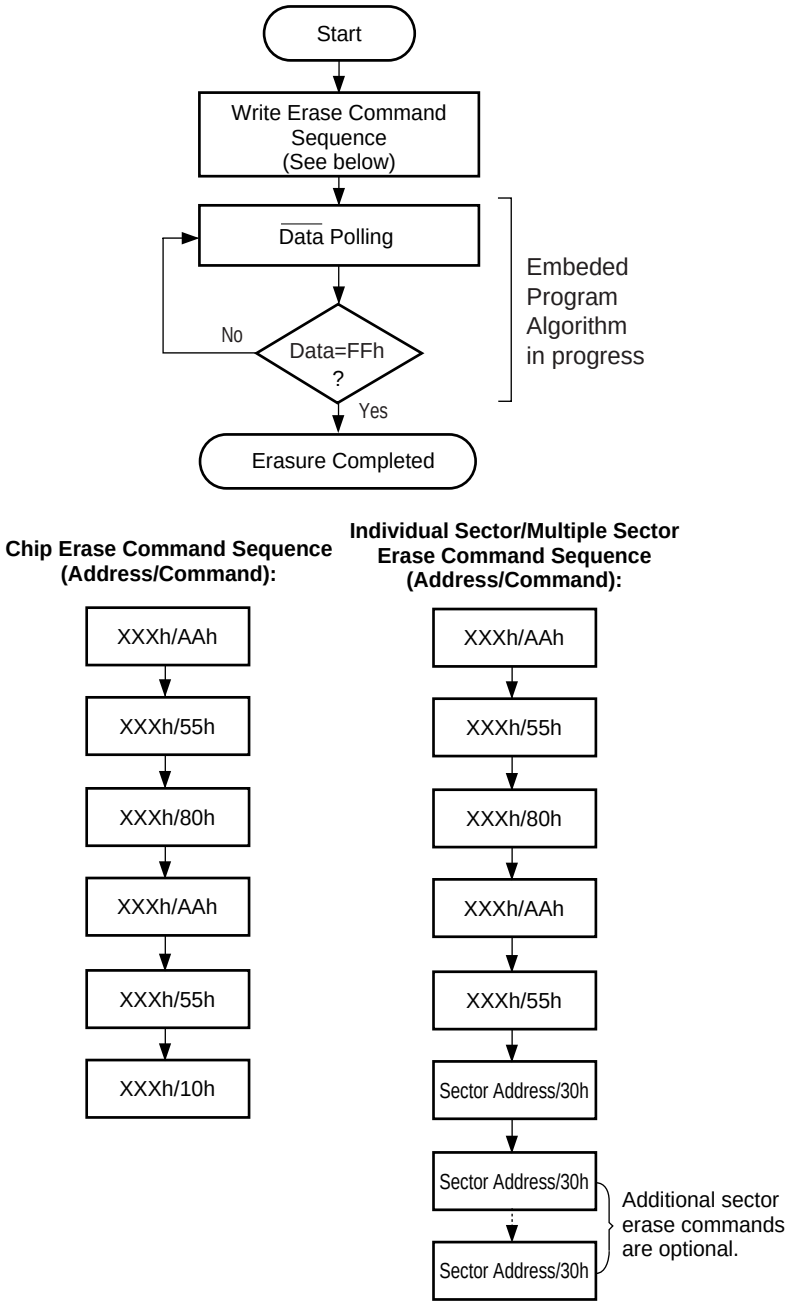
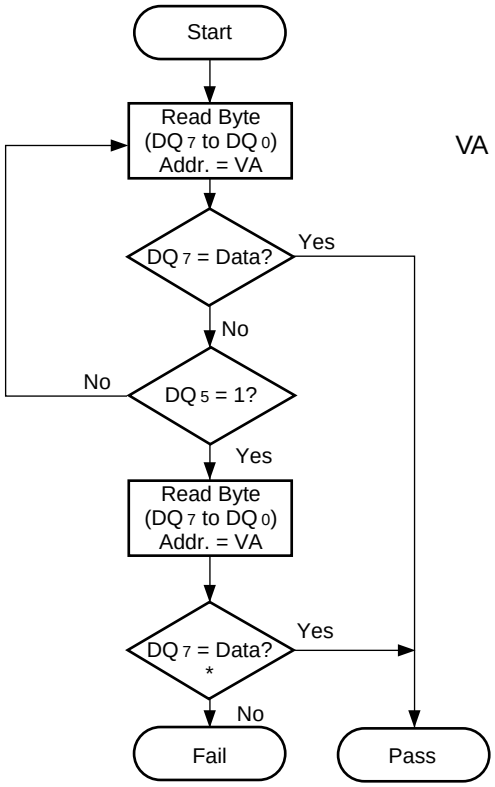


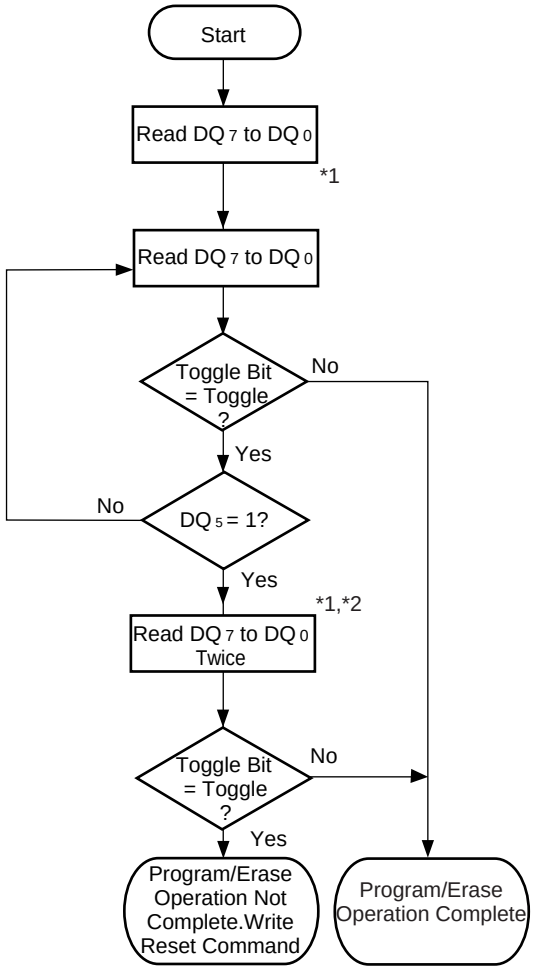
Figure 17 Embedded Erase™ Algorithm



VA = Byte address for programming
= Any of the sector addresses within the sector being erased during sector erase or multiple sector erases operation
= Any of the sector addresses within the sector not being protected during chip erase

* DQ_7 is rechecked even if DQ_5 = “1” because DQ_7 may change simultaneously with DQ_5.

Figure 18 $\overline{\text{Data}}$ Polling Algorithm



*1:Reset toggle bit twice to determine whether or not it is toggle.

*2:Recheck toggle bit because it may stop toggle as DQ5 changes to “1” .

Figure 19 Toggle Bit Algorithm

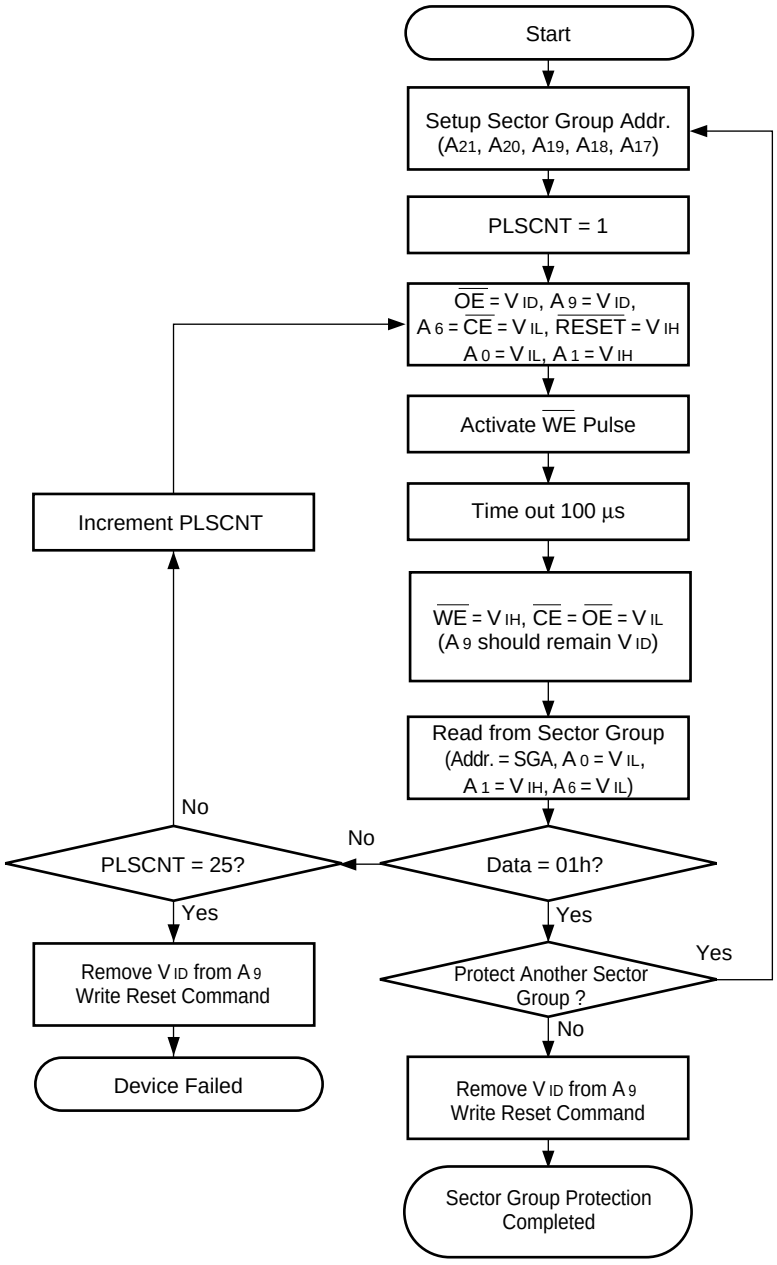
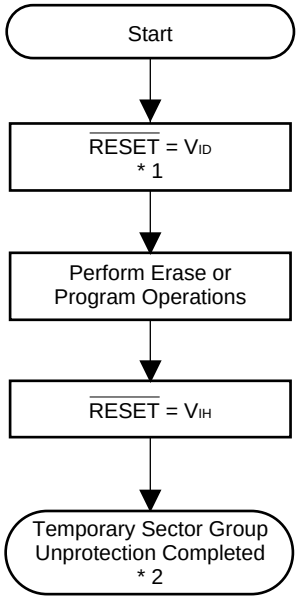


Figure 20 Sector Group Protection Algorithm



*1: All protected sector groups are unprotected.

*2: All previously protected sector groups are protected once again.

Figure 21 Temporary Sector Group Unprotection Algorithm

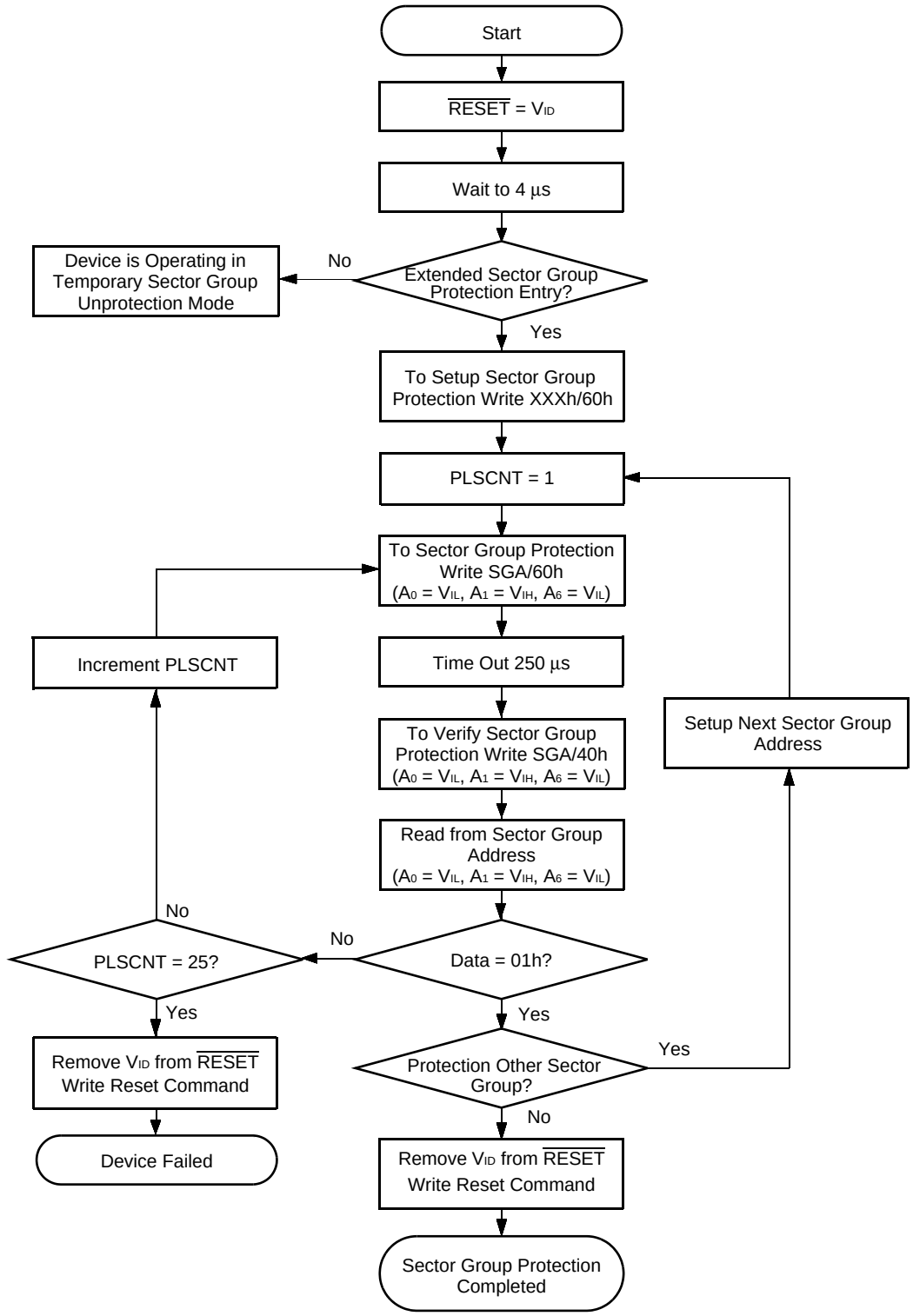


Figure 22 Extended Sector Group Protection Algorithm

FAST MODE ALGORITHM

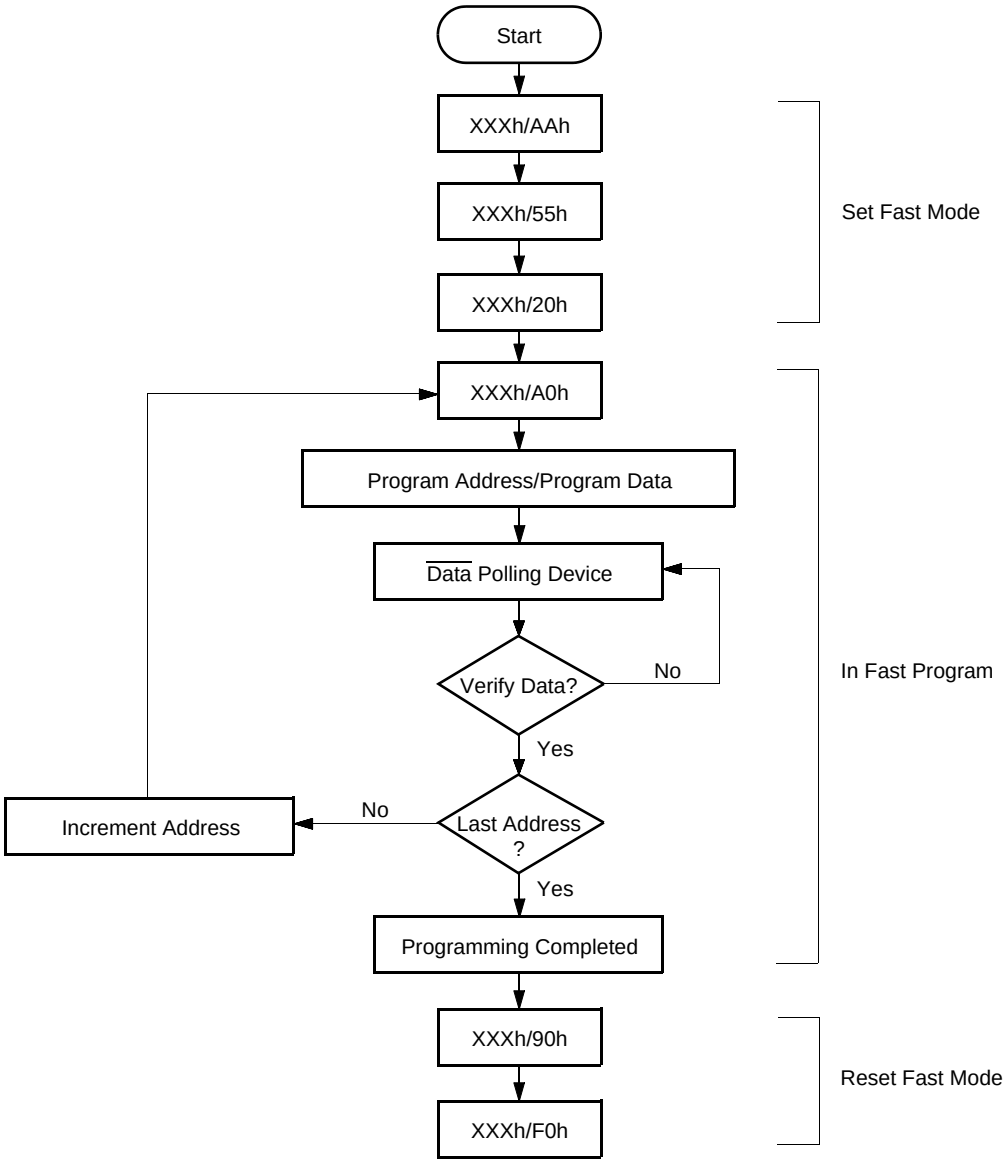


Figure 23 Embedded Program™ Algorithm for Fast Mode

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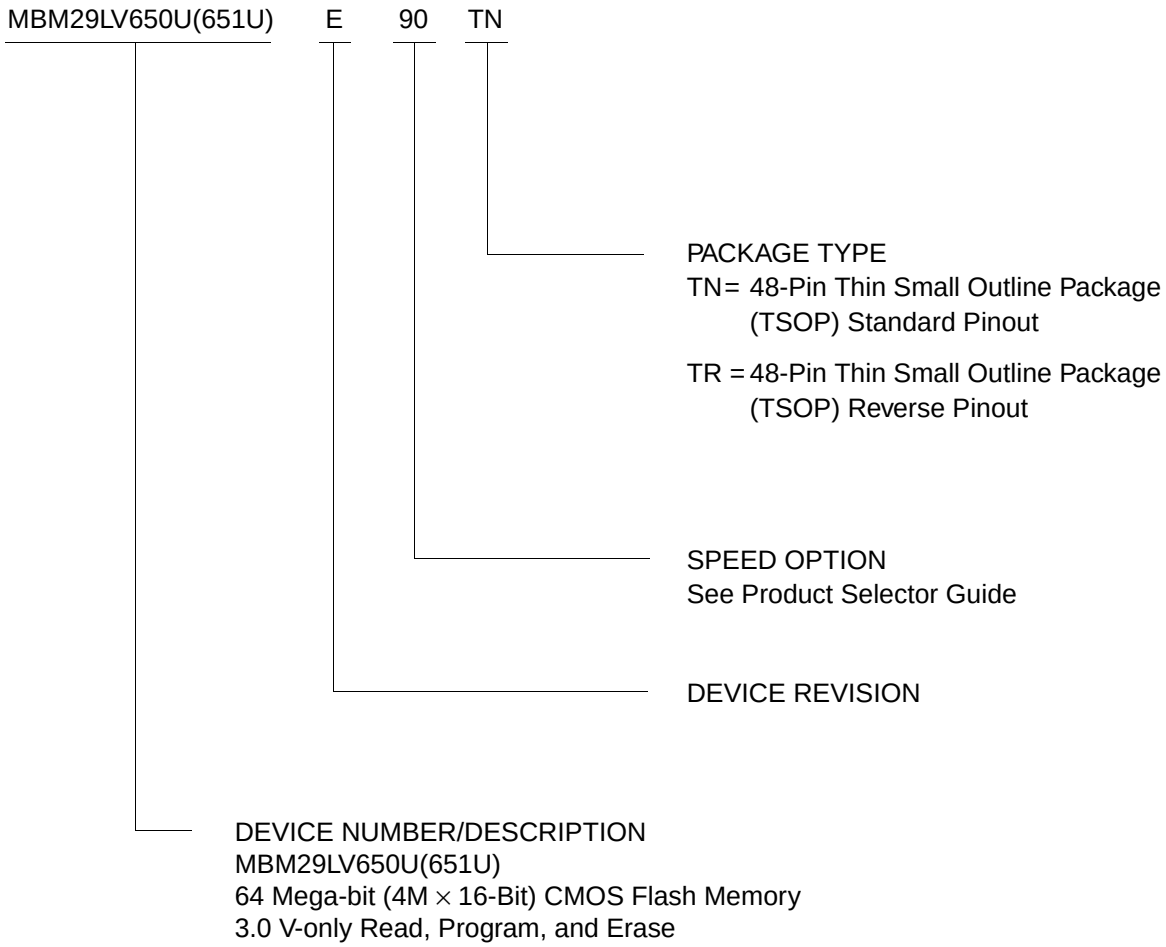
Standard Products

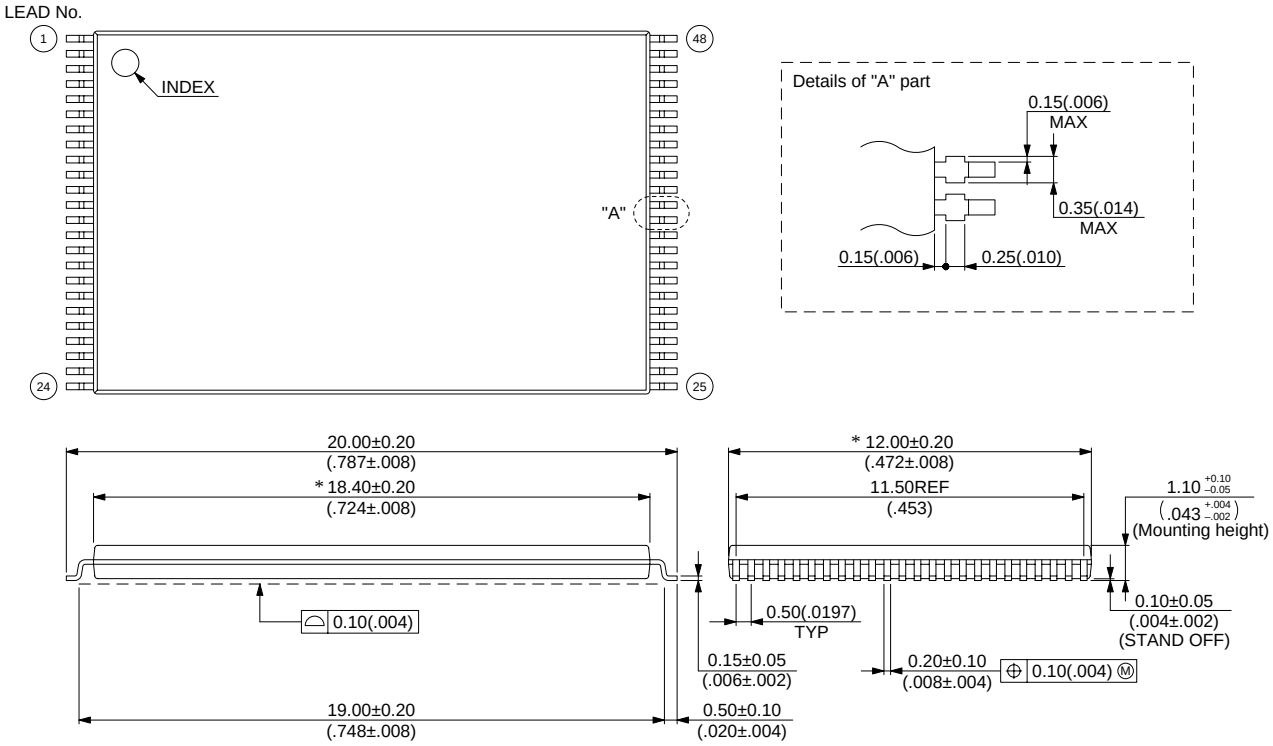
Fujitsu standard products are available in several packages. The order number is formed by a combination of:



■ PACKAGE DIMENSIONS

48-pin plastic TSOP (I)
(FPT-48P-M19)

*: Resin protrusion. (Each side: 0.15(.006) Max)



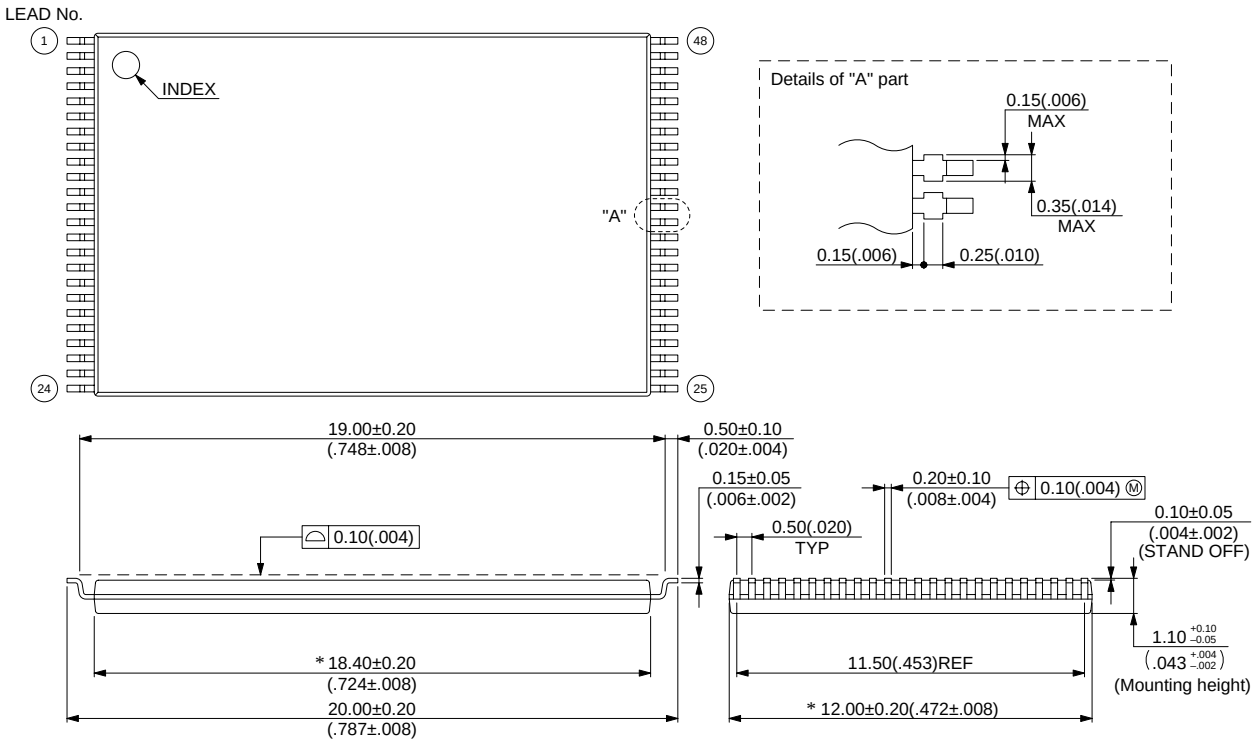
Dimensions in mm (inches)

(Continued)

(Continued)

48-pin plastic TSOP (I)
(FPT-48P-M20)

*: Resin protrusion. (Each side: 0.15(.006) Max)



Dimensions in mm (inches)

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
Shinjuku Dai-Ichi Seimei Bldg. 7-1,
Nishishinjuku 2-chome, Shinjuku-ku,
Tokyo 163-0721, Japan
Tel: +81-3-5322-3347
Fax: +81-3-5322-3386

http://edevice.fujitsu.com/

North and South America

FUJITSU MICROELECTRONICS, INC.
3545 North First Street,
San Jose, CA 95134-1804, U.S.A.
Tel: +1-408-922-9000
Fax: +1-408-922-9179

Customer Response Center
Mon. - Fri.: 7 am - 5 pm (PST)
Tel: +1-800-866-8608
Fax: +1-408-922-9179

http://www.fujitsumicro.com/

Europe

FUJITSU MICROELECTRONICS EUROPE GmbH
Am Siebenstein 6-10,
D-63303 Dreieich-Buchschlag,
Germany
Tel: +49-6103-690-0
Fax: +49-6103-690-122

http://www.fujitsu-fme.com/

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE. LTD.
#05-08, 151 Lorong Chuan,
New Tech Park,
Singapore 556741
Tel: +65-281-0770
Fax: +65-281-0220

http://www.fmap.com.sg/

Korea

FUJITSU MICROELECTRONICS KOREA LTD.
1702 KOSMO TOWER, 1002 Daechi-Dong,
Kangnam-Gu,Seoul 135-280
Korea
Tel: +82-2-3484-7100
Fax: +82-2-3484-7111

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