

## Section 20 Electrical Specifications

### 20.1 Absolute Maximum Ratings

Table 20-1 lists the absolute maximum ratings.

**Table 20-1 Absolute Maximum Ratings**

Item	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	-0.3 to +7.0	V
Programming voltage	V <sub>PP</sub>	-0.3 to +13.5	V
Input voltage (except port 8)	V <sub>in</sub>	-0.3 to V <sub>CC</sub> + 0.3	V
(port 8)	V <sub>in</sub>	-0.3 to AV <sub>CC</sub> + 0.3	V
Analog supply voltage	AV <sub>CC</sub>	-0.3 to +7.0	V
Analog input voltage	VA <sub>N</sub>	-0.3 to AV <sub>CC</sub> + 0.3	V
Operating temperature	T <sub>opr</sub>	Regular specifications: -20 to +75	°C
		Wide-range specifications: -40 to +85	°C
Storage temperature	T <sub>stg</sub>	-55 to +125	°C

**Note:** Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions.

### 20.2 Electrical Characteristics

#### 20.2.1 DC Characteristics

Table 20-2 lists the DC characteristics.

**Table 20-2 DC Characteristics**

Conditions:  $V_{CC} = 5.0V \pm 10\% *1$ ,  $AV_{CC} = 5.0V \pm 10\% *1$ ,  $V_{SS} = AV_{SS} = 0V$ ,  
 $T_a = -20$  to  $+75^\circ C$  (Regular Specifications)  
 $T_a = -40$  to  $+85^\circ C$  (Wide-Range Specifications)

Item		Sym- bol	Min	Typ	Max	Unit	Measurement Conditions
Input High voltage	<u>RES, STBY,</u>	$V_{IH}$	$V_{CC} - 0.7$	-	$V_{CC} + 0.3$	V	
	<u>MD2, MD1, MD0</u>						
	<u>EXTAL</u>						
	<u>Port 8</u>						
	Other input pins (except port 7)		2.2	-	$V_{CC} + 0.3$	V	
Input Low voltage	<u>RES, STBY,</u>	$V_{IL}$	-0.3	-	0.5	V	
	<u>MD2, MD1, MD0</u>						
	Other input pins (except port 7)		-0.3	-	0.8	V	
Schmitt trigger input voltage	Port 7	$V_{T-}$	1.0	-	2.5	V	
		$V_{T+}$	2.0	-	3.5	V	
		$V_{T+} - V_{T-}$	0.4	-	-	V	
Input leakage current	<u>RES</u>	$ I_{in} $	-	-	10.0	$\mu A$	$V_{in} = 0.5$ to
	<u>STBY, NMI,</u>				1.0	$\mu A$	$V_{CC} - 0.5V$
	<u>MD2, MD1, MD0</u> port 8				1.0	$\mu A$	$V_{in} = 0.5$ to $AV_{CC} - 0.5V$
Leakage current in 3-state (off state)	Port 9, ports 7 to 1	$ I_{TSI} $	-	-	1.0	$\mu A$	$V_{in} = 0.5$ to $V_{CC} - 0.5V$
Input pull-up MOS current	Ports 6 and 5	-IP	50	-	200	$\mu A$	$V_{in} = 0V$
Output High Voltage	All output pins	$V_{OH}$	$V_{CC} - 0.5$	-	-	V	$I_{OH} = -200\mu A$
			3.5	-	-	V	$I_{OH} = -1mA$
Output Low Voltage	All output pins	$V_{OL}$	-	-	0.4	V	$I_{OL} = 1.6mA$
	Port 4		-	-	1.0	V	$I_{OL} = 8mA$
			-	-	1.2	V	$I_{OL} = 10mA$
Input capacitance	<u>RES</u>	$C_{in}$	-	-	60	pF	$V_{in} = 0V$
	<u>NMI</u>				30	pF	$f = 1MHz$
	All input pins except <u>RES, NMI</u>				15	pF	$T_a = 25^\circ C$

**Note:** \*1  $AV_{CC}$  must be connected to a power supply line, even when the A/D converter is not used.

**Table 20-2 DC Characteristics (cont)**

Item		Sym- bol	Measurement				
			Min	Typ	Max	Unit Conditions	
Current dissipation*2	Normal operation	I <sub>CC</sub>	–	20	30	mA	f = 6MHz
			–	25	40	mA	f = 8MHz
			–	30	50	mA	f = 10MHz
	Sleep mode		–	12	20	mA	f = 6MHz
			–	16	25	mA	f = 8MHz
			–	20	30	mA	f = 10MHz
	Standby		–	0.01	5.0	μA	T <sub>a</sub> ≤ 50°C
			–	–	20	μA	T <sub>a</sub> > 50°C
Analog supply current	During A/D conversion	I <sub>CC</sub>	–	1.2	2.0	mA	
	While waiting		–	0.01	5.0	μA	
RAM standby voltage		V <sub>RAM</sub>	2.0	–	–	V	

\*2 Current dissipation values assume that V<sub>IH</sub> min = V<sub>CC</sub> – 0.5V, V<sub>IL</sub> max = 0.5V, all output pins are in the no-load state, and all MOS input pull-ups are off.

**Table 20-3 Allowable Output Current Sink Values**

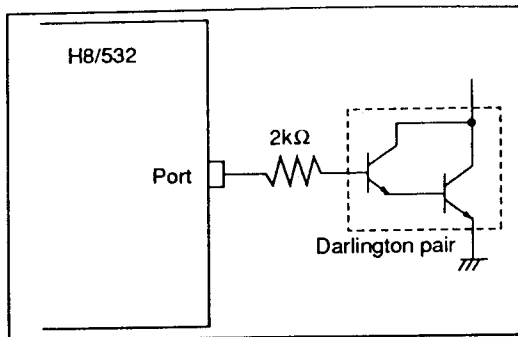
Conditions: V<sub>CC</sub> = 5.0V ±10%, AV<sub>CC</sub> = 5.0V ±10%, V<sub>SS</sub> = AV<sub>SS</sub> = 0V,

T<sub>a</sub> = –20 to +75°C (Regular Specifications)

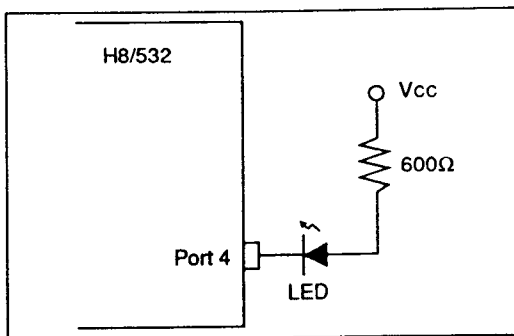
T<sub>a</sub> = –40 to +85°C (Wide-Range Specifications)

Item		Symbol	Min	Typ	Max	Unit
Allowable output Low current sink (per pin)	Port 4	I <sub>OL</sub>	–	–	10	mA
	Other output pins		–	–	2.0	mA
Allowable output Low current sink (total)	Port 4, total of 8 pins	Σ I <sub>OL</sub>	–	–	40	mA
	Total of all other output pins		–	–	80	mA
Allowable output High current sink (per pin)	All output pins	–I <sub>OH</sub>	–	–	2.0	mA
Allowable output High current sink (total)	Total of all output pins	Σ –I <sub>OH</sub>	–	–	25	mA

**Note:** To avoid degrading the reliability of the chip, be careful not to exceed the output current sink values in table 20-3. In particular, when driving a Darlington transistor pair or LED directly, be sure to insert a current-limiting resistor in the output path. See figures 20-1 and 20-2.



**Figure 20-1 Example of Circuit for Driving a Darlington Transistor Pair**



**Figure 20-2 Example of Circuit for Driving an LED**

### 20.2.2 AC Characteristics

The AC characteristics of the H8/532 chip are listed in three tables. Bus timing parameters are given in table 20-4, control signal timing parameters in table 20-5, and timing parameters of the on-chip supporting modules in table 20-6.

**Table 20-4 Bus Timing**

Conditions:  $V_{CC} = 5.0V \pm 10\%$ ,  $AV_{CC} = 5.0V \pm 10\%$ ,  $\phi = 0.5$  to 10MHz,  $V_{SS} = 0V$   
 $T_a = -20$  to  $+75^\circ C$  (Regular Specifications)  
 $T_a = -40$  to  $+85^\circ C$  (Wide-Range Specifications)

Item	Symbol	6MHz		8MHz		10MHz		Unit	Measurement Conditions
		Min	Max	Min	Max	Min	Max		
Clock cycle time	$t_{cy}$	166.7	2000	125	2000	100	2000	ns	See figure 20-4
Clock pulse width Low	$t_{CL}$	65	—	45	—	35	—	ns	
Clock pulse width High	$t_{CH}$	65	—	45	—	35	—	ns	
Clock rise time	$t_{Cr}$	—	15	—	15	—	15	ns	
Clock fall time	$t_{Cf}$	—	15	—	15	—	15	ns	
Address delay time	$t_{AD}$	—	70	—	65	—	65	ns	
Address hold time	$t_{AH}$	30	—	25	—	20	—	ns	
Data strobe delay time 1	$t_{DSD1}$	—	70	—	60	—	40	ns	
Data strobe delay time 2	$t_{DSD2}$	—	70	—	60	—	50	ns	
Data strobe delay time 3	$t_{DSD3}$	—	70	—	60	—	50	ns	
Write data strobe pulse width	$t_{DSWW}$	200	—	150	—	120	—	ns	
Address setup time 1	$t_{AS1}$	25	—	20	—	15	—	ns	

**Table 20-4 Bus Timing (cont)**

Item	Symbol	6MHz		8MHz		10MHz		Unit	Measurement Conditions
		Min	Max	Min	Max	Min	Max		
Address setup time 2	tAS2	105	–	80	–	65	–	ns	See figure 20-4
Read data setup time	tRDS	60	–	50	–	40	–	ns	
Read data hold time	tRDH	0	–	0	–	0	–	ns	
Read data access time	tACC	–	280	–	190	–	160	ns	
Write data delay time	tWDD	–	70	–	65	–	65	ns	
Write data setup time	tWDS	30	–	15	–	10	–	ns	
Write data hold time	tWDH	30	–	25	–	20	–	ns	
Wait setup time	tWTS	40	–	40	–	40	–	ns	See figure 20-5
Wait hold time	tWTH	10	–	10	–	10	–	ns	
Bus request setup time	tBRQS	40	–	40	–	40	–	ns	See figure 20-10
Bus acknowledge delay time 1	tBACD1	–	70	–	60	–	55	ns	
Bus acknowledge delay time 2	tBACD2	–	70	–	60	–	55	ns	
Bus floating delay time	tBZD	–	tBACD1	–	tBACD1	–	tBACD1	ns	
E clock delay time	tED	–	20	–	15	–	15	ns	See figure 20-11
E clock rise time	tEr	–	15	–	15	–	15	ns	
E clock fall time	tEf	–	15	–	15	–	15	ns	
Read data hold time (E clock sync)	tRDHE	0	–	0	–	0	–	ns	See figure 20-6
Write data hold time (E clock sync)	tWDHE	50	–	40	–	30	–	ns	

**Table 20-5 Control Signal Timing**

Conditions:  $V_{CC} = 5.0V \pm 10\%$ ,  $AV_{CC} = 5.0V \pm 10\%$ ,  $\phi = 0.5$  to 10MHz,  $V_{SS} = 0V$   
 $T_a = -20$  to  $+75^\circ C$  (Regular Specifications)  
 $T_a = -40$  to  $+85^\circ C$  (Wide-Range Specifications)

Item	Symbol	6MHz		8MHz		10MHz		Unit	Measurement Conditions
		Min	Max	Min	Max	Min	Max		
RES setup time	tRESS	200	–	200	–	200	–	ns	See figure 20-7
RES pulse width	tRESW	6.0	–	6.0	–	6.0	–	tcyc	
Mode programming setup time	tMDS	4.0	–	4.0	–	4.0	–	tcyc	
NMI setup time	tNMIS	150	–	150	–	150	–	ns	See figure 20-8
NMI hold time	tNMIH	10	–	10	–	10	–	ns	
IRQ <sub>0</sub> setup time	tIRQ0S	50	–	50	–	50	–	ns	
IRQ <sub>1</sub> setup time	tIRQ1S	50	–	50	–	50	–	ns	
IRQ <sub>1</sub> hold time	tIRQ1H	10	–	10	–	10	–	ns	
NMI pulse width (for recovery from software standby mode)	tNMW	200	–	200	–	200	–	ns	See figure 20-9
Crystal oscillator settling time (reset)	tOSC1	20	–	20	–	20	–	ms	See figure 20-12
Crystal oscillator settling time (software standby)	tOSC2	10	–	10	–	10	–	ms	See figure 18-1

**Table 20-6 Timing Conditions of On-Chip Supporting Modules**

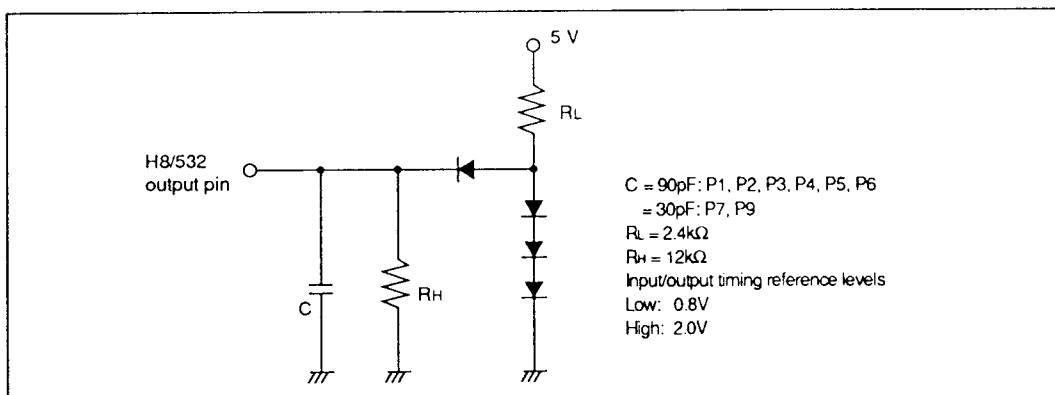
Conditions:  $V_{CC} = 5.0V \pm 10\%$ ,  $AV_{CC} = 5.0V \pm 10\%$ ,  $\phi = 0.5$  to 10MHz,  $V_{SS} = 0V$

$T_a = -20$  to  $+75^\circ C$  (Regular Specifications)

$T_a = -40$  to  $+85^\circ C$  (Wide-Range Specifications)

Item	Symbol	6MHz		8MHz		10MHz		Unit	Measurement Conditions	
		Min	Max	Min	Max	Min	Max			
FRT	Timer output delay time	tF TOD	–	100	–	100	–	100	ns	See figure 20-14
	Timer input setup time	tF TIS	50	–	50	–	50	–	ns	
	Timer clock input setup time	tF TCS	50	–	50	–	50	–	ns	See figure 20-15
	Timer clock pulse width	tF TCWL, tF TCWH	1.5	–	1.5	–	1.5	–	t <sub>cy</sub>	
TMR	Timer output delay time	tT MOD	–	100	–	100	–	100	ns	See figure 20-16
	Timer clock input setup time	tT MCS	50	–	50	–	50	–	ns	See figure 20-17
	Timer clock pulse width	tT MCWL, tT MCWH	1.5	–	1.5	–	1.5	–	t <sub>cy</sub>	
	Timer reset input setup time	tT MRS	50	–	50	–	50	–	ns	See figure 20-18
PWM	Timer output delay time	tP WOD	–	100	–	100	–	100	ns	See figure 20-19
SCI	Input clock cycle	(Async) tS <sub>cy</sub> (Sync)	2	–	2	–	2	–	t <sub>cy</sub>	See figure 20-20
	Input clock pulse width	tS <sub>CKW</sub>	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>S<sub>cy</sub></sub>	
	Transmit data delay time (Sync)	tT XD	–	100	–	100	–	100	ns	See figure 20-21
	Receive data setup time (Sync)	tR XS	100	–	100	–	100	–	ns	
	Receive data hold time (Sync)	tR XH	100	–	100	–	100	–	ns	
	Port	Output data delay time	tP WD	–	100	–	100	–	100	ns
Input data setup time		tP RS	50	–	50	–	50	–	ns	
Input data hold time		tP RH	50	–	50	–	50	–	ns	

• Measurement Conditions for AC Characteristics



**Figure 20-3 Output Load Circuit**

### 20.2.3 A/D Converter Characteristics

Table 20-7 lists the characteristics of the on-chip A/D converter.

**Table 20-7 A/D Converter Characteristics**

Conditions:  $V_{CC} = 5.0V \pm 10\%$ ,  $AV_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,

$T_a = -20$  to  $+75^\circ C$  (Regular Specifications)

$T_a = -40$  to  $+85^\circ C$  (Wide-Range Specifications)

Item	6MHz			8MHz			10MHz			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution	10	10	10	10	10	10	10	10	10	Bits
Conversion time	—	—	23.0	—	—	17.25	—	—	13.8	$\mu s$
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Allowable signal-source impedance	—	—	10	—	—	10	—	—	10	k $\Omega$
Nonlinearity error	—	—	$\pm 2.0$	—	—	$\pm 2.0$	—	—	$\pm 2.0$	LSB
Offset error	—	—	$\pm 2.0$	—	—	$\pm 2.0$	—	—	$\pm 2.0$	LSB
Full-scale error	—	—	$\pm 2.0$	—	—	$\pm 2.0$	—	—	$\pm 2.0$	LSB
Quantizing error	—	—	$\pm 0.5$	—	—	$\pm 0.5$	—	—	$\pm 0.5$	LSB
Absolute accuracy	—	—	$\pm 2.5$	—	—	$\pm 2.5$	—	—	$\pm 2.5$	LSB

## 20.3 MCU Operational Timing

This section provides the following timing charts:

20.3.1 Bus timing	Figures 20-4 to 20-6
20.3.2 Control Signal Timing	Figures 20-7 to 20-10
20.3.3 Clock Timing	Figures 20-11 and 20-12
20.3.4 I/O Port Timing	Figure 20-13
20.3.5 16-Bit Free-Running Timer Timing	Figures 20-14 and 20-15
20.3.6 8-Bit Timer Timing	Figures 20-16 to 20-18
20.3.7 Pulse Width Modulation Timer Timing	Figure 20-19
20.3.8 Serial Communication Interface Timing	Figure 20-20 and 20-21



## 20.3.1 Bus Timing

### 1. Basic Bus Cycle (without Wait States) in Expanded Modes

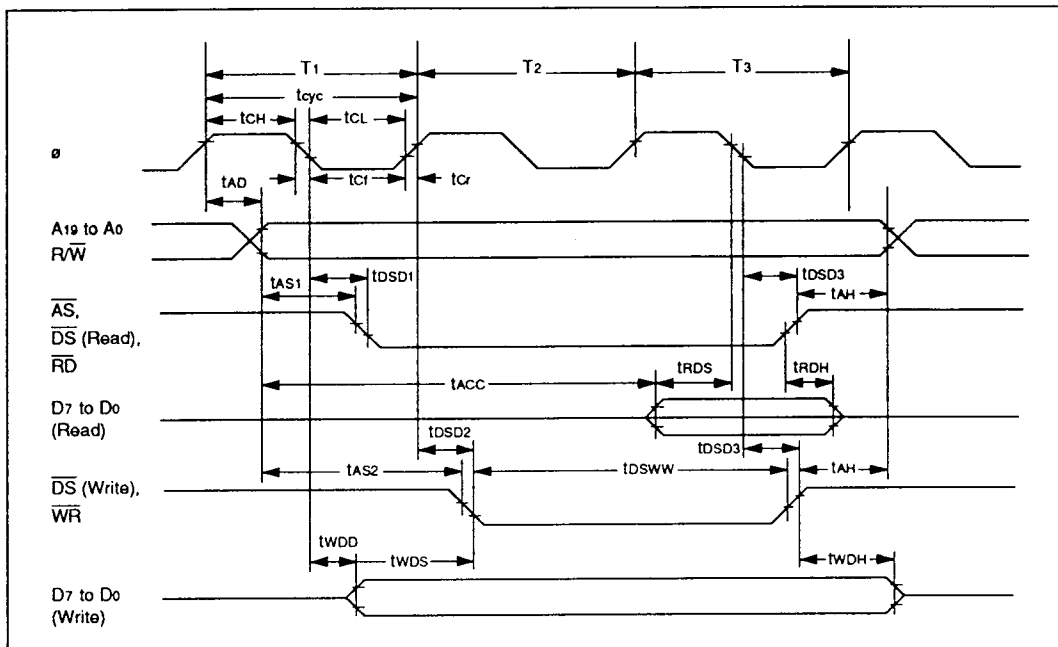


Figure 20-4 Basic Bus Cycle (without Wait States) in Expanded Modes

## 2. Basic Bus Cycle (with 1 Wait State) in Expanded Modes

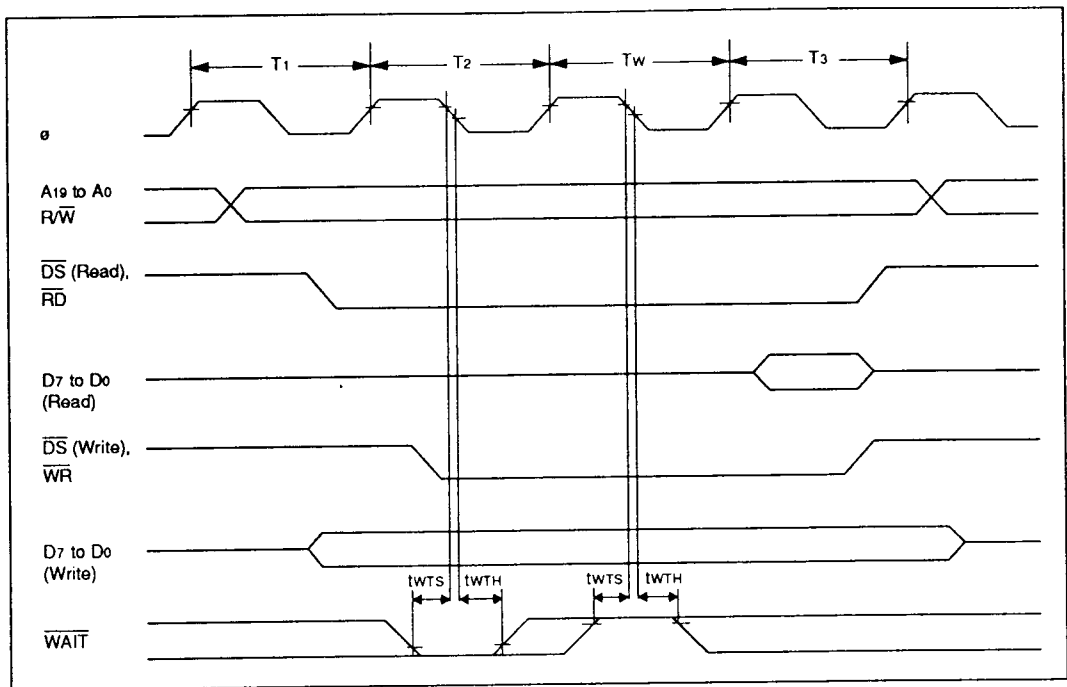


Figure 20-5 Basic Bus Cycle (with 1 Wait State) in Expanded Modes

### 3. Bus Cycle Synchronized with E Clock

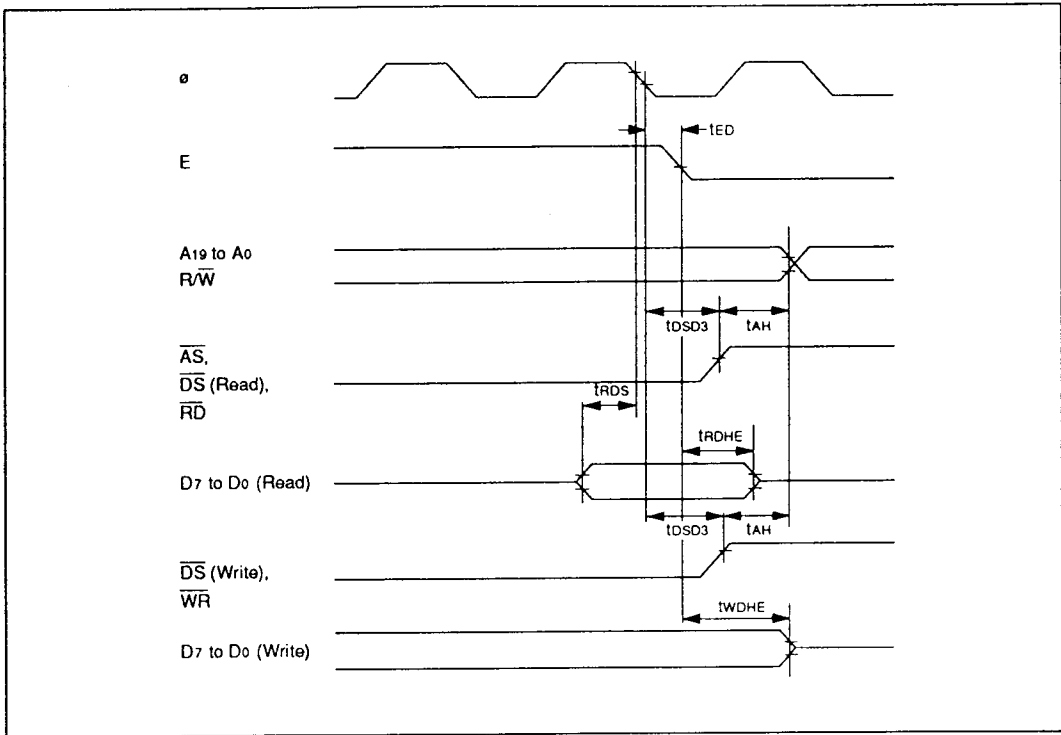


Figure 20-6 Bus Cycle Synchronized with E Clock

## 20.3.2 Control Signal Timing

### 1. Reset Input Timing

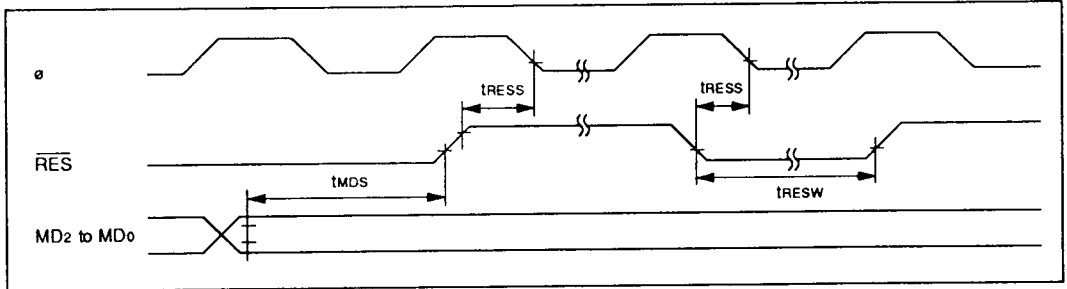


Figure 20-7 Reset Input Timing

### 2. Interrupt Input Timing

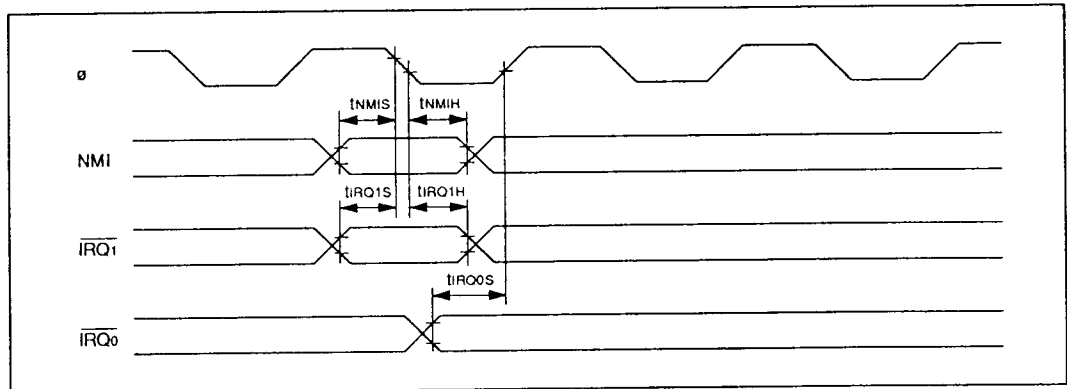


Figure 20-8 Interrupt Input Timing

### 3. NMI Pulse Width

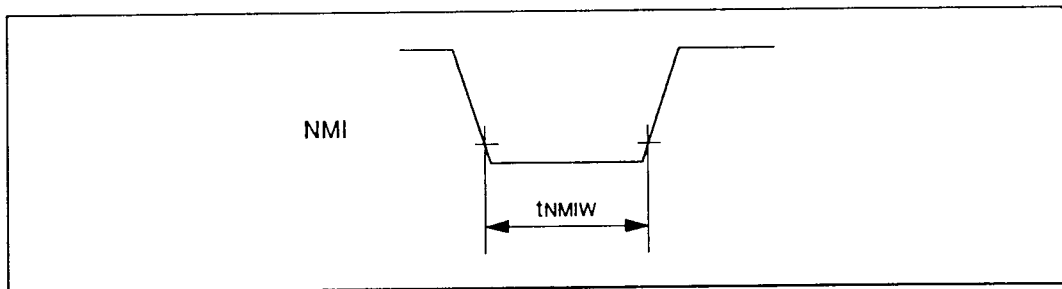


Figure 20-9 NMI Pulse Width (for Recovery from Software Standby Mode)

#### 4. Bus Release State Timing

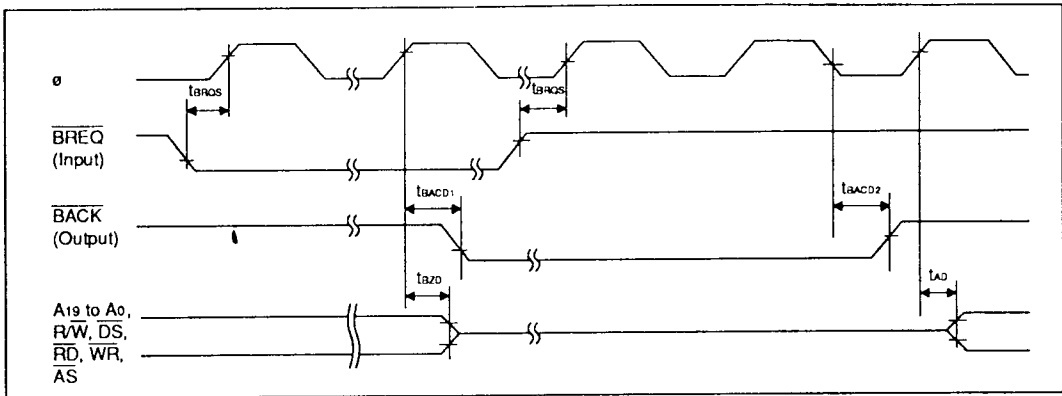


Figure 20-10 Bus Release State Timing

#### 20.3.3 Clock Timing

##### 1. E Clock Timing

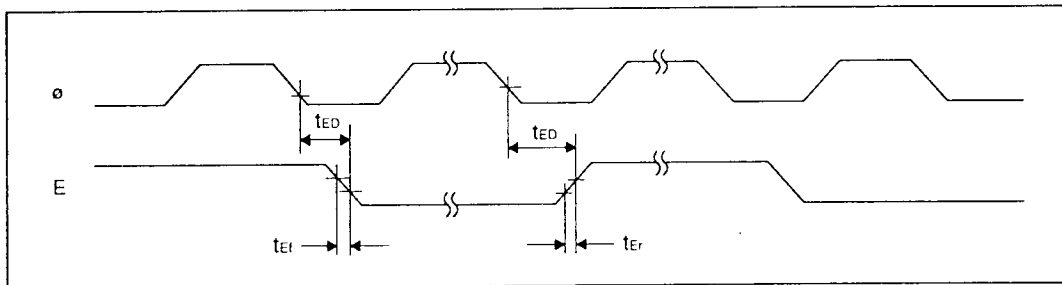


Figure 20-11 E Clock Timing

## 2. Clock Oscillator Stabilization Timing

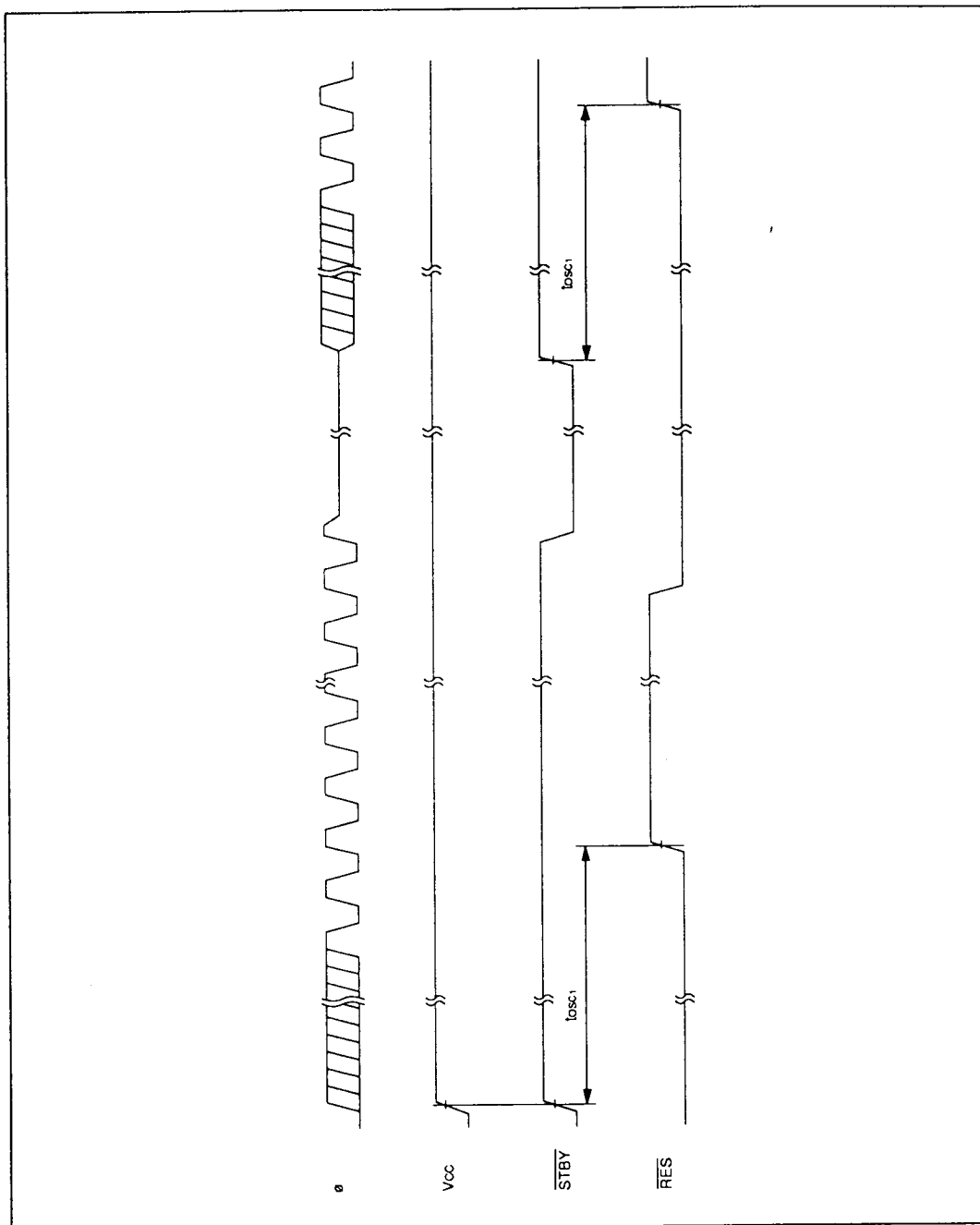


Figure 20-12 Clock Oscillator Stabilization Timing

### 20.3.4 I/O Port Timing

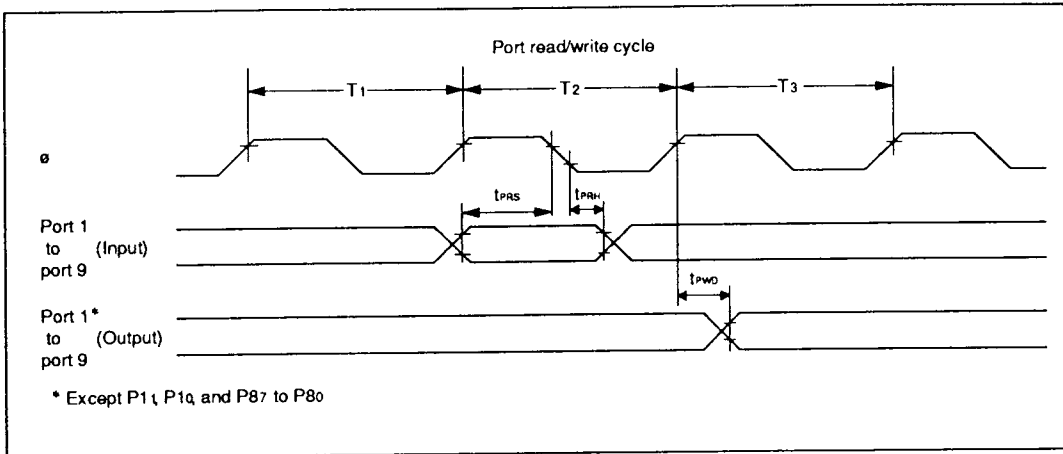


Figure 20-13 I/O Port Input/Output Timing

## 20.3.5 16-Bit Free-Running Timer Timing

### 1. Free-Running Timer Input/Output Timing

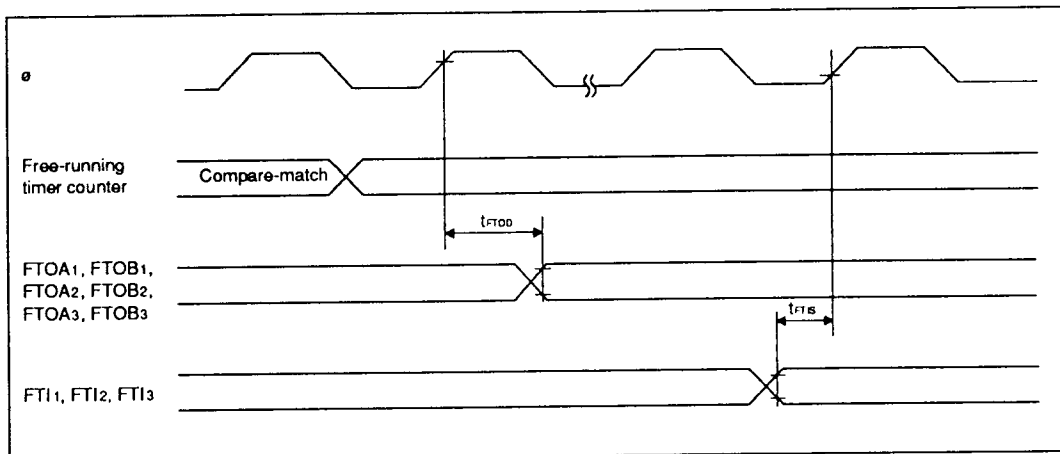


Figure 20-14 Free-Running Timer Input/Output Timing

### 2. External Clock Input Timing for Free-Running Timers

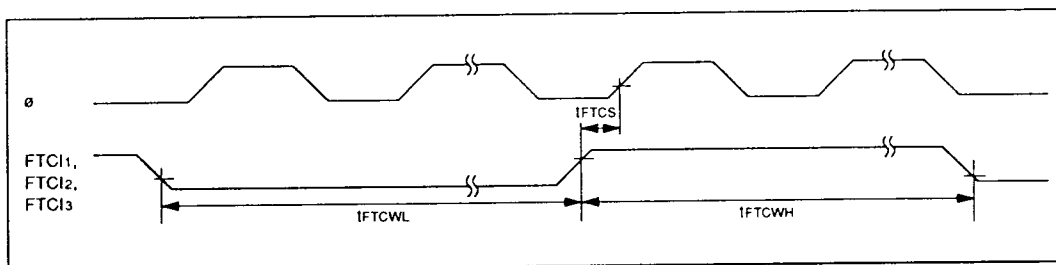


Figure 20-15 External Clock Input Timing for Free-Running Timers



## 20.3.6 8-Bit Timer Timing

### 1. 8-Bit Timer Output Timing

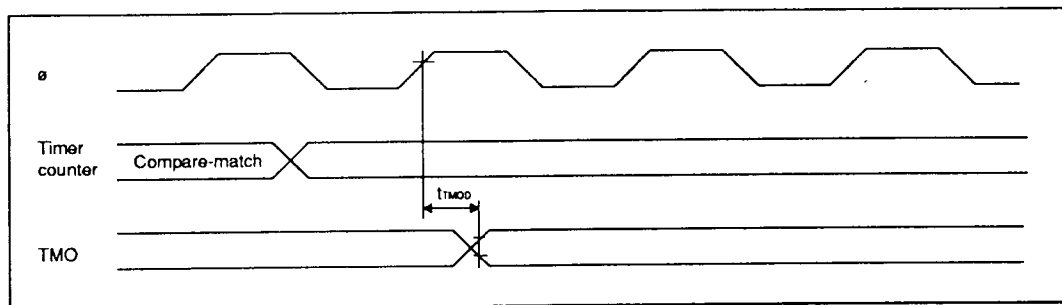


Figure 20-16 8-Bit Timer Output Timing

### 2. 8-Bit Timer Clock Input Timing

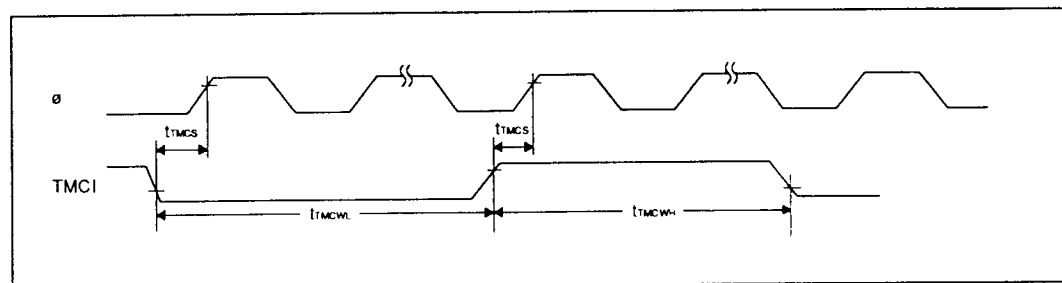


Figure 20-17 8-Bit Timer Clock Input Timing

### 3. 8-Bit Timer Reset Input Timing

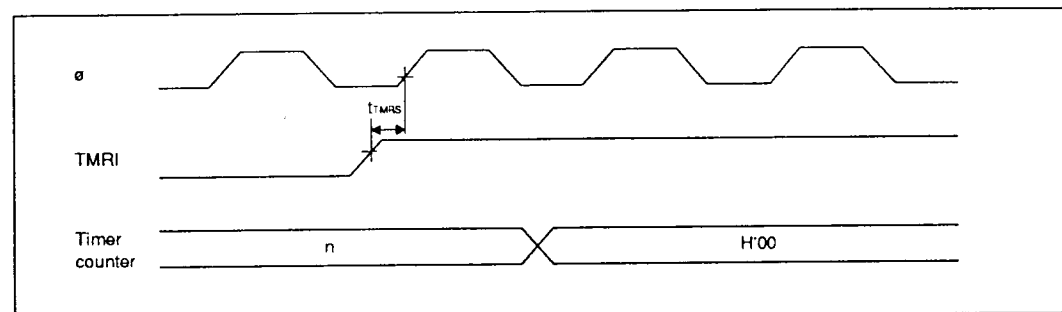


Figure 20-18 8-Bit Timer Reset Input Timing

### 20.3.7 Pulse Width Modulation Timer Timing

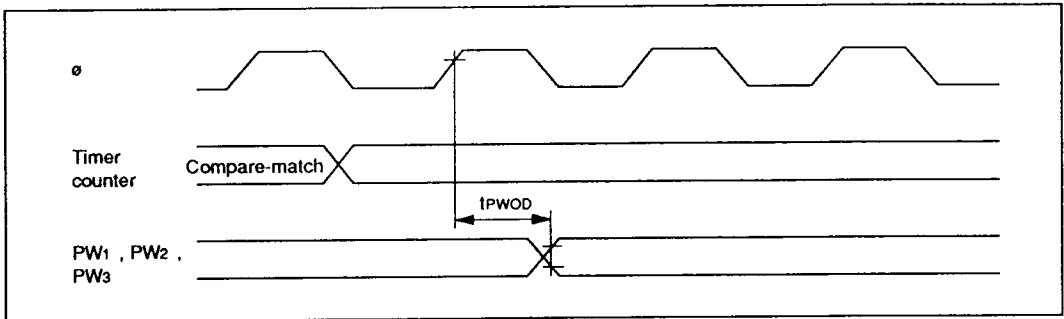


Figure 20-19 PWM Timer Output Timing

### 20.3.8 Serial Communication Interface Timing

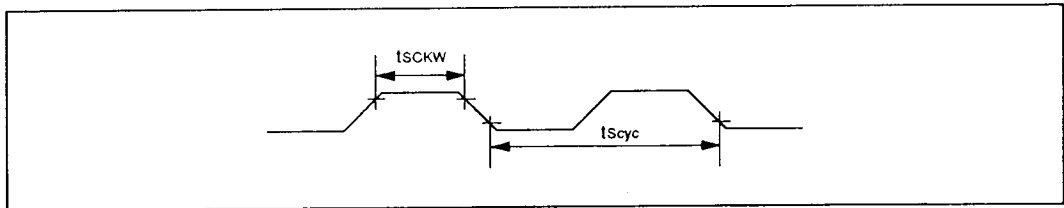


Figure 20-20 SCI Input Clock Timing

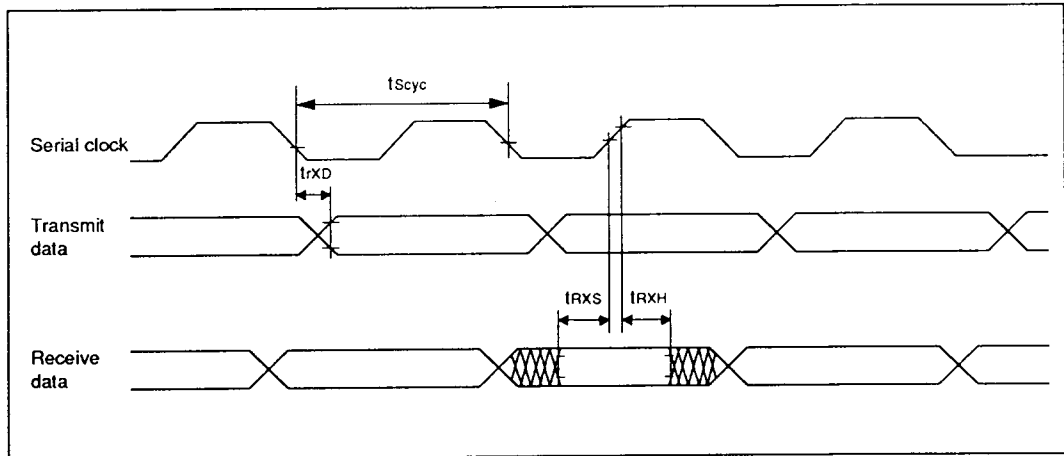


Figure 20-21 SCI Input/Output Timing (Synchronous Mode)