REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add package types Z and U. Add device types 02, 03, and 04. Editorial changes throughout.	92-07-15	

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	A	A	A	A	A	A	A	A											
SHEET	15	16	17	18	19	20	21	22											

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Jeffery Tunstall

CHECKED BY
Tim H. Noh

APPROVED BY
William K. Heckman

DRAWING APPROVAL DATE
91-02-01

REVISION LEVEL A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS 12 X 12 MULTIPLIER/ACCUMULATOR, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-90996
A	67268	

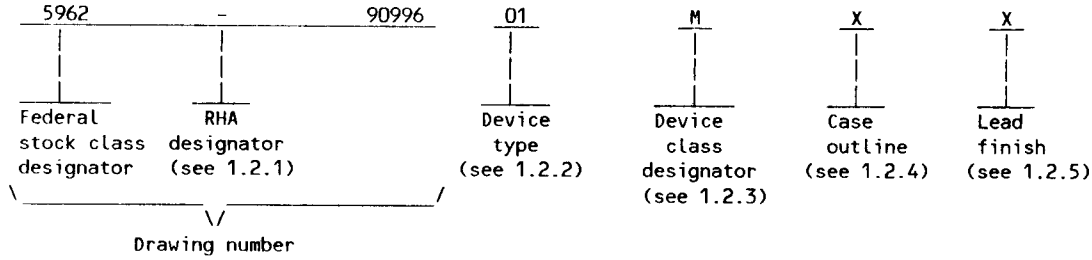
SHEET 1 OF 22

DESC FORM 193

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Multiply time
01	TMC2009	12 x 12 bit CMOS multiplier/accumulator	170 ns
02	LMA1009/2009	12 x 12 bit CMOS multiplier/accumulator	95 ns
03	LMA1009/2009	12 x 12 bit CMOS multiplier/accumulator	65 ns
04	LMA1009/2009	12 x 12 bit CMOS multiplier/accumulator	55 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). For device classes M, B, and S, case outline(s) shall meet the requirements in appendix C of MIL-M-38510 and as listed below. For device classes Q and V, case outline(s) shall meet the requirements of MIL-I-38535, appendix C of MIL-M-38510, and as listed below.

Outline letter	Case outline
X	D-13 (64-lead, 3.240" x .920" x .225"), dual-in-line package
Y	C-7 (68-terminal, .962" x .962" x .120"), square leadless chip carrier package
Z	C-J5 (68-terminal, .960" x .960" x .135"), square grid chip carrier package unformed lead option only
U	P-AC (68-pin, 1.180" x 1.180" x .345"), square pin grid array

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage	-0.5 to +7.0 V
Input voltage	-0.5 to (V_{DD} + 0.5) V
Output:	
Applied voltage 3/	-0.5 to (V_{DD} +0.5) V
Forced current 4/ 5/	-3.0 mA to +6.0 mA
Temperature:	
Operating, case	-60°C to +130°C
Operating, junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	-65°C to +150°C
Maximum power dissipation, unloaded 6/	
Device type 01	330 mW
Device types 02, 03, and 04	138 mW
Thermal resistance, junction-to-case (Θ_{JC}):	
Cases X, Y, Z, U	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	4.5 V ≤ V_{DD} ≤ 5.5 V
Input voltage, logic low (V_{IL})	0.8 V
Input voltage, logic high (V_{IH})	2.0 V
Case temperature (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 7/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is not implied.

3/ Applied voltage must be current limited to specified range, and measured with respect to GND.

4/ Forcing voltage must be limited to specified range.

5/ Current is specified as conventional current flowing into the device.

6/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

7/ Values will be added when they become available.

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block or logic diagram. The block or logic diagram shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.

3.2.6 Input/output data format. The input/output data format shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current, quiescent	I_{DDQ}	V_{DD} = max, V_{IN} = 0 V, TSL, TSM, TSX = 5.0 V	1, 2, 3	01		10	mA
		V_{DD} = max 2/		02, 03, 04		1.0	
Supply current, unloaded	I_{DDU}	V_{DD} = max, freq = 2 MHz, TSL, TSM, TSX = 5.0 V	1, 2, 3	01		17	mA
		V_{DD} = max 3/		02, 03, 04		25	
Supply current, loaded	I_{DDL}	V_{DD} = max, freq = 2 MHz, TSL, TSM, TSX = 0 V Test load: $V_{LOAD} = V_{DD}$ max	1, 2, 3	01		46	mA
Input current, low	I_{IL}	V_{DD} = max, V_I = 0 V	1, 2, 3	01	-10	10	µA
Input current, high	I_{IH}	V_{DD} = max, $V_I = V_{DD}$	1, 2, 3	01	-10	10	µA
Input current	I_{IX}	Ground $\le V_{IN} \le V_{CC}$	1, 2, 3	02, 03 04	-20	20	µA
Output voltage, low	V_{OL}	V_{DD} = min, I_{OL} = 4 mA, V_{IN} = 2.0 V or 0.8 V	1, 2, 3	01		0.4	V
		V_{DD} = min, I_{OL} = 8.0 mA, V_{IN} = 2.0 V or 0.8 V		02, 03, 04		0.5	
Output voltage, high	V_{OH}	V_{DD} = min, I_{OH} = -2 mA, V_{IN} = 2.0 V or 0.8 V	1, 2, 3	01	2.4		V
				02, 03, 04	3.5		
Short circuit output current	I_{OS}	V_{DD} = max V_{OUT} = ground 4/	1, 2, 3	All		-160	mA
Output leakage current, low	I_{OZL}	V_{DD} = max, V_I = 0 V	1, 2, 3	01	-40		µA
Output leakage current, high	I_{OZH}	V_{DD} = max, $V_I = V_{DD}$	1, 2, 3	01		40	µA
Output leakage current	I_{OZ}	Ground $\le V_{OUT} \le V_{CC}$	1, 2, 3	02, 03, 04	-20	20	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input capacitance	C_{IN}	Freq = 1.0 MHz, T_A = +25°C, see 4.4.1b	4	All		15	pF
Output capacitance	C_{OUT}	Freq = 1.0 MHz, T_A = +25°C, see 4.4.1b	4	All		15	pF
Functional test		V_{DD} = 5.0 V, see 4.4.1c	7, 8	All			
Multiply accumulate time 5/	t_{MA}	V_{DD} = min, see figure 5	9, 10, 11	01		170	ns
				02		95	
				03		65	
				04		55	
Output delay 5/	t_D	V_{DD} = min, see figure 5, V_{LOAD} = 2.2 V	9, 10, 11	01		45	ns
				02		35	
				03		30	
				04		25	
Three-state output enable time	t_{ENA}	V_{DD} = min, see figure 5, V_{LOAD} = 1.5 V	9, 10, 11	01		45	ns
				02		35	
				03		35	
				04		30	
Three-state output disable time	t_{DIS}	V_{DD} = min, see figure 5, V_{LOAD} = 0.0 V, 2.6 V	9, 10, 11	01		40	ns
				02		30	
				03		30	
				04		30	
Clock pulse width	t_{PW}	V_{DD} = min, see figure 5	9, 10, 11	01	35		ns
				02	20		
				03	20		
				04	15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input register setup time	t_S	V_{DD} = min, see figure 5	9, 10, 11	01	30		ns
				02	20		
				03	20		
				04	15		
Input register hold time	t_H	V_{DD} = min, see figure 5	9, 10, 11	01	03		ns
				02	02		
				03	02		
				04	02		
Preload setup time	t_{SP}	V_{DD} = min, see figure 5	9, 10, 11	01	30		ns
				02	20		
				03	20		
				04	15		
Preload hold time	t_{HP}	V_{DD} = min, see figure 5	9, 10, 11	01	03		ns
				02	02		
				03	02		
				04	02		

1/ All test to be performed using worst-case conditions unless otherwise specified.

2/ Tested with all inputs within 0.1 V of V_{CC} or ground, no load.

3/ Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

4/ Duration of the output short circuit should not exceed 30 seconds. This parameter is guaranteed but not tested.

5/ The transitions are measured at 1.5 V level. Inputs are driven at V_{IL} = 0 V and V_{IH} = 3 V during testing.

All device types

Case outline U

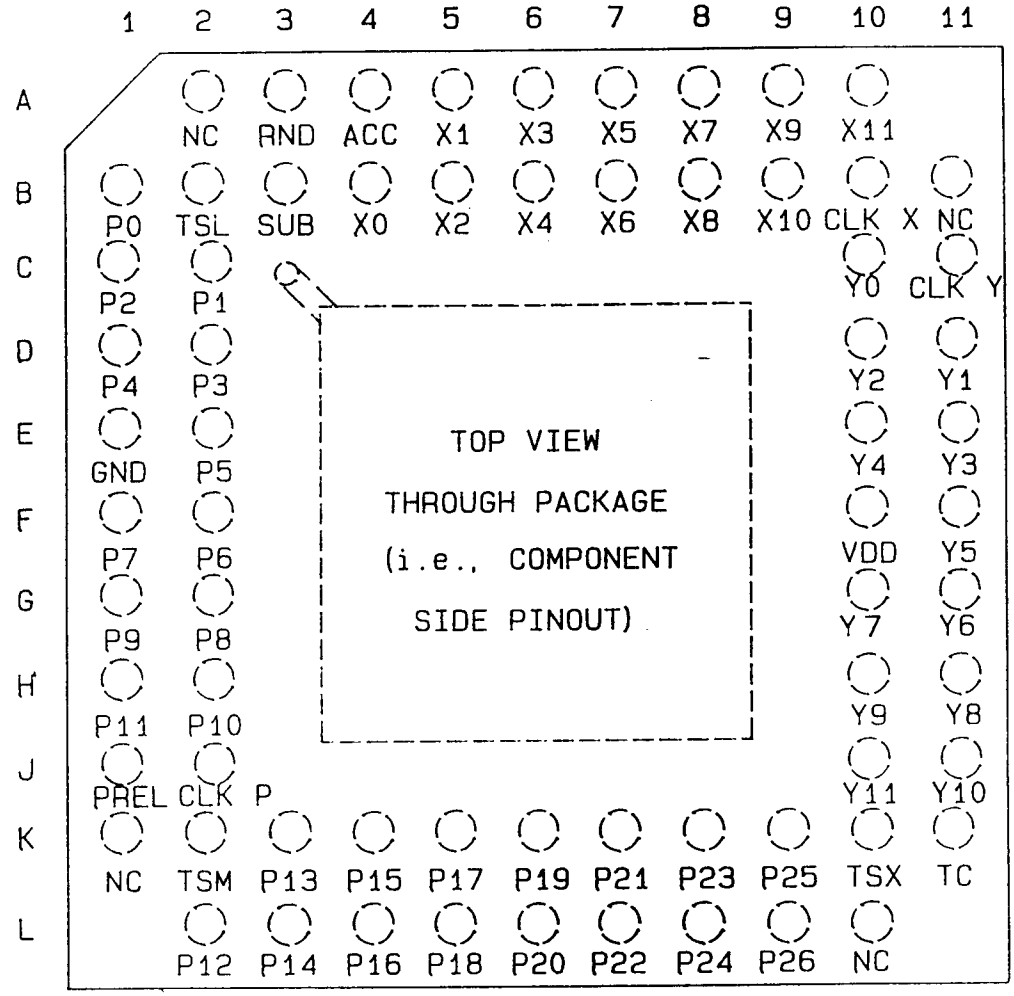


FIGURE 1. Terminal connections.

Device type 01

Case outline Z

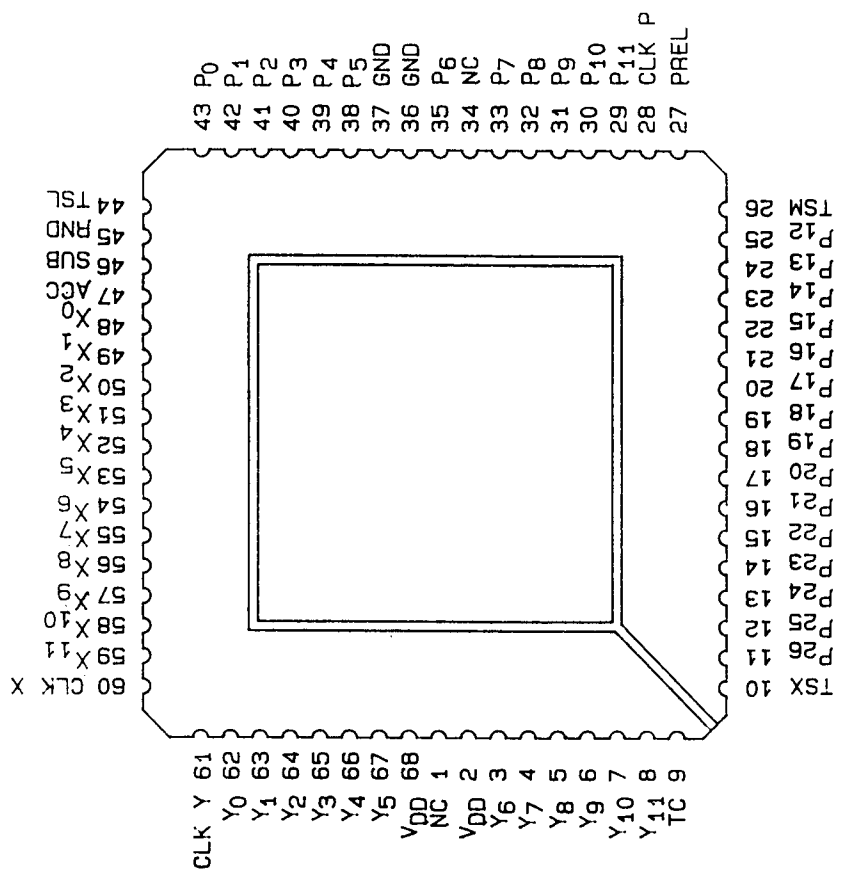
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	nc	35	P_6
2	V_{DD}	36	GND
3	Y_6	37	GND
4	Y_7	38	P_5
5	Y_8	39	P_4
6	Y_9	40	P_3
7	Y_{10}	41	P_2
8	Y_{11}	42	P_1
9	TC	43	P_0
10	TSX	44	TSL
11	P_{26}	45	RND
12	P_{25}	46	SUB
13	P_{24}	47	ACC
14	P_{23}	48	X_0
15	P_{22}	49	X_1
16	P_{21}	50	X_2
17	P_{20}	51	X_3
18	P_{19}	52	X_4
19	P_{18}	53	X_5
20	P_{17}	54	X_6
21	P_{16}	55	X_7
22	P_{15}	56	X_8
23	P_{14}	57	X_9
24	P_{13}	58	X_{10}
25	P_{12}	59	X_{11}
26	TSM	60	CLK X
27	PREL	61	CLK Y
28	CLK P	62	Y_0
29	P_{11}	63	Y_1
30	P_{10}	64	Y_2
31	P_9	65	Y_3
32	P_8	66	Y_4
33	P_7	67	Y_5
34	nc	68	V_{DD}

FIGURE 1. Terminal connections - Continued.

All device types

Case outline Y

CASE OUTLINE Y



Case outline X

CASE OUTLINE X

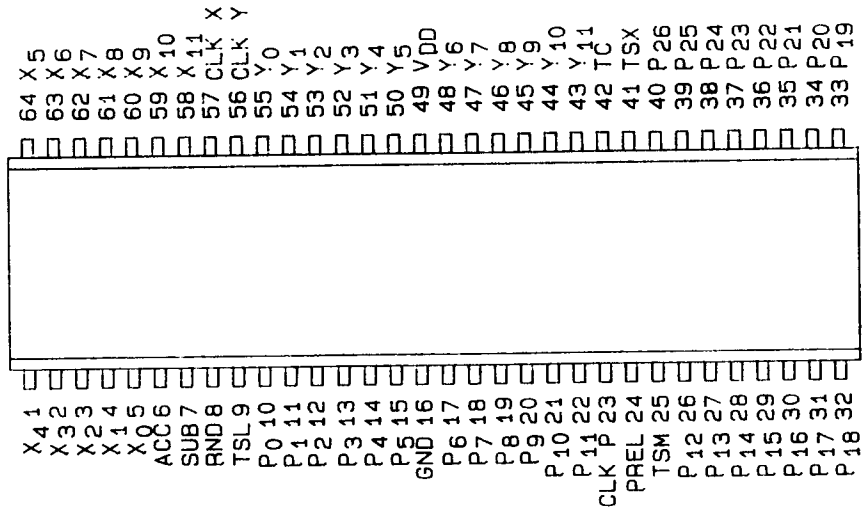


FIGURE 1. Terminal connections - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90996
		REVISION LEVEL A	SHEET 11

Preload truth table

PREL (see note 1)	TSX (see note 1)	TSM (see note 1)	TSL (see note 1)	XTP	MSP	LSP
L	L	L	L	Register——>Output pin	Register——>Output pin	Register——>Output pin
L	L	L	H	Register——>Output pin	Register——>Output pin	Hi-Z
L	L	H	L	Register——>Output pin	Hi-Z	Register——>Output pin
L	L	H	H	Register——>Output pin	Hi-Z	Hi-Z
L	H	L	L	Hi-Z	Register——>Output pin	Register——>Output pin
L	H	L	H	Hi-Z	Register——>Output pin	Hi-Z
L	H	H	L	Hi-Z	Hi-Z	Register——>Output pin
L	H	H	H	Hi-Z	Hi-Z	Hi-Z
H[2]	L	L	L	Hi-Z	Hi-Z	Hi-Z
H[2]	L	L	H	Hi-Z	Hi-Z	Hi-Z preload
H[2]	L	H	L	Hi-Z	Hi-Z preload	Hi-Z
H[2]	L	H	H	Hi-Z	Hi-Z preload	Hi-Z preload
H[2]	H	L	L	Hi-Z preload	Hi-Z	Hi-Z
H[2]	H	L	H	Hi-Z preload	Hi-Z	Hi-Z preload
H[2]	H	H	L	Hi-Z preload	Hi-Z preload	Hi-Z
H[2]	H	H	H	Hi-Z preload	Hi-Z preload	Hi-Z preload

NOTES:
1. PREL, TSX, TSM, and TSL are not required.
2. PREL high inhibits any change of output register for those outputs in which the three-state control is low.

FIGURE 2. Truth table.

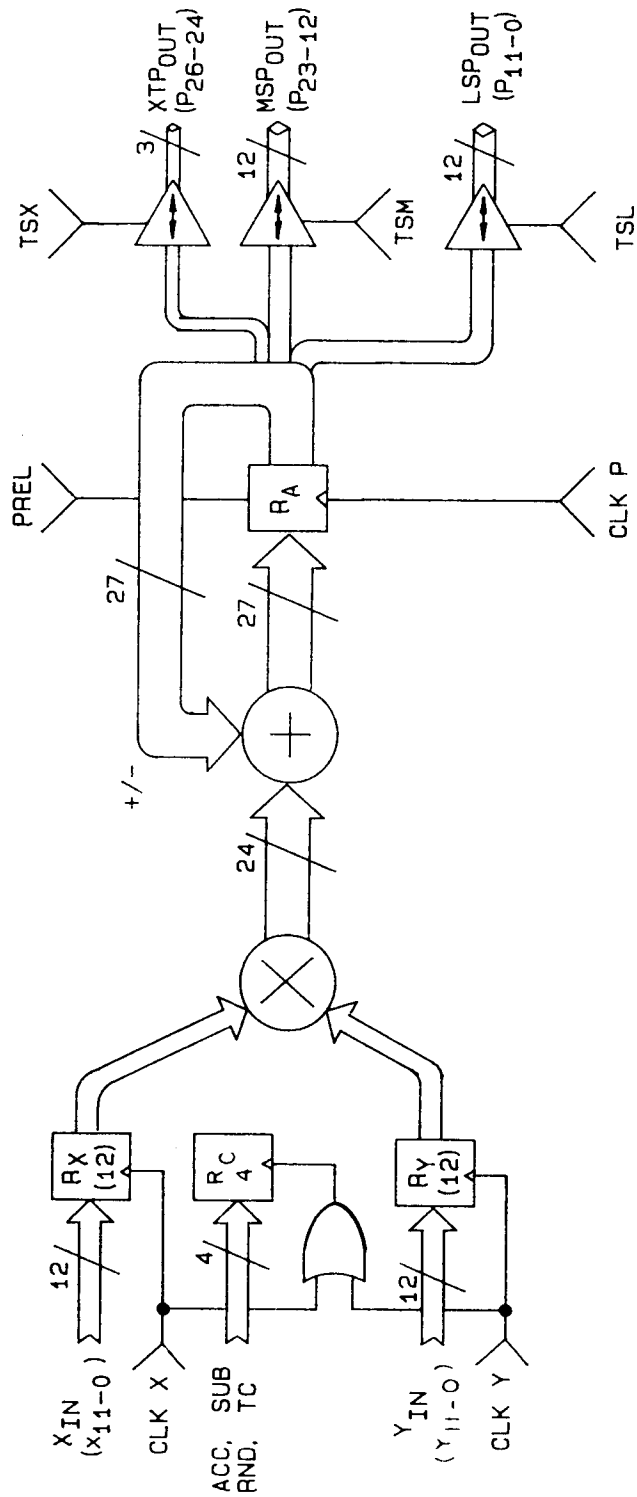
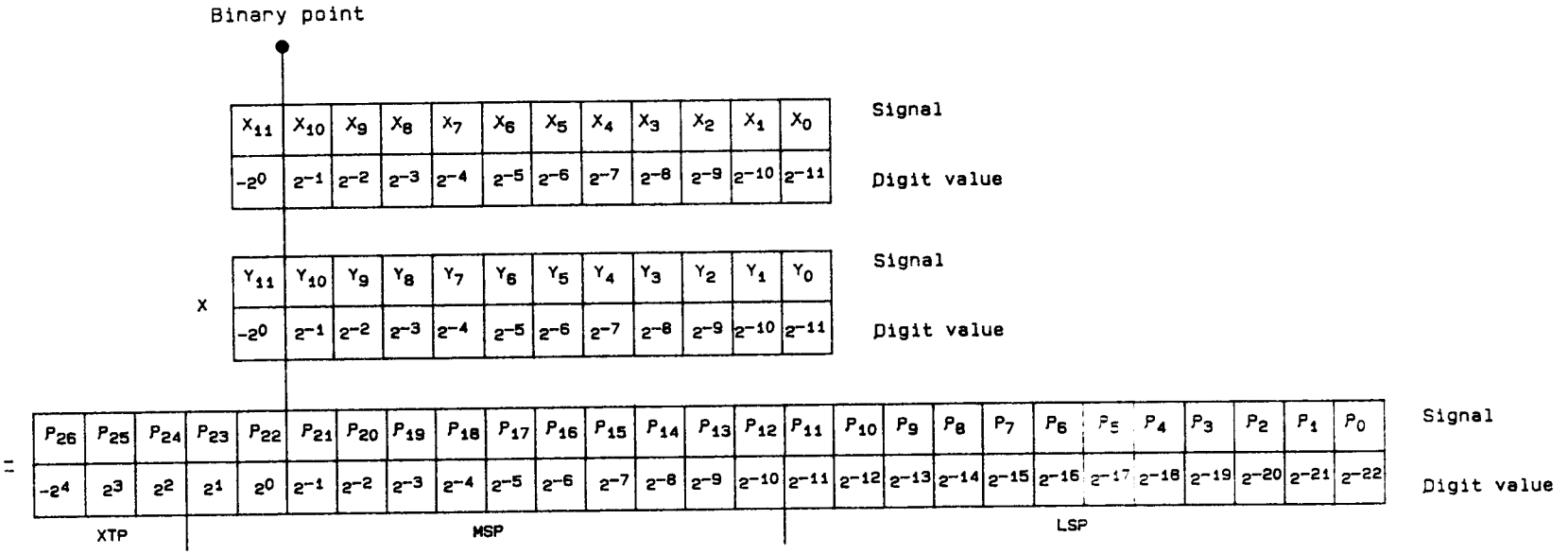


FIGURE 3. Block diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90996
		REVISION LEVEL A	SHEET 13

Fractional two's complement notation



Fractional unsigned magnitude notation

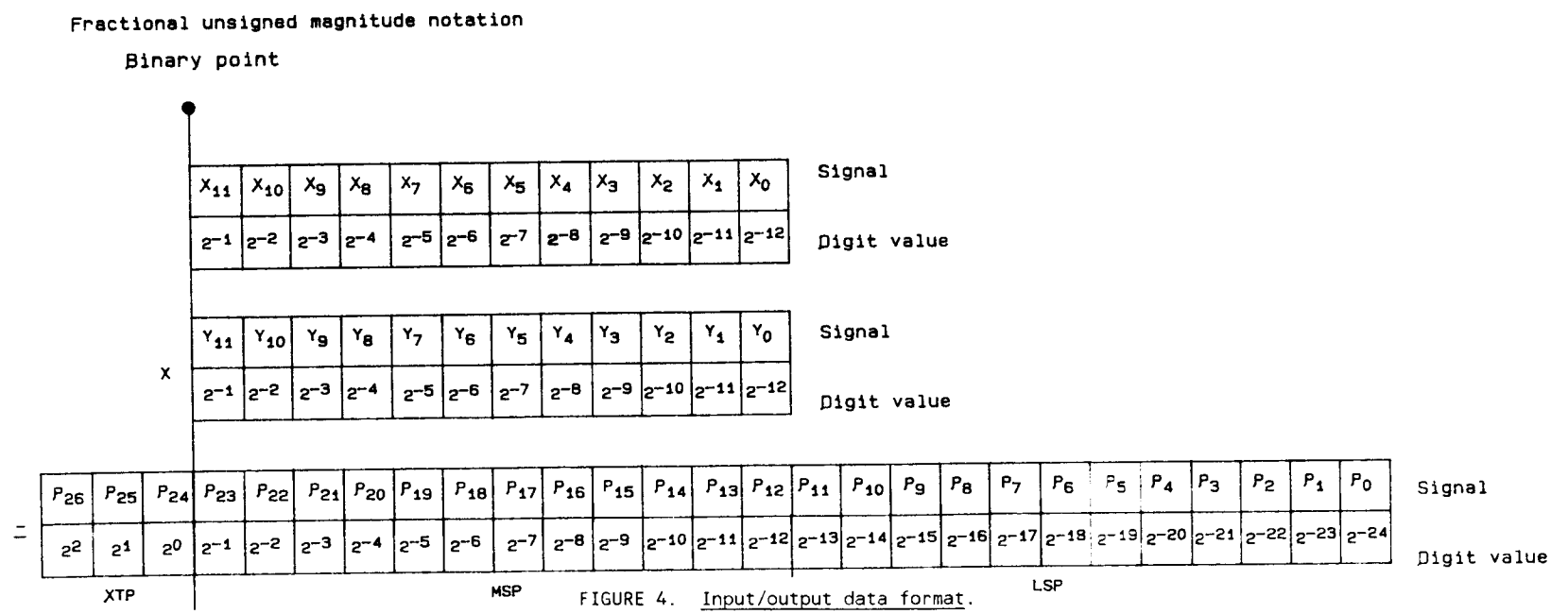


FIGURE 4. Input/output data format.

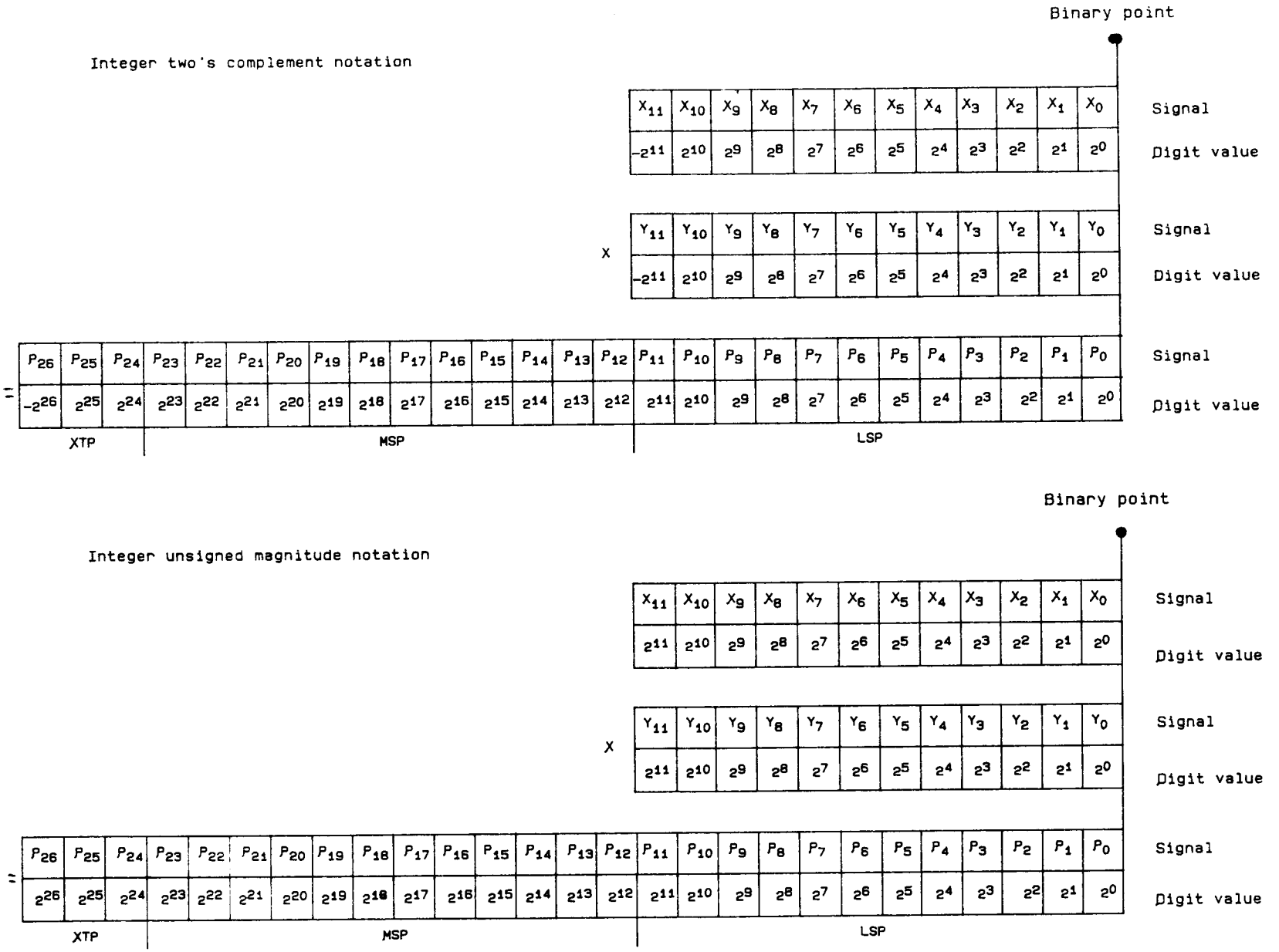


FIGURE 4. Input/output data format - Continued.

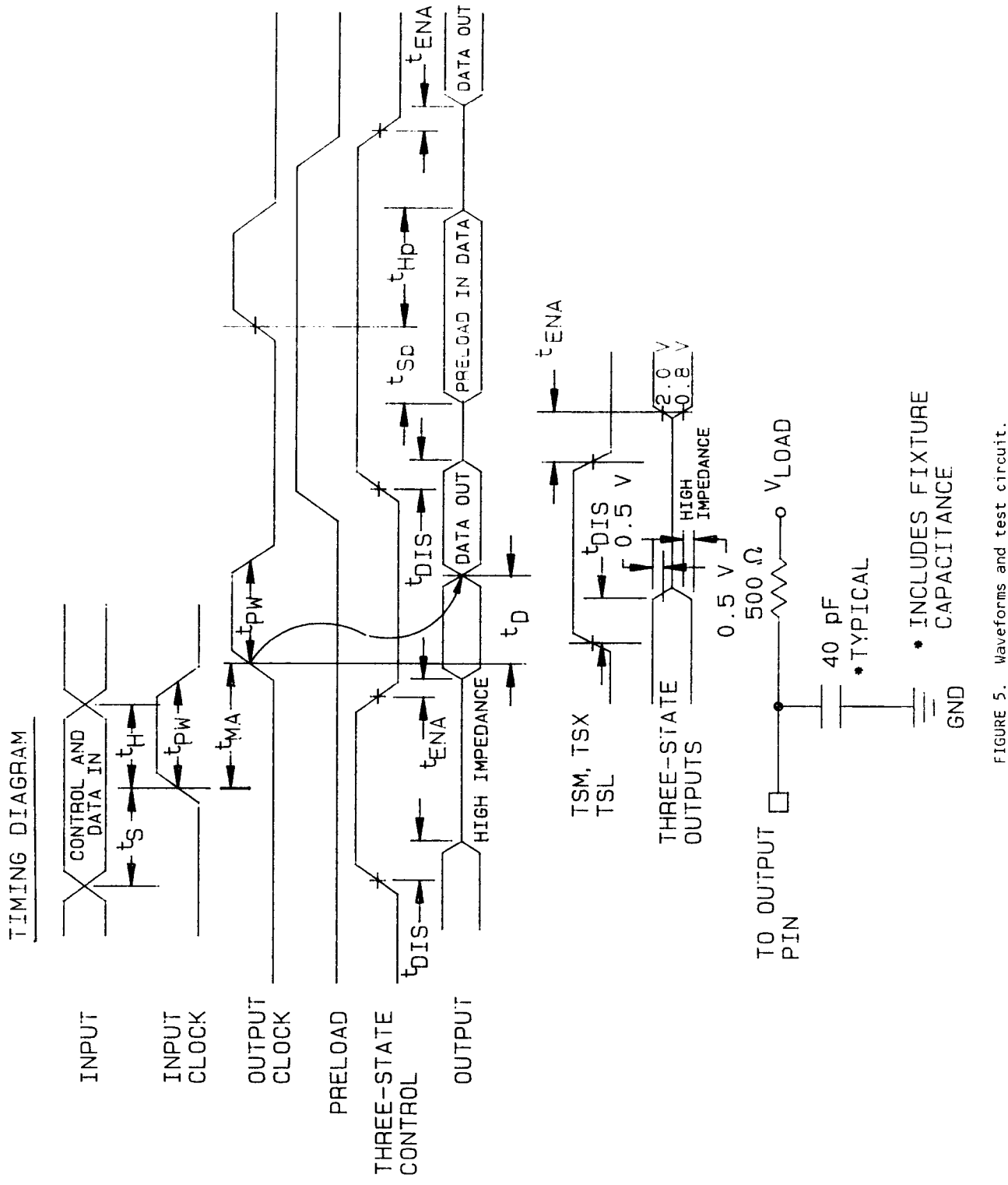


FIGURE 5. Waveforms and test circuit.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

c. Subgroups 7 and 8 shall verify the functionality of the device. These tests form a part of the manufacturer's test tape and shall be maintained and available from the approved source of supply.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)			1,7,9		1,7,9
Final electrical parameters (see 4.2)	1/ 1-3,7-11	1/ 1-3,7-11	2/ 1-3,7-11	1/ 1-3,7-11	2/ 1-3,7-11
Group A test requirements (see 4.4)	1-4,7-11	1-4,7-11	1-4,7-11	1-4,7-11	1-4,7-11
Group B end-point electrical parameters (see 4.4)			1,7,9		1,7,9
Group C end-point electrical parameters (see 4.4)	1,2,7,9	1,2,7,9		1,2,7,9	
Group D end-point electrical parameters (see 4.4)	1,2,7,9	1,2,7,9	1,2,7,9	1,2,7,9	1,2,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hours at +125°C	100%
Radiographic	2012	100%

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IIA herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein.

d. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes M, B, and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.4 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8526.

6.5 Symbols, definitions, and functional descriptions. See table III.

TABLE III. Pin functions.

Pin	Description
V_{DD}, GND	The device operates from a single +5 V supply. All power and ground lines must be connected.
X_{11-0}	The 12-bit two's complement or unsigned magnitude X data input. X_{11} is the MSB and contains the sign information for two's complement notation. The data on the X input is clocked into the input register on the rising edge of CLK X.
Y_{11-0}	The 12-bit two's complement or unsigned magnitude Y data input. Y_{11} is the MSB and contains the sign information for two's complement notation. The data on the Y input is clocked into the input register on the rising edge of CLK Y.
PREL	PRELoad is the active-high control used to directly load the output register (see figure 2). When PREL is high, all output buffers are forced into the high-impedance state. Second, when any or all the TSX, TSM, and TSL controls are also high, external data present at the output pins will be preloaded into the corresponding section of the output register on the rising edge of the CLK P. Normal data setup and hold times apply both to the logical AND of PREL and the relevant three-state control (TSX,TSM,TSL), and to the data being preloaded.
P_{26-0}	P_{26-0} is the accumulated product result for the device. The 27-bit output is either the two's complement or unsigned magnitude result of the accumulated products. The output is divided into two 12-bit output words (MSB,LSB) and one 3-bit output word (XTP). P26 is the MSB and contains the sign information for two's complement notation. Formats for two's complement, fractional unsigned magnitude, integer two's complement and integer unsigned notation are show on figure 5.
TC	The Two's Complement input is used to control how the device interprets the data on the X and Y inputs. TC high makes both inputs two's complement, while TC low makes both inputs unsigned magnitude numbers.
ACC	When ACCumulate is high, the content of the output register is added or subtracted from the next product generated, and their sum stored back into the output register on the next rising edge of CLK P. When ACC is low, multiplication without accumulation is performed, and the next product generated is stored into the output registers directly. This operation is used for the first term in a summation to avoid a separate "clear" operation.
SUB	SUBtract is used in conjunction with the ACC control. When both the ACC and SUB control are high, the content of the output register is subtracted from the next product generated and the difference is stored back into the output register. Note that the previous output is subtracted from the product, not the product from the previous output.
RND	The RouND input is used to control the rounding of results. When RND is high, a 1 is added to the (MSB) of the LSP for rounding the product in the MSP and XTP rather than truncating it. This control is used to improve the accuracy when the LSP will not be used.

TABLE III. Pin functions - Continued.

Pin	Description
CLK X, CLK Y	The rising edge of CLK X (CLK Y) loads the data lines into the appropriate input register. The RouND (RND), Two's Complement (TC), ACCumulate (ACC), and SUBtract (SUB) control inputs are registered and loaded on the logical OR of both CLK X and CLK Y. Special attention to clock signals is required if normally high clock signals are used. problems can be avoided by the use of normally low clocks.
CLK P	CLK P is used to clock the accumulated product sum into the output register. If ACC is high, the content of the output register is added to the next product generated and loaded into the output register. CLK P is also used to preload the output register from the output pins (see figure 4).
TSX,TSM,TSL	TSX is the three-state control for the 3-bit XTP output drivers. TSM and TSL are the three-state controls for the MSP and LSP outputs respectively. The outputs are in the high-impedance state when the control is high, and enabled when the control is low.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.