

TLP2200

- Isolated Buss Driver
- High Speed Line Receiver
- Microprocessor System Interfaces
- MOS FET Gate Driver
- Direct Replacement For HCPL-2200

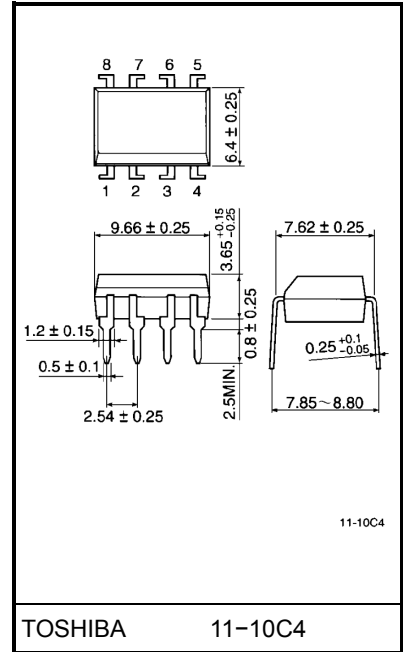
The TOSHIBA TLP2200 consists of a GaAsIred light emitting diode and integrated high gain, high speed photodetector. This unit is 8-lead DIP package. The detector has a three state output stage that eliminates the need for pull-up resistor, and built-in schmitt trigger. The detector IC has an internal shield that provides a guaranteed common mode transient immunity of 1000V / μ s.

- Input current: $I_F = 1.6\text{mA}$
- Power supply voltage: $V_{CC} = 4.5\sim 20\text{V}$
- Switching speed: 2.5MBd guaranteed
- Common mode transient immunity: $\pm 1000\text{V} / \mu\text{s}$ (min.)
- Guaranteed performance over temp: $0\sim 85^\circ\text{C}$
- Isolation voltage: 2500Vrms(min.)
- UL recognized: UL1577, file No. E67349

Truth Table (positive logic)

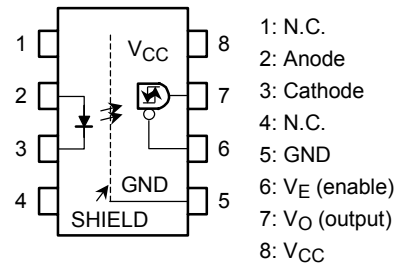
Input	Enable	Output
H	H	Z
L	H	Z
H	L	H
L	L	L

Unit in mm

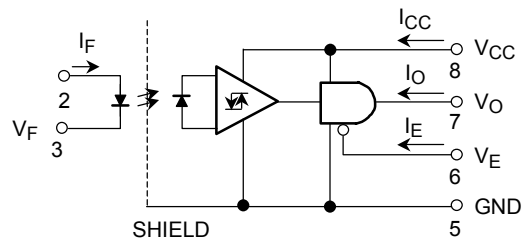


Weight: 0.54 g

Pin Configuration (top view)



Schematic



Recommended Operating Conditions

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input current, on	$I_{F(ON)}$	1.6	—	5	mA
Input current, off	$I_{F(OFF)}$	0	—	0.1	mA
Supply voltage	V_{CC}	4.5	—	20	V
Enable voltage high	V_{EH}	2.0	—	20	V
Enable voltage low	V_{EL}	0	—	0.8	V
Fan out (TTL load)	N	—	—	4	—
Operating temperature	T_{opr}	0	—	85	°C

Absolute Maximum Ratings (no derating required up to 70°C)

Characteristic	Symbol	Rating	Unit
Forward current	I_F	10	mA
Peak transient forward current (Note 1)	I_{FPT}	1	A
Reverse voltage	V_R	5	V
Output current	I_O	25	mA
Supply voltage	V_{CC}	-0.5~20	V
Output voltage	V_O	-0.5~20	V
Three state enable voltage	V_E	-0.5~20	V
Total package power dissipation (Note 2)	P_T	210	mW
Operating temperature range	T_{opr}	-40~85	°C
Storage temperature range	T_{stg}	-55~125	°C
Lead solder temperature (10s) (**)	T_{sol}	260	°C
Isolation voltage (AC 1min., R.H. ≤ 60%, $T_a = 25^\circ\text{C}$) (Note 3)	BV_S	2500	Vrms

(Note 1) Pulse width 1μs 300pps.

(Note 2) Derate 4.5mW / °C above 70°C ambient temperature.

(Note 3) Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5,6,7 and 8 shorted together

(**) 1.6mm below seating plane.

Electrical Characteristics (unless otherwise specified, Ta = 0~85°C, V_{CC} = 4.5~20V, I_{F(ON)} = 1.6~5mA, I_{F(OFF)} = 0~0.1mA, V_{EL} = 0~0.8V, V_{EH} = 2.0~20V)

Characteristic	Symbol	Test Condition		Min.	Typ.*	Max.	Unit
Output leakage current (V _O > V _{CC})	I _{OHH}	I _F = 5mA, V _{CC} = 4.5V	V _O = 5.5V	—	—	100	μA
			V _O = 20V	—	2	500	
Logic low output voltage	V _{OL}	I _{OL} = 6.4mA (4 TTL load)		—	0.32	0.5	V
Logic high output voltage	V _{OH}	I _{OH} = -2.6mA		2.4	3.4	—	V
Logic low enable current	I _{EL}	V _E = 0.4V		—	-0.13	-0.32	mA
Logic high enable current	I _{EH}	V _E = 2.7V		—	—	20	μA
		V _E = 5.5V		—	—	100	
		V _E = 20V		—	0.01	250	
Logic low enable voltage	V _{EL}	—		—	—	0.8	V
Logic high enable voltage	V _{EH}	—		2.0	—	—	V
Logic low supply current	I _{CCL}	I _F = 0mA, V _E = don't care	V _{CC} = 5.5V	—	5	6.0	mA
			V _{CC} = 20V	—	5.6	7.5	
Logic high supply current	I _{CCH}	I _F = 5mA, V _E = don't care	V _{CC} = 5.5V	—	2.5	4.5	mA
			V _{CC} = 20V	—	2.8	6.0	
High impedance state output current	I _{OZL}	I _F = 5mA, V _E = 2V	V _O = 0.4V	—	1	-20	μA
			V _O = 2.4V	—	—	20	
	I _{OZH}	I _F = 0mA, V _E = 2V	V _O = 5.5V	—	—	100	
			V _O = 20V	—	0.01	500	
Logic low short circuit output current (Note 4)	I _{OSL}	I _F = 0mA	V _O = V _{CC} = 5.5V	25	55	—	mA
			V _O = V _{CC} = 20V	40	80	—	
Logic high short circuit output current (Note 4)	I _{OSH}	I _F = 5mA, V _O = GND	V _{CC} = 5.5V	-10	-25	—	mA
			V _{CC} = 20V	-25	-60	—	
Input current hysteresis	I _{HYS}	V _{CC} = 5V		—	0.05	—	mA
Input forward voltage	V _F	I _F = 5mA, Ta = 25°C		—	1.55	1.7	V
Temperature coefficient of forward voltage	ΔV _F / ΔTa	I _F = 5mA		—	-2.0	—	mV / °C
Input reverse breakdown voltage	BV _R	I _R = 10μA, Ta = 25°C		5	—	—	V
Input capacitance	C _{IN}	V _F = 0V, f = 1MHz, Ta = 25°C		—	45	—	pF
Resistance (input-output)	R _{I-O}	V _{I-O} = 500V R.H. ≤ 60% (Note 3)		5 × 10 ¹⁰	10 ¹⁴	—	Ω
Capacitance (input-output)	C _{I-O}	V _{I-O} = 0V, f = 1MHz (Note 3)		—	0.6	—	pF

(**) All typ. values are at Ta = 25°C, V_{CC} = 5V, I_{F(ON)} = 3mA unless otherwise specified.

Switching Characteristics

(unless otherwise specified, $T_a = 0\sim 85^\circ\text{C}$, $V_{CC} = 4.5\sim 20\text{V}$, $I_{F(\text{ON})} = 1.6\sim 5\text{mA}$, $I_{F(\text{OFF})} = 0\sim 0.1\text{mA}$)

Characteristic	Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time to logic high output level (Note 5)	t_{pLH}	1	Without peaking capacitor C_1	—	235	—	ns
			With peaking capacitor C_1	—	—	400	
Propagation delay time to logic low output level (Note 5)	t_{pHL}		Without peaking capacitor C_1	—	250	—	ns
			With peaking capacitor C_1	—	—	400	
Output rise time (10–90%)	t_r			—	35	—	ns
Output fall time (90–10%)	t_f			—	20	—	ns
Output enable time to logic high	t_{pZH}		2	—	—	—	ns
Output enable time to logic low	t_{pZL}			—	—	—	ns
Output disable time from logic high	t_{pHZ}	—		—	—	ns	
Output disable time from logic low	t_{pLZ}	—		—	—	ns	
Common mode transient immunity at logic high output (Note 6)	CM_H	3	$I_F = 1.6\text{mA}$, $V_{CM} = 50\text{V}$, $T_a = 25^\circ\text{C}$	-1000	—	—	$\text{V} / \mu\text{s}$
Common mode transient immunity at logic low output (Note 6)	CM_L		$I_F = 0\text{mA}$, $V_{CM} = 50\text{V}$, $T_a = 25^\circ\text{C}$	1000	—	—	$\text{V} / \mu\text{s}$

(*) All typ. values are at $T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $I_{F(\text{ON})} = 3\text{mA}$ unless otherwise specified.

(Note 4) Duration of output short circuit time should not exceed 10ms.

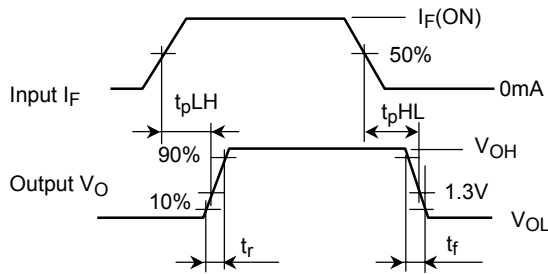
(Note 5) The t_{pLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3V point on the leading edge of the output pulse.

The t_{pHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3V point on the trailing edge of the output pulse.

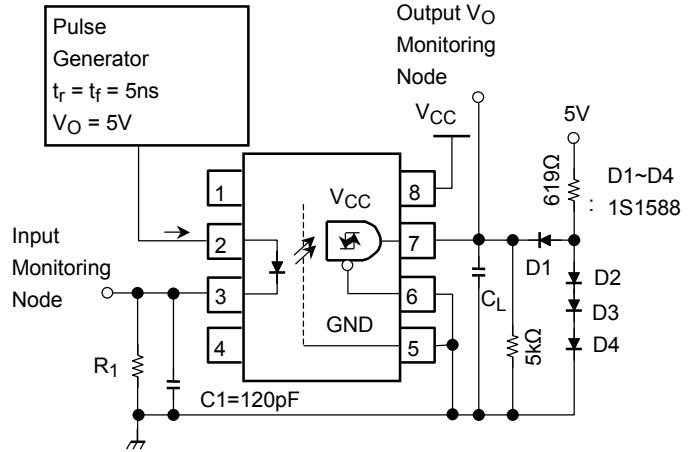
(Note 6) CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O \leq 0.8\text{V}$).

CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O \leq 2.0\text{V}$).

Test Circuit 1 t_{pHL} , t_{pLH} , t_r and t_f

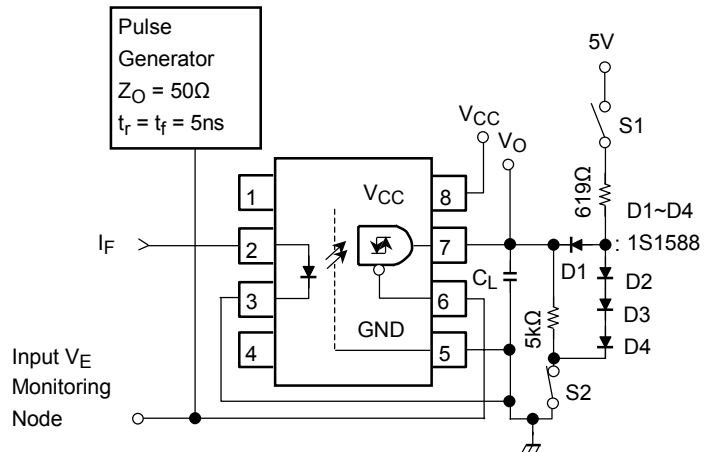
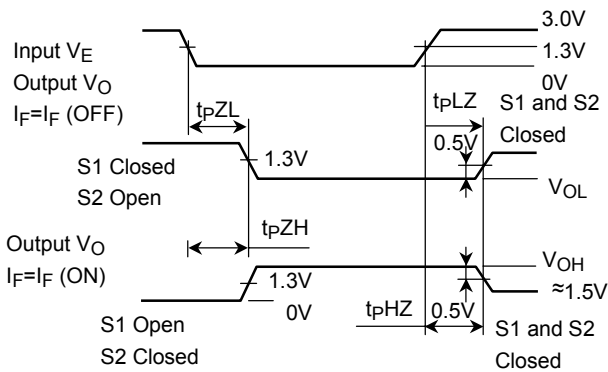


R_1	2.15k Ω	1.1k Ω	681 Ω
$I_F(ON)$	1.6mA	3mA	5mA



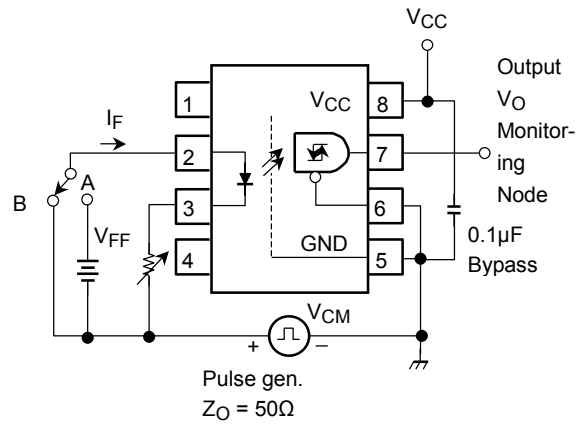
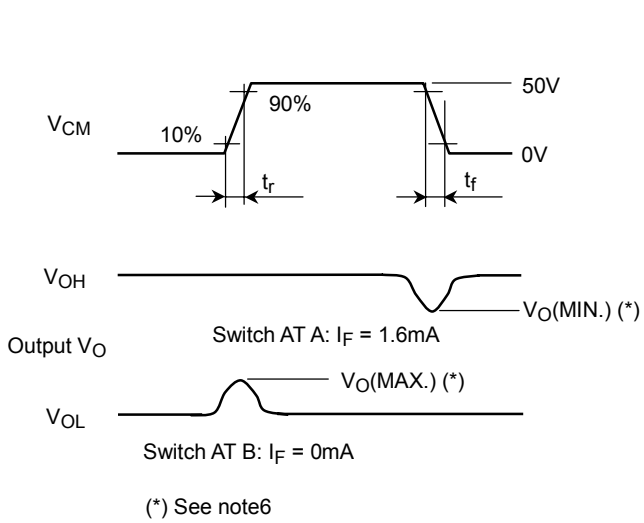
C_1 is peaking capacitor. The probe and jig capacitances are include in C_1 .
 C_L is approximately 15pF which includes probe and stray wiring capacitance.

Test Circuit 2 t_{pHZ} , t_{pZH} , t_{pLZ} and t_{pZL}



C_L is approximately 15pF which includes probe and stray wiring capacitance.

Test Circuit 3 Common Mode Transient Immunity



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