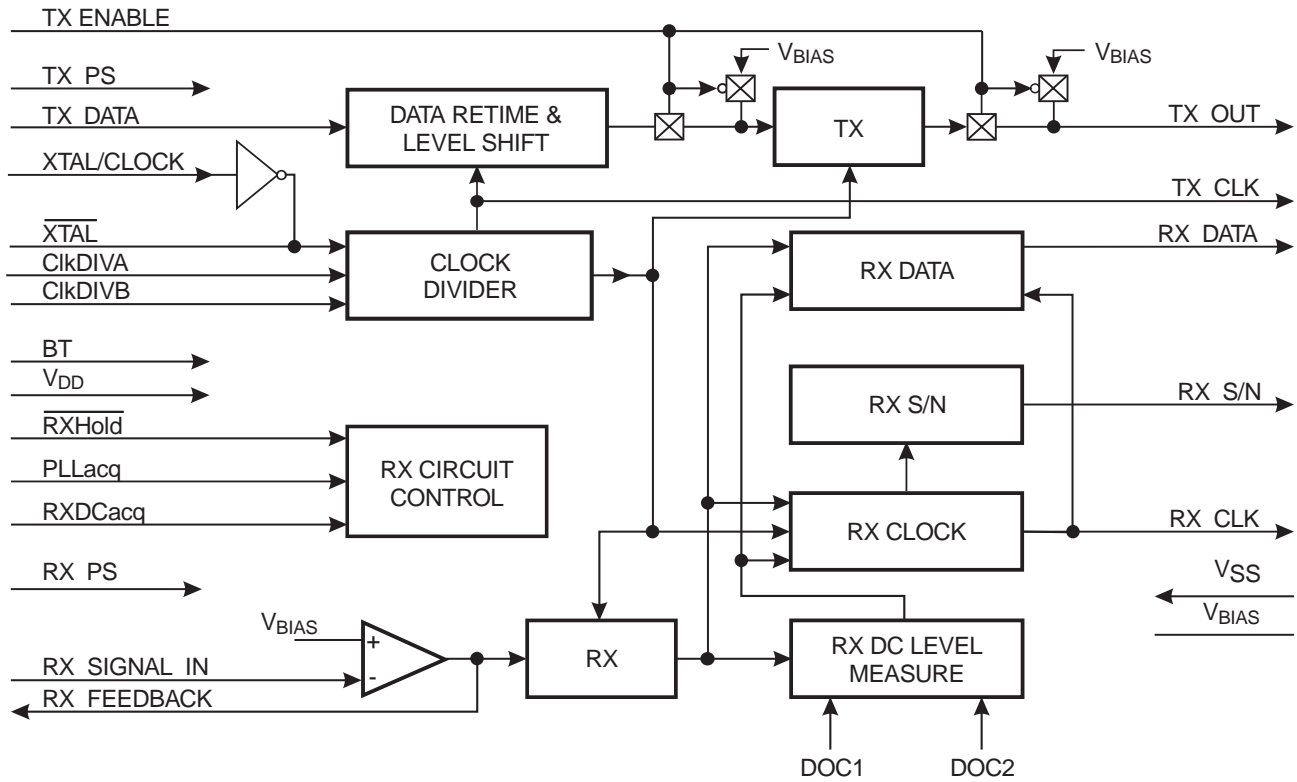


MX•COM, INC. MiXed Signal ICs

APPLICATION NOTE

MX589 GMSK MODEM Application



This application note is to be read in conjunction with the current MX589 Data Bulletin. This document is issued to clarify points in currently published documents and to present new information that will enable the user to easily understand and implement this GMSK product.

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1. Data Transmission by FM Radio

The simplest method of sending data over FM radio is to shift the RF carrier frequency in one direction to represent a logic '1' and in the other direction for a logic '0'. This direct method is known as Frequency Shift Keying (FSK); FSK can be successful but results in a very wide transmission bandwidth requirement.

To reduce the transmission bandwidth required input data may be pre-filtered prior to modulation using a specific form of lowpass filtering. One effective method is Gaussian Filtered Minimum Shift Keying (GMSK). Figure 4 is a comparison of the bandwidth requirements of direct FSK and Gaussian filtered data.

2. Gaussian Filtered Minimum Shift Keying (GMSK)

GMSK is a method of data modulation for sending high-speed data in narrow band FM radio channels.

In its simplest form, GMSK involves passing a digital bitstream through a Gaussian filter before applying it to the input of a frequency modulator.

A Gaussian filter is a lowpass element which when excited by an impulse at its input, gives a Gaussian shaped output response.



Figure 1: The Performance of a Gaussian filter

3. GMSK in FM Radio

In an FM radio system using a GMSK modem the data flow is as shown below:

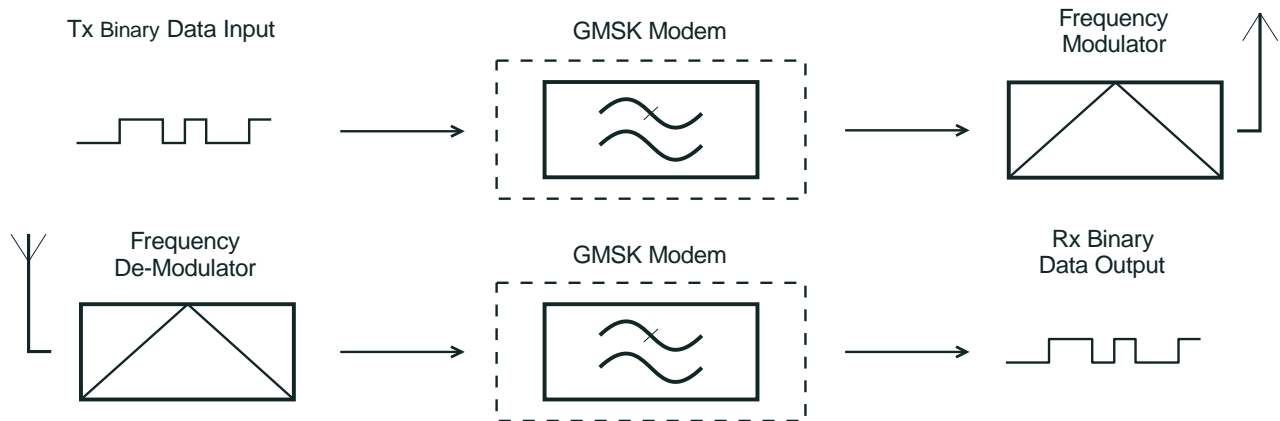


Figure 2: Data flow in a GMSK FM Radio Modem

4. GMSK

The diagram below shows GMSK filter outputs for a logic input of '10001000'. Note that a filter delay is present and that the individual output pulse spreads across more than one bit-period.

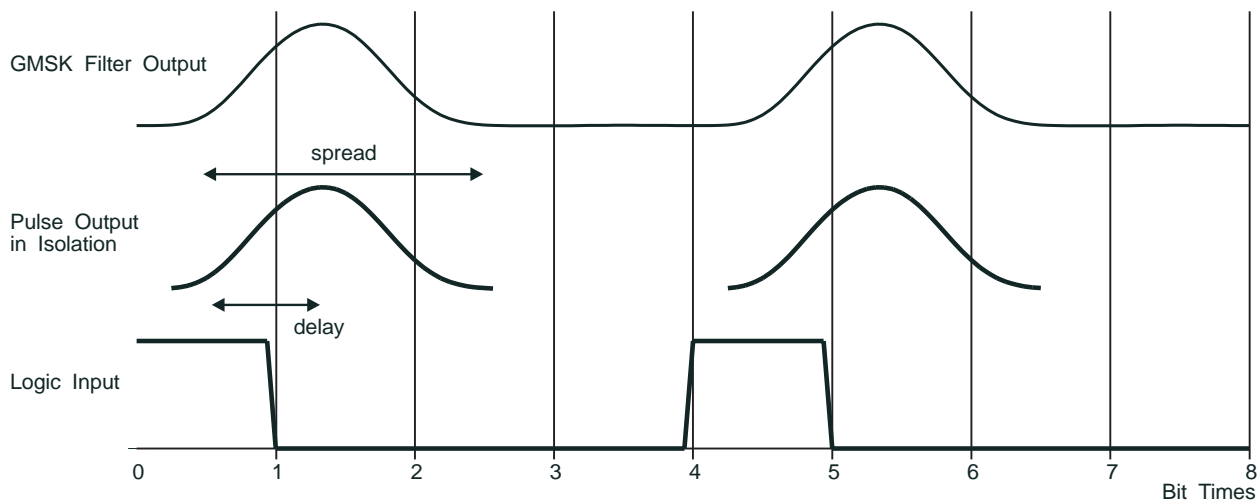


Figure 3: GMSK Filter Input/Output Relationships

True GMSK transmission, in radio, is achieved when the data output of the Gaussian filter is passed through an FM modulator having a continuous phase response, with peak deviation being set to half of the applied bit rate.

$$\text{Max deviation (Hz)} = \frac{\text{Data Rate}}{2}$$

For example: $DEV_{MAX} = 2\text{kHz}$ for a data rate of 4kbps

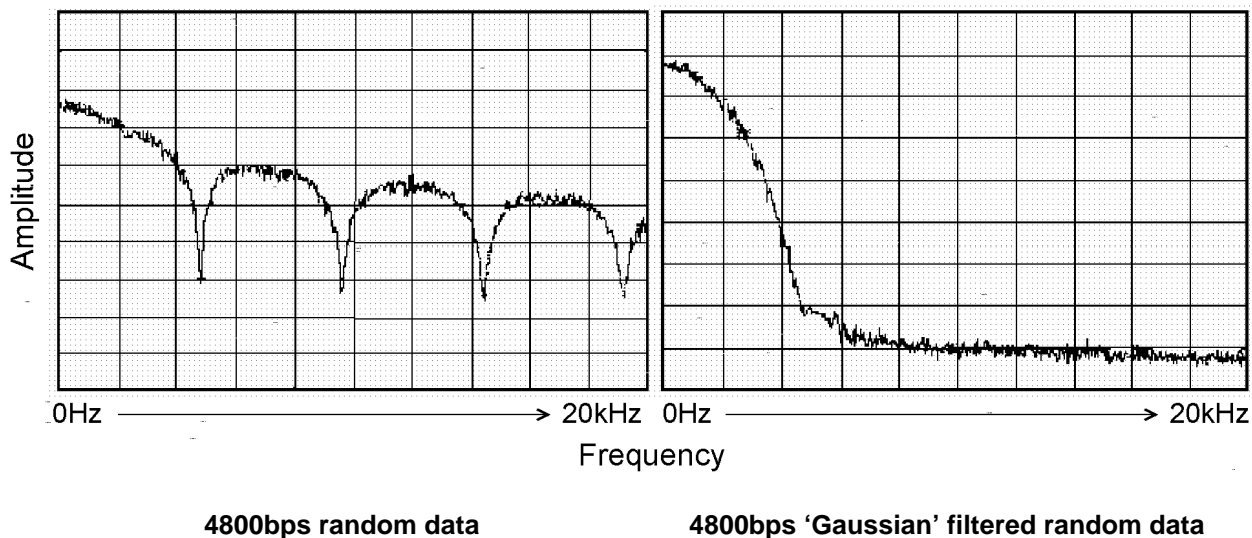


Figure 4: Spectral Comparison of FSK and Gaussian MSK Requirements

5. Implementation of GMSK using the MX589

GMSK, as a form of modulation for high-speed data transfer is relatively simple to implement as long as careful attention is paid to several points:

5.1 Bitrate, BT, and Bandwidth

The maximum data rate that can be transmitted over a radio channel depends on the following:

1. Channel spacing
2. Allowable adjacent channel interference
3. Tx filter bandwidth (BT)
4. Peak carrier deviation (Modulation Index)
5. Tx and Rx carrier frequency accuracy
6. Modulator and Demodulator linearity
7. Rx IF filter frequency and phase characteristics
8. Use of error correction techniques
9. Acceptable error-rate

5.2 Data Formats

The receive section of the MX589 gives the lowest bit error rate with data which has a reasonably 'random' structure --the data should contain approximately the same number of 'ones' as 'zeros' with no long sequences of consecutive 'ones' or 'zeroes'.

5.3 Coupling of Rx and Tx signals

Ideally, the Rx demodulator should be DC coupled to the MX589 'Rx Signal In' pin (with a DC bias added to center the signal around $V_{BIAS} [= V_{DD}/2]$), however AC coupling can be used provided that -

1. The 3dB cut-off frequency is 20Hz (at 8kbps) or below (i.e. a 0.1uF capacitor in series with 100k Ω). The cut-off frequency requirement changes proportionally with the applied data rate.
2. The data does not contain long sequences (in excess of 100 bits) of consecutive ones or zeroes.
3. Sufficient time is allowed after a step change at the discriminator output (resulting from channel changing or the appearance of a RF carrier) for the voltage into the MX589 to settle before the 'RxDCacq' line is strobed.

In practical applications, it will usually be possible to arrange for any AC coupling between the MX589 Tx output and the frequency modulator to cut-off at a very low frequency such as 5.0Hz, but AC coupling between the receive discriminator and the input of the MX589 may need to have a shorter time constant to avoid problems with voltage steps at the output of the discriminator when changing channels or when the distant transmitter turns on.

For these reasons, as well as to maintain reasonable BER, the optimum -3dB cut-off frequencies are around 5Hz in the Tx path, 20Hz in Rx, at 8kbps.

Figure 5 shows the typical static Bit-Error-Rate performance of the MX589 operating under nominal conditions (8kbps, $V_{DD}=5.0V$, $T_{AMB}=25^{\circ}C$, Tx BT=0.3) for various degrees of AC coupling at the Rx Input and the Tx Output.

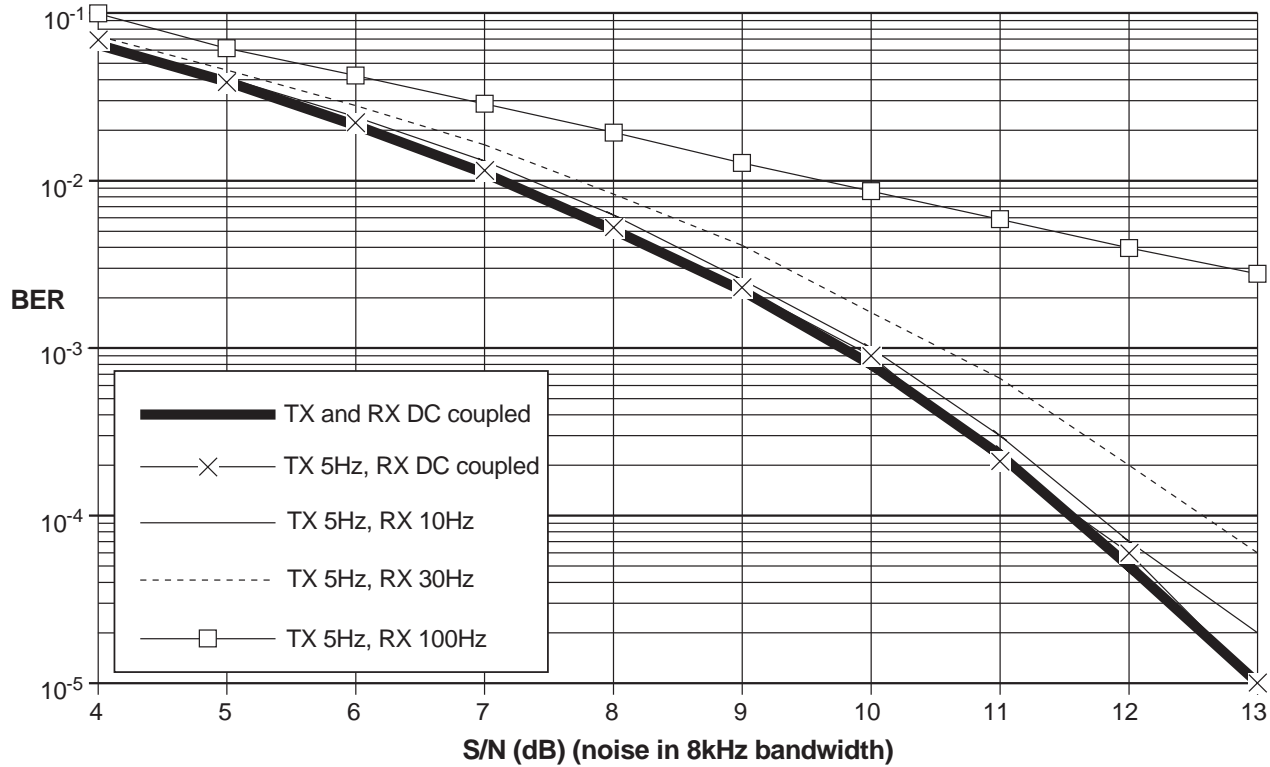


Figure 5: Typical Static Bit Error Rates

5.4 Baseband and RF Bandwidth

The required baseband bandwidth, and therefore the RF bandwidth requirement of a GMSK system is principally determined by two factors: the data rate and the system filter's response. The response characteristic with respect to an applied data rate is referred to as the system BT (bandwidth - data rate) factor.

The BT factor is the ratio of the -3dB point of the filter (-3dBf₀) and the applied data rate.

$$BT = \frac{-3dBf_0}{Data\ Rate} \quad \text{i.e. } -3dBf_0 = BT \times Data\ Rate$$

As can be seen from Figure 6, a lower BT figure (0.3) allows less high-frequency components and produces, theoretically, a narrower bandwidth requirement. However, the interference caused by one bit symbol overlapping another (intersymbol interference) is increased (Figure 7).

The MX589 is capable, within the current specification, of operating to data rates of between 4kbps and 40kbps at a BT of 0.3 and 0.5; Table 1 provides a very rough guide to GMSK capabilities in narrow RF bandwidths. However, the details of the relevant system specification should always be adhered to.

Figure 6 shows the MX589 Tx filter response at BT values of 0.3 and 0.5.

BT	Channel Bandwidth (kHz)	Data Rate Max. (bps)	BT	Channel Bandwidth (kHz)	Data Rate Max. (bps)
0.5	12.5	4800	0.3	12.5	8000
0.5	25.0	9600	0.3	25.0	16000
0.5	50.0	19200	0.3	50.0	32000

Table 1: Typical GMSK/Bandwidth Capabilities

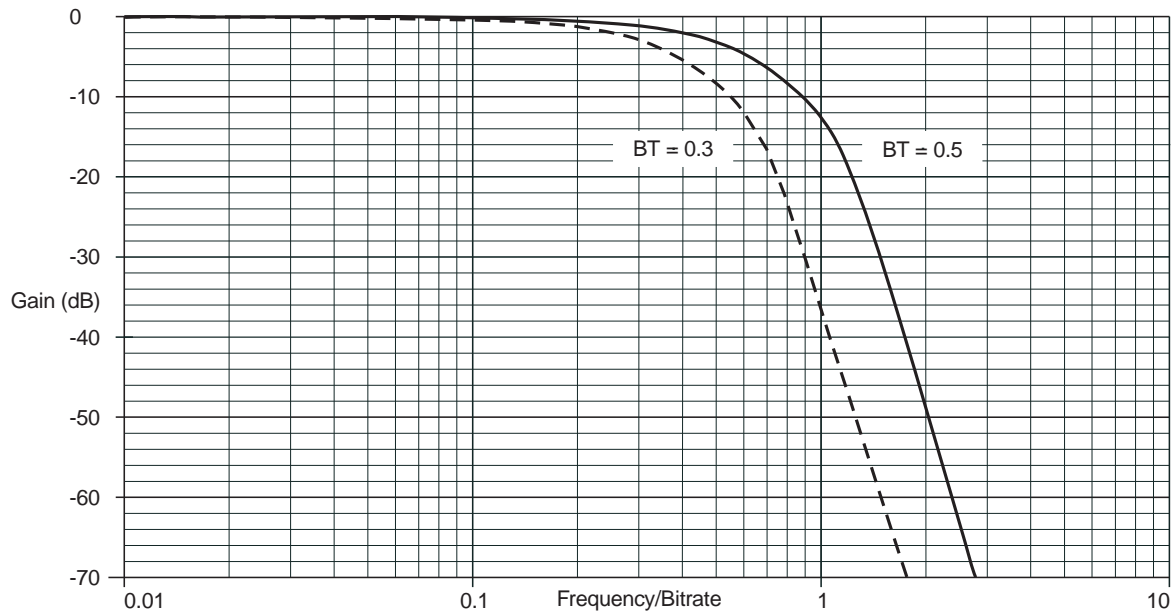


Figure 6: MX589 Tx Filter Response

5.5 Intersymbol Interference

This is the effect of one data bit overlapping the next due to the lowpass filtering. As this effect becomes more pronounced the receiving modem may have trouble deciding whether the bit is a '1' or a '0'.

Figure 7 shows the output of the GMSK modem for an input of "1 1 0 1 1 1 1" with BT settings of 0.5 and 0.3; the increasing effect of intersymbol interference can be clearly seen.

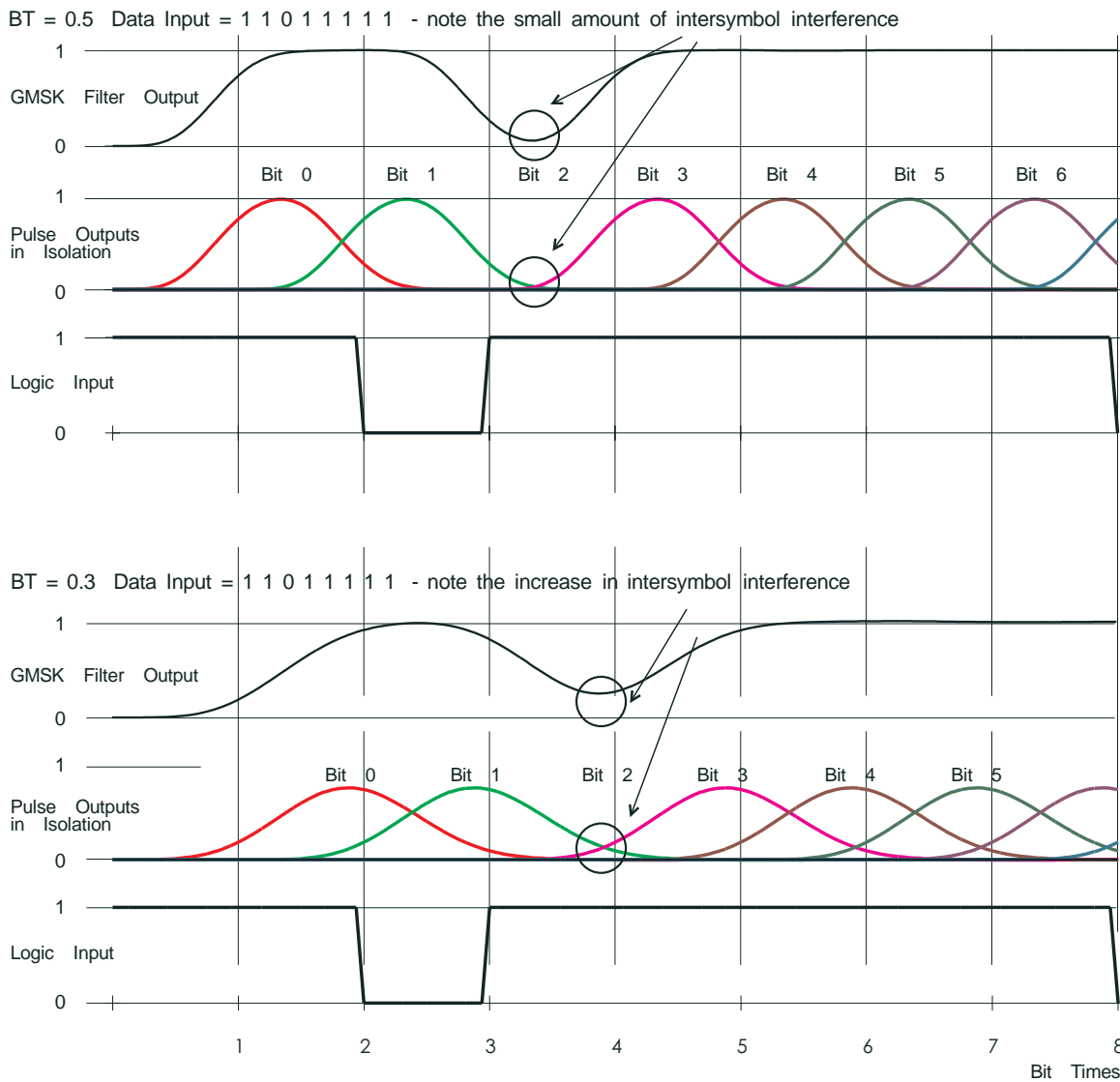


Figure 7: Illustration of Intersymbol Interference Increase due to Decrease in BT Value

6. FM Modulator, Demodulator, and IF Performance

6.1 The Eye Pattern

The EYE pattern diagram is an oscilloscope-type trace of the baseband signal (at the input to the FM modulator or at the output of the FM discriminator).

It is an indication of the condition of the signal and its path and therefore the FM modulator, demodulator, IF circuit, and channel circuit performance.

The EYE diagram provides information about the following parameters of the signal and/or system:

Channel signal/noise conditions -

Channel amplitude and phase responses -

For optimum performance, the EYE pattern of the received signal applied to the MX589 for random transmitted data should be as close as possible to the examples given in Figure 9.

Of particular importance are general symmetry, cleanliness of the zero-crossings, and for a BT of 0.3, the relative amplitude of the inner eye opening (which should be approximately 0.48 of the total for a BT of 0.3, about 0.9 for a BT of 0.5).

To achieve this, attention must be paid to -

1. Linearity and frequency/phase response of the Tx frequency modulator and discriminator. The modulator frequency response should extend down to a few Hertz; two-point modulation is necessary for synthesized radios.
2. Bandwidth and phase response of the Rx IF filters.
3. Accuracy of the Tx and Rx carrier frequencies -any difference will shift the received signal towards one of the skirts of the IF filter response.

The diagrams on the following pages provide examples of various EYE patterns and their causes.

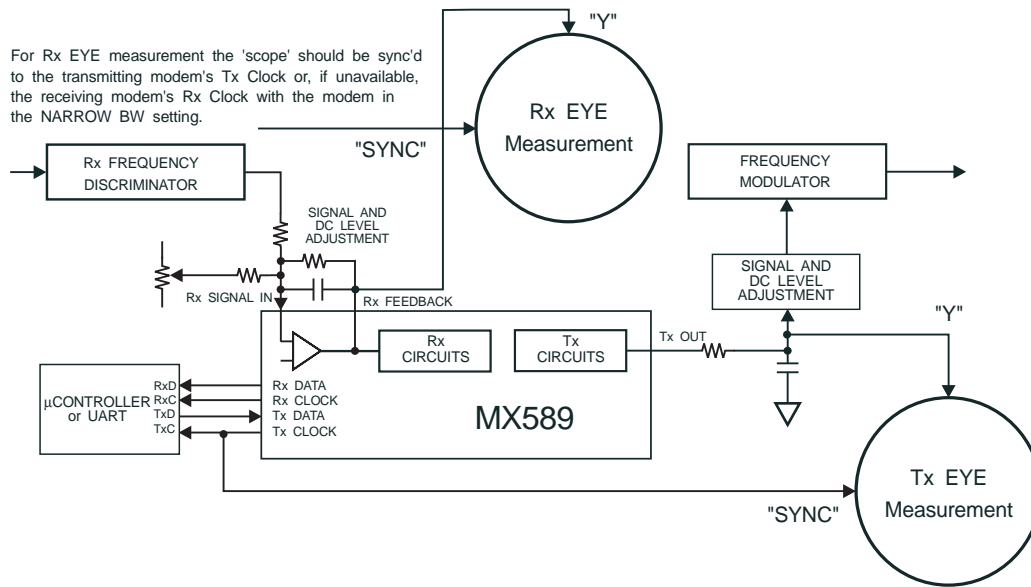


Figure 8: Measurement of an EYE Pattern

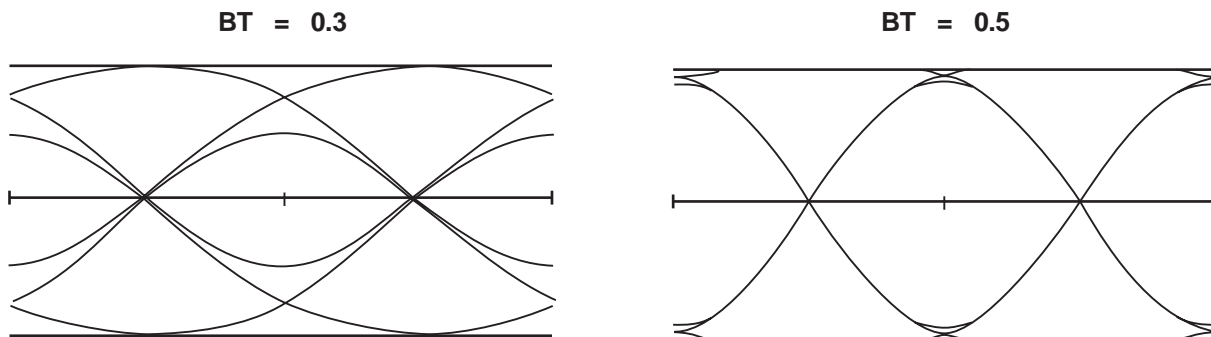


Figure 9: Typical Good EYE Patterns diagrams

6.1.1 Example Eye Patterns

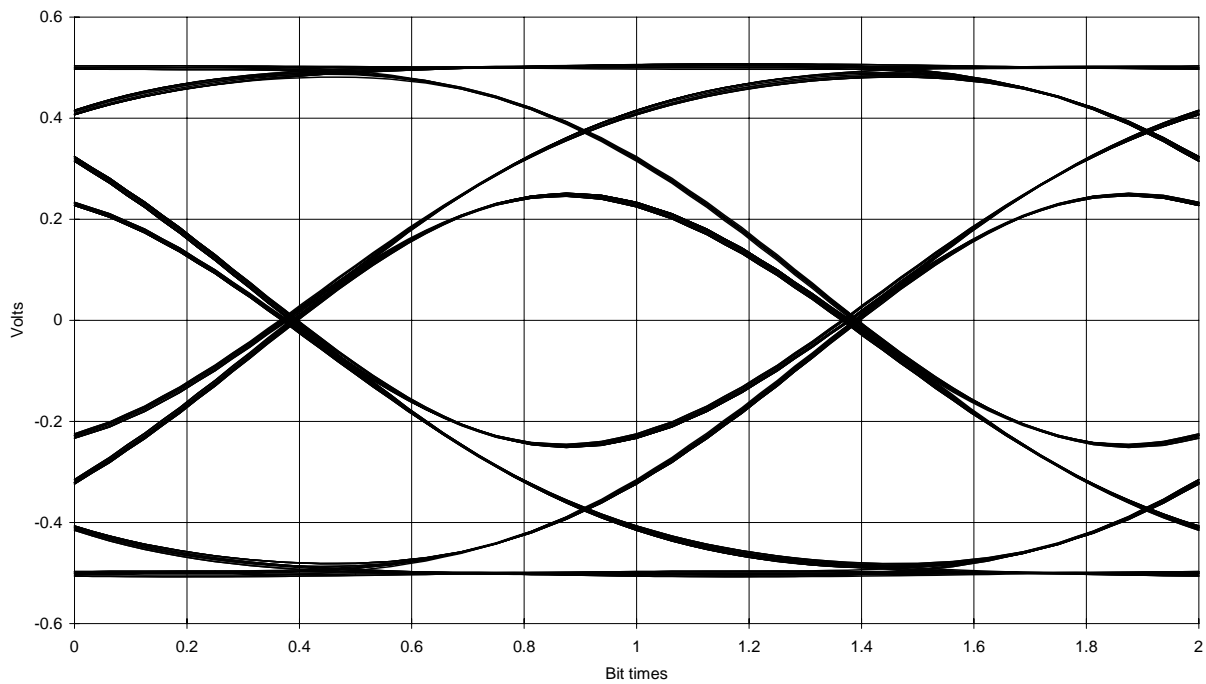


Figure 10: Good Rx EYE (BT = 0.3)

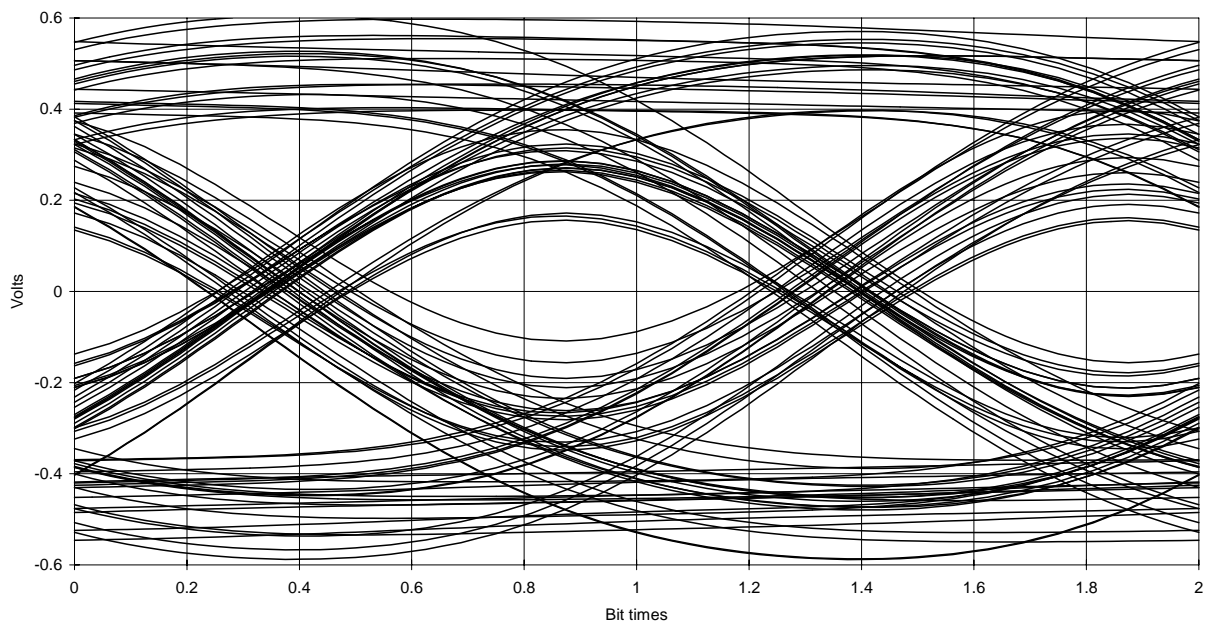


Figure 11: Effect of AC coupling (BT = 0.3)
Corner frequency approx. 1% of bitrate

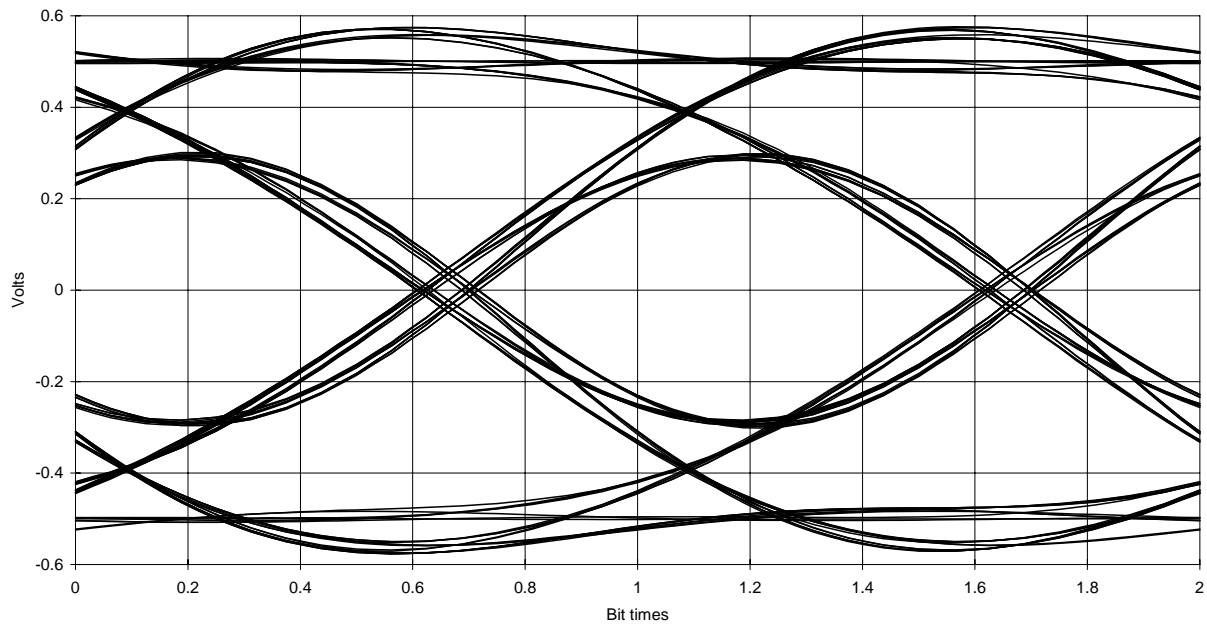


Figure 12: Effect of Poor Channel Amplitude and Phase Response (BT = 0.3)

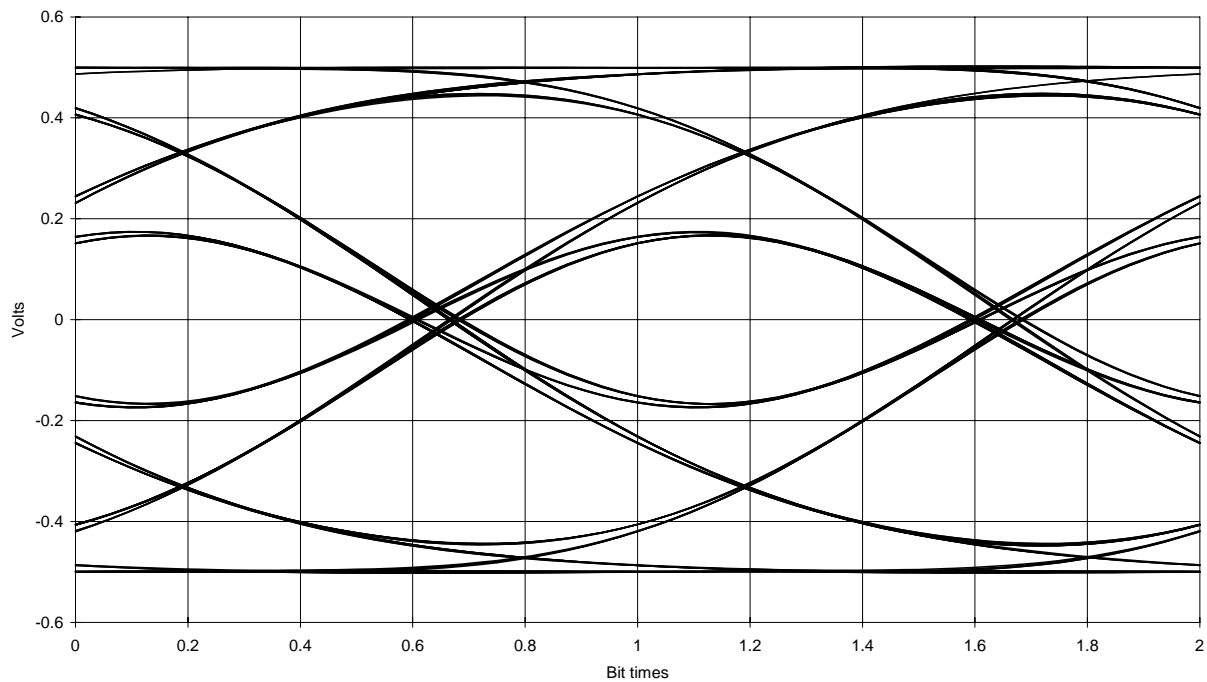


Figure 13: Effect of Slight High Frequency Attenuation (BT = 0.3)
6dB/octave low pass filtering, -3dB at 0.5 x bitrate

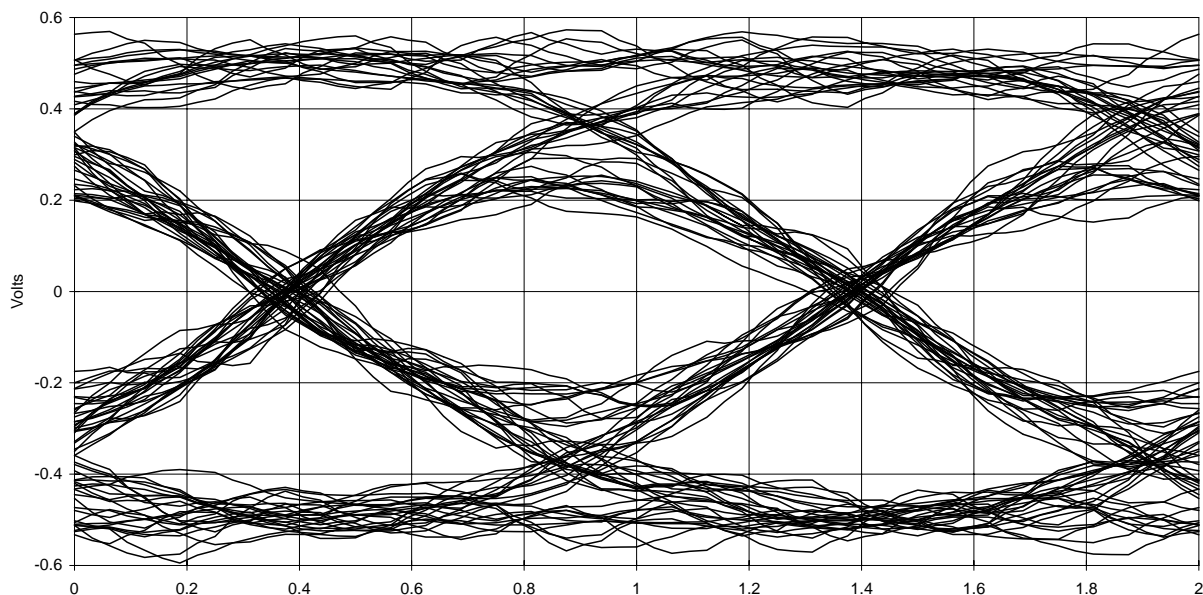


Figure 14: Effect of Noise (BT = 0.3)
Noise Bandwidth = 2 x bitrate; S/N = 25dB

7. Data Sequencing

To ensure that the MX589 Rx clock recovery and Rx level circuits are given the best opportunity to operate correctly the receive section works best with data which has a reasonably 'random' structure. The data should contain approximately the same number of 'ones' as 'zeroes' with no long sequences of consecutive 'ones' or 'zeroes'. Also, long sequences (>100 bits) of '10101010 ...' patterns should be avoided. For this reason, it is recommended that data be scrambled in some manner before transmission.

A string of logic 1's will be modulated as a single frequency shift at the beginning of the string and a single frequency shift at the end; no frequency changes will occur. This will appear at the Rx modem as near DC and can result in the receiver not being able to track the incoming signal correctly. Both bit timing and level information can be lost.

Particularly when a BT value of 0.3 is being used problems also occur when single bits bounded by their complement are being sent repeatedly ('0000010000' or '111101111' note however, that these are not the only patterns to give problems); these sequences sent many times over can cause the GMSK demodulator to give out bits in error.

Where data is transmitted in bursts, each burst should be preceded by a preamble designed to allow the receive modem to establish timing and level lock as quickly as possible. This preamble should be at least 16 bits long, and should preferably consist of alternating pairs of '1's and '0's i.e. '110011001100'; the pattern '10101010' should be avoided, particularly when BT = 0.3.

Many FSK and FFSK data systems use a '10101010...' pattern as a synchronizing preamble, Figure 15A shows the resultant output from a system using BT values of both 0.5 and 0.3.

In this case the output of a BT = 0.3 system does not provide true level information for the level measuring circuits to lock on to. When the BT is 0.5 the output does not display the problem to the same degree.

Figure 15B, Figure 15C, and Figure 15D show outputs from inputs of '11001100...', '111100001111...' and '010000100...' respectively. Where it is impossible for data to be provided to the modem within the above guidelines, it is recommended that external sequencing is used; i.e. scrambling or data coding.

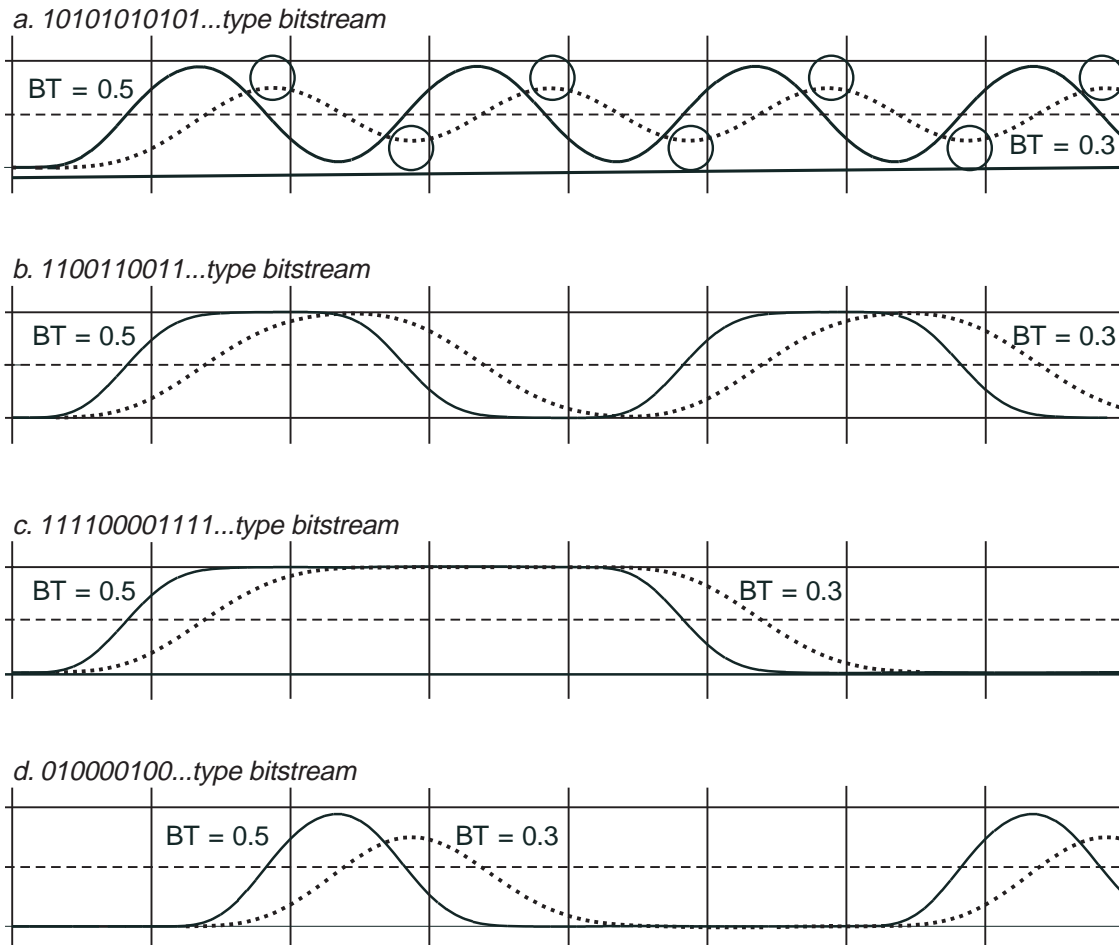


Figure 15: GMSK Output Levels for Various Input Bit Configurations

7.1 Data Randomizing (Scrambling)

As previously discussed, the receive section of the MX589 prefers data which has a reasonably 'random' structure. Whether the applied data (digital bits) originate from a computer type system or by voice digitization, it is not always possible to ensure that streams of constant-'sense' Rx data are avoided.

Illustrated below are two simple ways to randomize data:

1. Exclusive-OR the input binary data with a pseudo-random binary stream. This method will require both Rx and Tx pseudo-random codes to be in sync.
2. Exclusive-OR the input binary data with a shifted input data stream. A self-synchronizing method which exclusive-OR's the Rx input data with a time-shifted version of itself. This method of randomizing will propagate bit errors as any Rx bit in error will be duplicated with each EX-OR function in the loop. This method is in accordance with CCITT recommendations (V.26 ter)

Preamble bits and/or SYNC words should not, of course, be randomized.

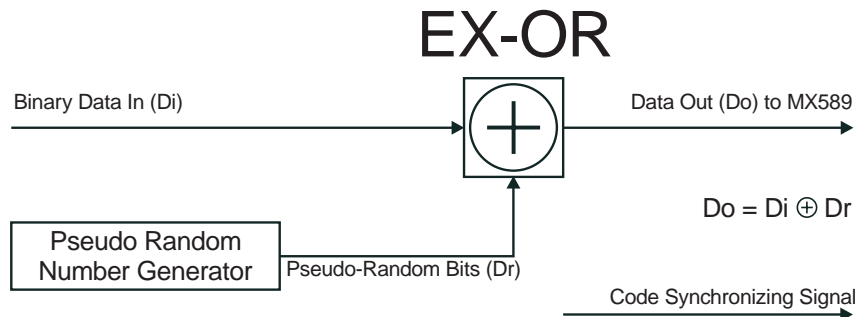


Figure 16: Exclusive-OR the Input with a Pseudo-Random Data Stream

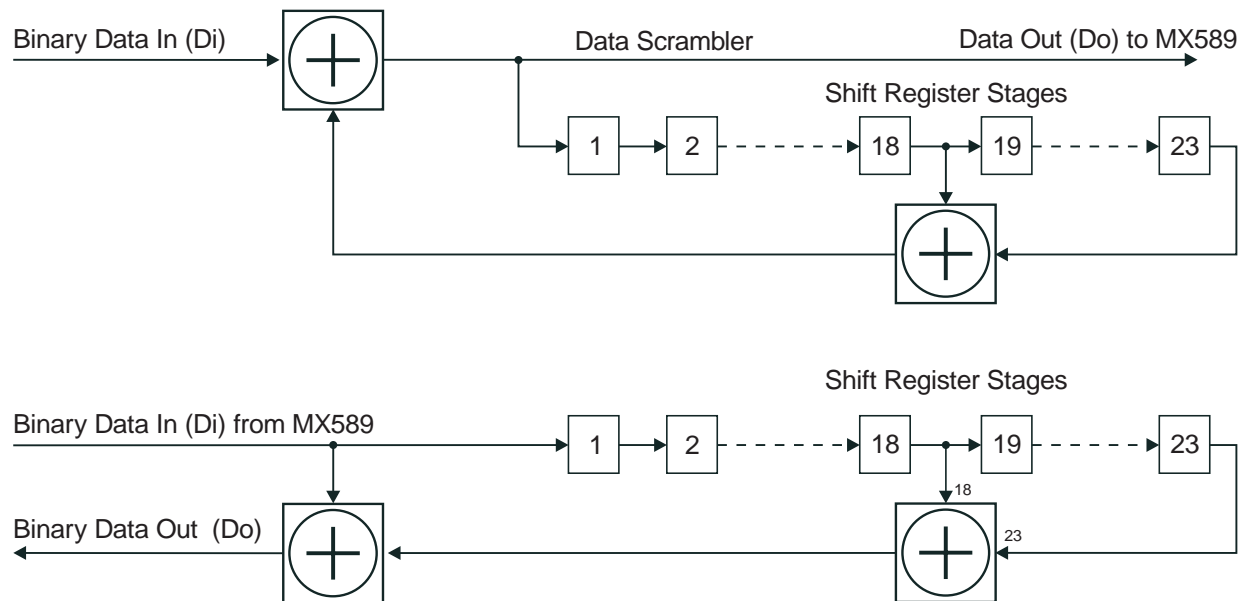


Figure 17: Exclusive-OR the Input with a Shifted Input Data Stream

7.2 Data Coding

If it is important, for hardware or system interface considerations, that the lower frequency limit of a GMSK signal is kept above a specific frequency it is possible to deliberately encode the data prior to modulation; for instance where AC coupling is employed or there are PLL control limits.

This entails ensuring that sequences (blocks) of bits that contain low –frequency components are altered to produce the required overall output. This coding can be carried out in software or hardware, as appropriate. It should be noted that if coding that results in an increase in the number of bits is used this will reduce the actual system ‘data rate’ unless the bit rate is increased, which in turn may take the system outside the bandwidth specification.

8. Rx ‘Acquisition’ and ‘Hold’ Modes

The MX589 may be expected to receive data efficiently under several different signal and configuration conditions depending upon the system formatting and the device coupling methods.

Conditions identified so far are:

Rx with Carrier Detect Indication

Rx with No Carrier Detect Indication

The upper and lower voltage levels of the input signal, after internal filtering, are stored on external capacitors connected to the Doc1 and Doc2 pins. These are used to generate levels inside the device to enable the detection of zero-crossings and to extract the received binary data.

As data is received, the values stored on these capacitors are updated to track amplitude variations and drift, unless ‘Hold’ is selected in which case the voltages will decay very slowly towards V_{BIAS} .

The voltages on the Doc1 and Doc2 pins reflect the average peak positive and negative excursions of the (filtered) receive signal, and could therefore be used to derive a measure of the data signal amplitude.

Note however, that these pins are driven from very high-impedance circuits, so that the DC load presented by any external circuitry should exceed $10M\Omega$ to V_{BIAS} .

8.1 Rx Acquisition with Carrier Detect Indication

The MX589 can tolerate DC offsets in the received signal of at least $\pm 10\%V_{DD}$ with respect to V_{BIAS} , however to ensure that the DC offset compensation circuit operates correctly and with minimum delay, 'Low' to 'High' transitions of the 'RxDcAcq' and 'PLLaq' inputs should occur after the mean input voltage to the MX589 has settled to within about 0.1V of its final value (Note that this can place restrictions on the value of any series signal coupling capacitor).

1. MX589 connected as Figure 2 in the current Data Sheet; inputs RxDcAcq and PLLacq 'Low';
2. At the receipt of an RF carrier detect indication to the μC : wait two bit periods; place RxDcAcq and PLLacq 'High' ('clamp' - Doc1 and Doc2 capacitors are rapidly charged towards a voltage midway between the Rx signal level and V_{BIAS}). The 'RxDcAcq' and 'PLLaq' inputs must be placed 'High' for a minimum of 16 bits at the start of reception to ensure that the DC measurement and timing extraction circuits lock on to the received signal correctly. To confirm that 'lock' has been achieved it may be necessary to employ additional methods of sync detect; such as a frame detection or MX589 S/N output monitoring.
3. To give the MX589 a satisfactory reference level to 'clamp' to, it is recommended that the transmitting station is configured to provide a short period of blank carrier before the data starts.
To calculate this period the following system parameters should be considered: Tx power-up time + Rx demodulator settling time + Rx AC coupling values [+ 2 bit times].
4. When lock is confirmed the above inputs should be taken 'Low' again and the acquisition circuits operated as described in the Data Sheet.

In most applications, there will be a DC step in the output voltage from the receiver FM discriminator due to carrier frequency offsets as channels are changed or when the distant transmitter is turned on. Every time a channel change occurs, the preamble/acquire sequence (steps 1 - 4) should be performed.

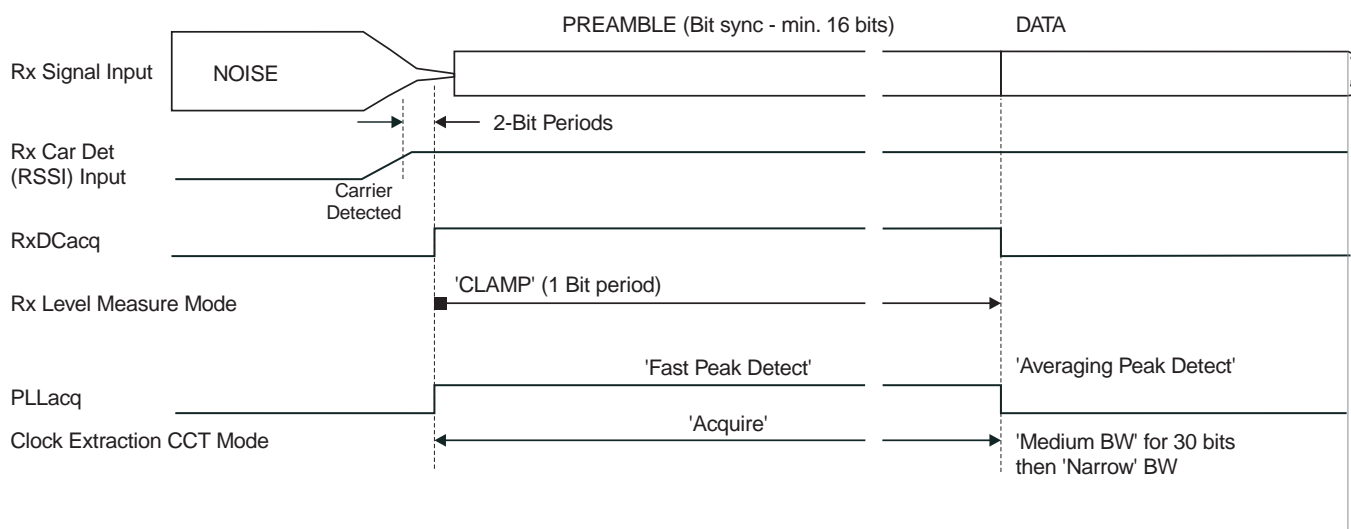


Figure 18: Rx Acquisition with Carrier Detect Available

8.2 Rx Acquire Sequences

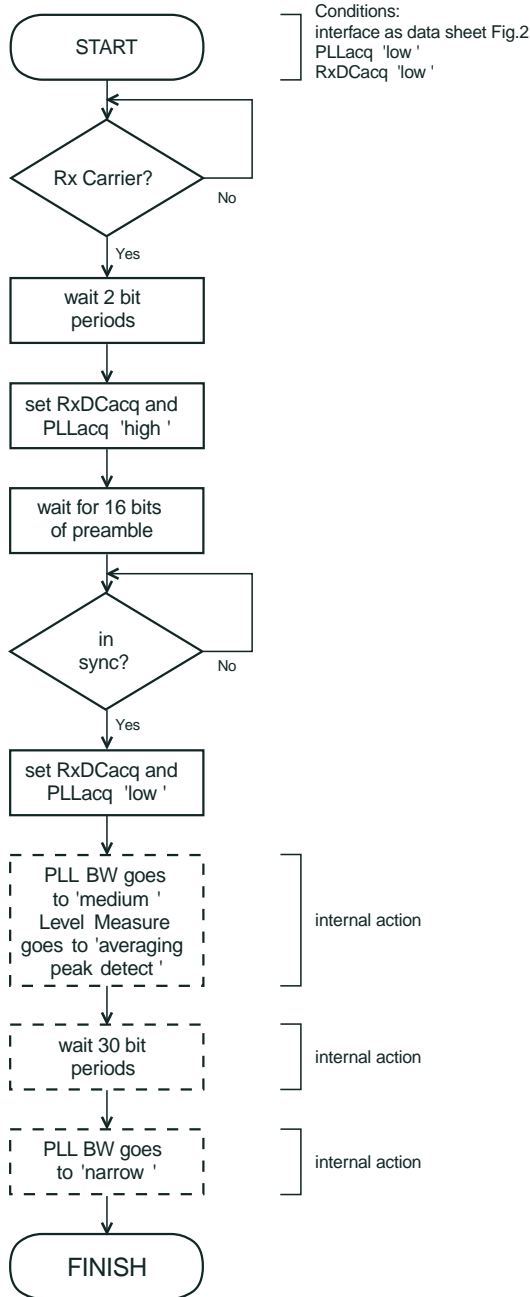


Figure 19: Rx/Data Carrier Indication Available

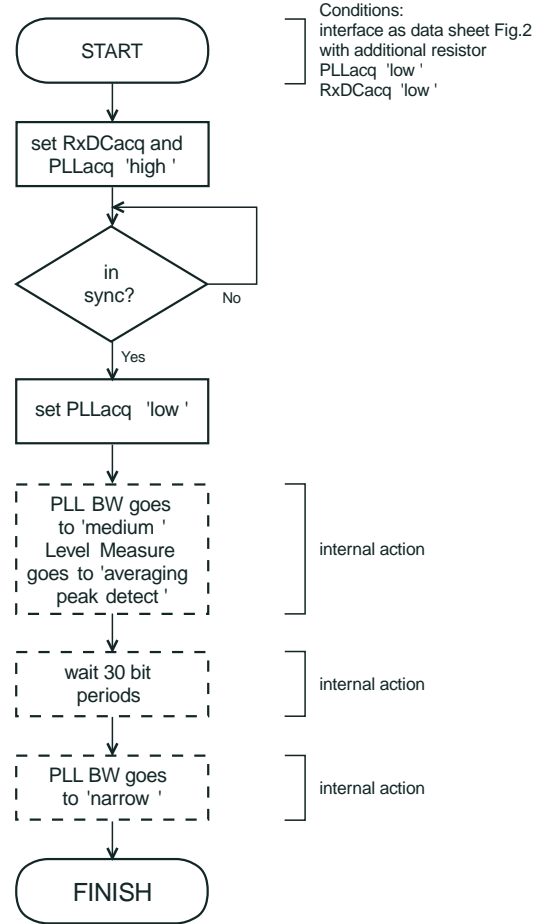


Figure 20: No Rx/Data Carrier Indication Available

8.3 'RxHold' Input

'RxHold' Input

As well as using the 'Rx Hold' input to freeze the Level Measuring and Clock Extraction circuits during a signal 'fade', it may also be used in systems which employ a continuously transmitting control channel to freeze the receive circuitry during transmission of a data packet, allowing reception to resume afterwards without losing bit synchronization. To achieve this, the MX589 'Xtal' clock needs to be accurate enough that the derived 'RxClock' output does not drift by more than about 0.1 bit time from the actual received data timing during the time that the 'RxHold' input is 'Low'.

The 'RxDcacq' input, however, may need to be pulsed 'High' to re-establish the level measurements if the 'RxHold' input is 'Low' for more that a few hundred bit-times.

8.4 Rx Acquisition with No Carrier Detect Indications

If the receive system has no method of indicating when the RF carrier or signal preamble will start it is recommended that:

1. With reference to the current MX589 Data Sheet, Figure 2, a new component, resistor R, of value between $1.0M\Omega$ and $2.0M\Omega$, should be connected across output pins Doc1 and Doc2.
2. RxDCacq and PLLacq inputs set 'Low'.
3. Before or when the required signal is expected to appear: Set RxDCacq and PLLacq 'High'; the modem acquisition circuits will clamp and then lock and track the data. The RxDCacq pin setting may remain in this position for the duration of operation.
4. The PLLacq pin should be taken 'Low' when lock has been confirmed to improve the signal-to-noise performance by reducing the PLL bandwidth. With the additional resistor, R, connected, there is no advantage in taking the RXDCacq input 'Low' again to attain the Averaging Peak Detect mode.
5. If the received signal has a long preamble sequence, e.g. 100bits, RxDCacq and PLLacq settings may remain low; the circuitry will eventually attain lock.

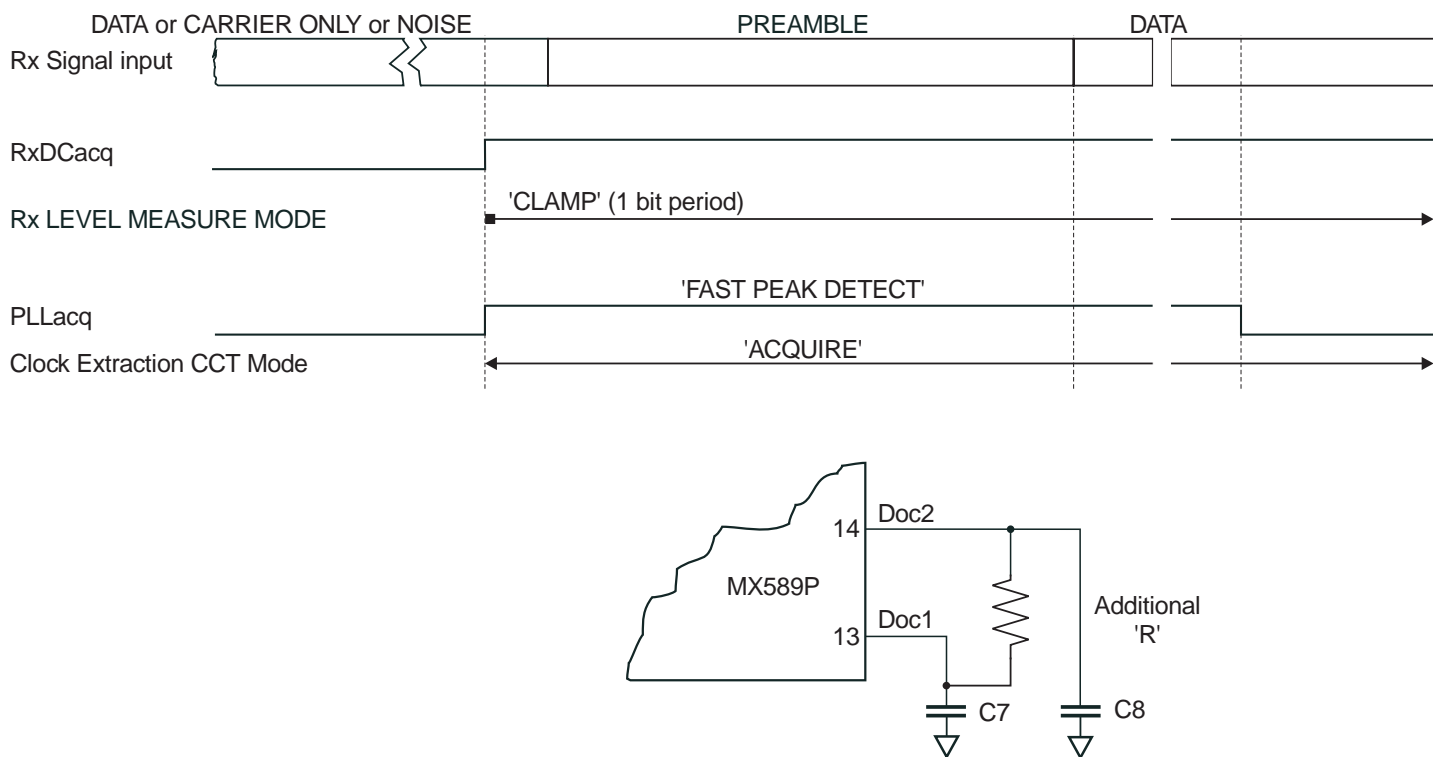


Figure 21: Rx Acquisition with No Carrier Detect Available

9. Interleaving on Systems with Forward Error Correction (FEC)

Data for transmission, with its FEC overhead, is loaded to the MX589 serially.

If, during transmission, a section of data bits (block) is corrupted by some external disturbance (ignition interference etc.) there is a possibility that a whole block (or blocks) of data will be damaged making large amounts of data at the Rx uncorrectable and therefore unreadable. This will result in a request for a re-transmission and reduction in the overall data rate.

If however, prior to loading to the modem, the data bits within blocks are interchanged between blocks (interleaved), then if external disturbance is experienced and a section is damaged, when the blocks are rebuilt (de-interleaved) at the receiver only one or two of the bits in each original block of data will be in error therefore allowing the FEC system a better chance of correction.

With reference to the example in Figure 22, interleaving is carried out externally, prior to loading the modem. Data is supplied to the interleaving process in the following sequence (real data):

A1, A2, A3, A4,H9, H10

and read-out from the process in the following sequence (interleaved data):

H1, G1, F1, E1, ...H2, G2, B10, A10.

De-interleaving is the reverse process.

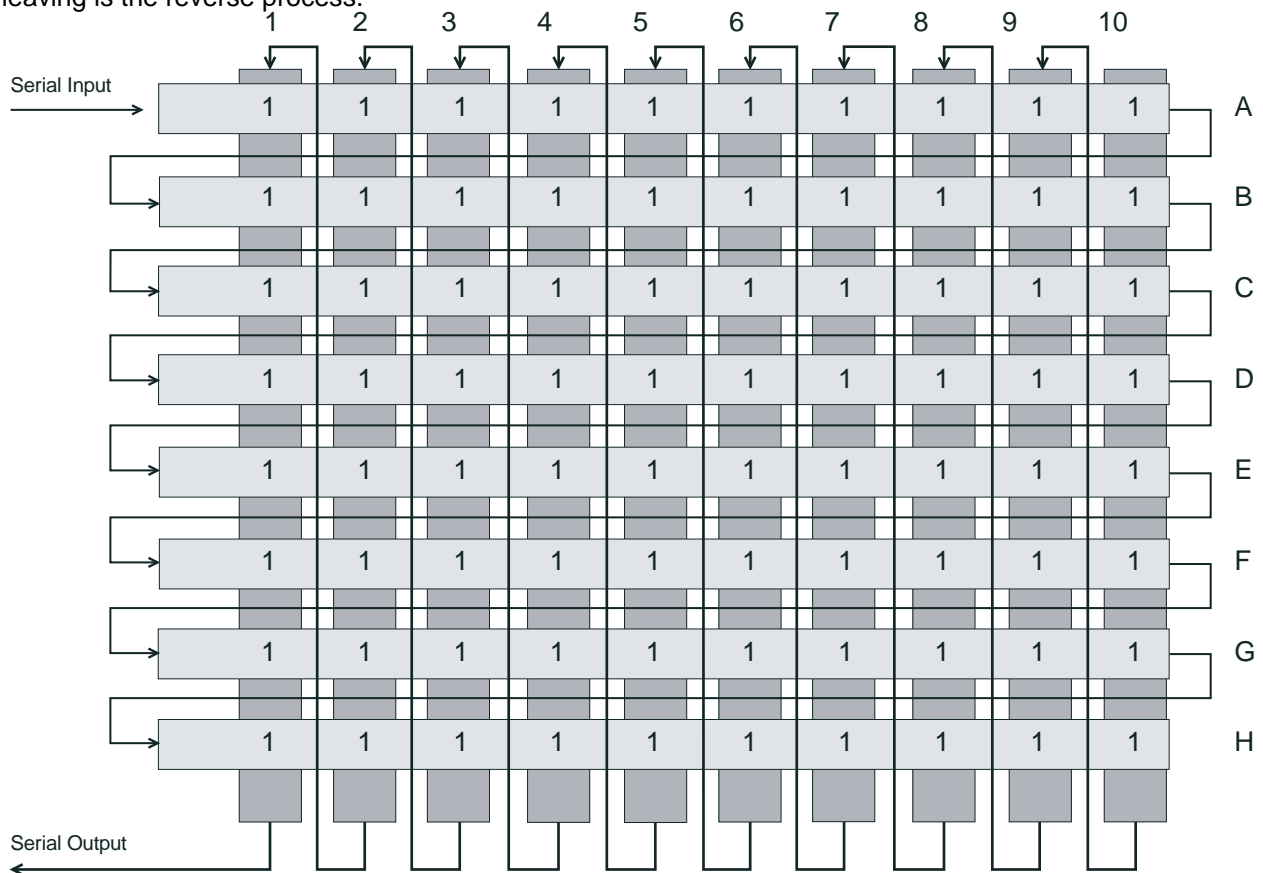


Figure 22: Interleave Example

10. Alternative Data Rates

The current MX589 Data Sheet specifies device operation at data rates of between 4kbps and 64kbps at 5.0 volts and Xtal/clock frequencies of between 1.0MHz and 10.4MHz.

To enable this device to be used, efficiently, in the maximum number of data transfer applications, this Application Note details tables that are intended to provide more information to operate at data rates other than those illustrated in the data sheet.

With due regard to the operating V_{DD} values recommended in the Data Sheet, the following parameters control/affect the data rate operation of this device:

Clock Oscillators and Dividers.

Tx OUT output external component (R1 and C1) values.

The values of Doc1 and Doc2 capacitors (C7 and C8). Note that peripheral components to the Rx Level Measurement circuitry, should also be considered.

10.1 Clock Oscillator and Dividers

The Tx and (nominal) Rx data rates are determined by division of the frequency present at the Xtal pin, which may be generated by the on-chip Xtal oscillator or be derived from an external source. Any Xtal/clock frequency in the range 1.0MHz to 5.0MHz ($V_{DD} = 3.0V$) or 1.0MHz to 6.5MHz ($V_{DD} = 5.0V$) may be employed, depending upon the desired data rate.

A division ratio to facilitate data-rate setting is controlled by the logic level inputs on the ClkDivA/B pins. The formula below is employed to calculate the data rate:

$$\text{Data Rate} = \frac{\text{Xtal/Clock Frequency}}{\text{Division Ratio (ClkDivA/B)}}$$

10.2 Tx OUT Output Components R1 and C1

The RC network formed by R1 and C1 is required between the Tx OUT pin and the input to the modulator. This network, which can form part of any DC level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to the capacitor C1 should be positioned to give maximum attenuation of high-frequency noise into the modulator. The component values should be chosen so that the product of the resistance (Ohms) and the capacitance (Farads) is:

$$\text{For a BT of 0.3} \quad R1C1 = 0.34/\text{bit rate (bps)}$$

$$\text{For a BT of 0.5} \quad R1C1 = 0.22/\text{bit rate (bps)}$$

10.3 Doc1 and Doc2 Capacitor (C7 and C8) Values

Note the Data Sheet recommendations with regard to these two components:

C7 and C8 should both be 0.015 μ F for a data rate of 8kbps, and inversely proportional to the data rate for other data rates, e.g. 0.03 μ F at 4kbps, 3000pF at 40kbps.

10.4 Alternative Data Rate Tables

10.4.1 3.6864MHz

For a Xtal/Clock value of 3.6864MHz					
Data Rate (bps)	ClkDiv A	ClkDiv B	BT	R1 (k Ω)	C1 (pF)
7200	1	0	0.3	100	470
7200	1	0	0.5	62	470
14400	0	1	0.3	130	180
14400	0	1	0.5	130	120
28800	0	0	0.3	62	180
28800	0	0	0.5	62	120

Table 2: Data Rate for 3.6864MHz Xtal/Clock

10.4.2 4.096MHz

For a Xtal/Clock value of 4.096MHz					
Data Rate (bps)	ClkDiv A	ClkDiv B	BT	R1 (k Ω)	C1 (pF)
4000	1	1	0.3	120	680
4000	1	1	0.5	120	470
8000	1	0	0.3	91	470
8000	1	0	0.5	120	220
16000	0	1	0.3	47	470
16000	0	1	0.5	91	150
32000	0	0	0.3	47	220
32000	0	0	0.5	47	150

Table 3: Data Rate for 4.096MHz Xtal/Clock

10.4.3 4.9152MHz

For a Xtal/Clock value of 4.9152MHz					
Data Rate (bps)	ClkDiv A	ClkDiv B	BT	R1 (k Ω)	C1 (pF)
4800	1	1	0.3	100	680
4800	1	1	0.5	100	470
9600	1	0	0.3	91	390
9600	1	0	0.5	47	470
19200	0	1	0.3	100	180
19200	0	1	0.5	91	120
38400	0	0	0.3	47	180
38400	0	0	0.5	47	120

Table 4: Data Rate for 4.9152MHz Xtal/Clock

10.4.4 8.192MHz

For a Xtal/Clock value of 8.192MHz					
Data Rate (bps)	ClkDiv A	ClkDiv B	BT	R1 (k Ω)	C2 (pF)
64000	0	0	0.5	47	82

Table 5: Data Rate for 8.192MHz Xtal/Clock