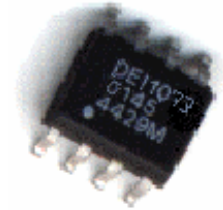**DEVICE**
ENGINEERING
INCORPORATED

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DEI1073, DEI1074, DEI1075 ARINC 429 LINE DRIVER WITH RATE SELECT AND TRI-STATE

FEATURES

- TTL/CMOS TO ARINC 429 Line Driver.
- Rate control input set Hi (100KBS) or Lo (12.5KBS) speed slew rates.
- Operates from ±9.5V to ±16.5V power supply.
- Drives full ARINC load.
- Output resistor options: 0, 10 or 37.5 Ohms.
- Tristate Outputs
- Thermally enhanced 8 lead SOIC package.
- Outputs Short Circuit Tolerant

GENERAL DESCRIPTION

The DEI1073 family of 8 pin BiCMOS integrated circuits are line drivers designed to directly drive the ARINC 429 avionics serial digital data bus. The device converts TTL/CMOS serial input data to the tri-level RZ bipolar differential modulation format of the ARINC bus. The outputs are tri-state capable. A TTL/CMOS control input selects the output slew rate for HI (100KBS) and LOW (12.5KBS) speed operation. No external timing capacitors are required.

The DEI1073 has internal 37.5 Ohm output resistors, the DEI1074 has 10 Ohm resistors, and the DEI1075 has none. The 10 and 0 Ohm options require external series resistors which are typically used to implement a transient voltage protection network.

Table 1 PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	HI/LO	**LOGIC INPUT.** Slew rate control. 1 = Hi speed. 0 = Low speed.
2	TTLIN0	**LOGIC INPUT.** Serial digital data input 0.
3	TTLIN1	**LOGIC INPUT.** Serial digital data input 1.
4	GND	**POWER INPUT.** Ground.
5	V-	**POWER INPUT.** −9.5 to −16.5 VDC
6	429OUTA	**429 OUTPUT.** ARINC 429 format serial digital data output A.
7	429OUTB	**429 OUTPUT.** ARINC 429 format serial digital data output B.
8	V+	**POWER INPUT.** +9.5 to +16.5 VDC.

Pinout:

HI/LO	1	8	V+
TTLIN0	2	7	429OUTB
TTLIN1	3	6	429OUTA
GND	4	5	V-
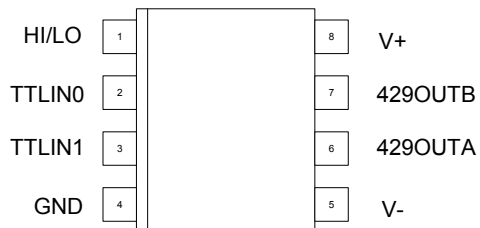
Note:
Heatsink pad is electrically Isolated.

FUNCTIONAL DESCRIPTION
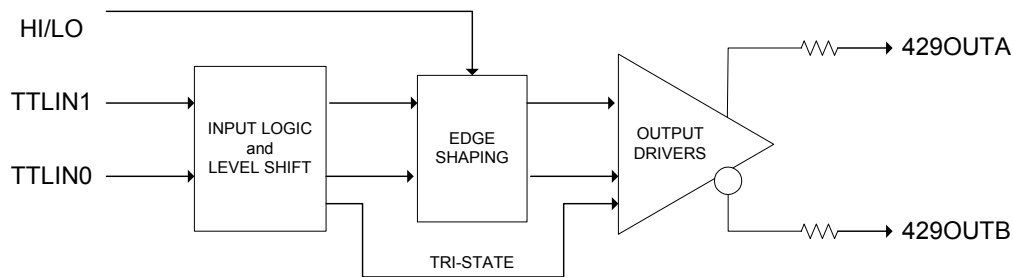
Block Diagram

Table 2 Speed Control Function Table

HI/LO	OUTPUT TRANSITION TIME
0	10uS (12.5 KBS data)
1	1.5uS (100KBS data)

Table 3 Transmit Data Function Table

TTLIN1	TTLIN0	429OUTA	429OUTB	NOTES
0	0	0V	0V	Null output
0	1	-5V	5V	Zero output
1	0	5V	-5V	One output
1	1	Hi-Z	Hi-Z	Tri-State output
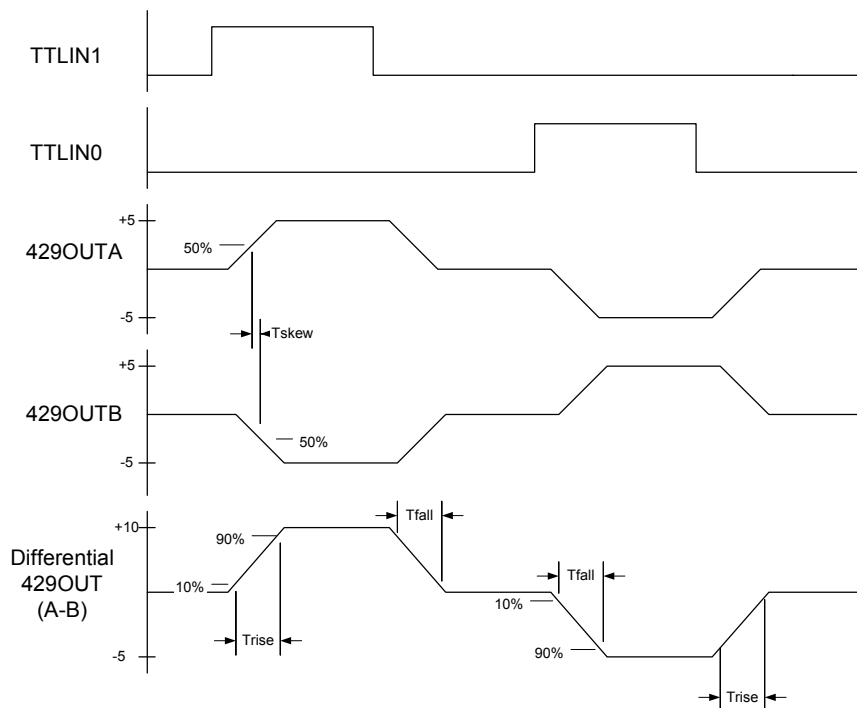
LINE DRIVER WAVEFORMS

ELECTRICAL DESCRIPTION

Table 4 Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS
Voltages referenced to Ground			
V+ Supply Voltage	-0.3	+20	V
V1- Supply Voltage	0.3	-20	V
V+, V- Supply Slew Rate		+/-100	V/uS
Storage Temperature	-65	+150	°C

Input Voltage
    TTLIN and HI/LO Inputs
    429OUT Outputs
	Gnd – 0.3
	'V-' – 0.3
		'V+' + 0.3
		'V+' + 0.3
			V
			V

Power Dissipation @ 85 °C: (> 10 Sec) 8 Lead EQ SOIC, thermal pad soldered to heat spreader land,		1.0	W

Junction Temperature:
    Tjmax, Plastic Packages (Limited by molding compound Tg)
    Tjmax, Ceramic Packages
		145
		160
			°C
			°C

ESD per JEDEC A114-A Human Body Model		2000	V
Lead Soldering Temperature (10 sec duration)		280	°C

Notes:
1. Stresses above absolute maximum ratings may cause permanent damage to the device.
2. The device is tolerant of one or both outputs shorted to Ground and of both outputs shorted together.

Table 5 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	V+ V-	9.5 to 16.5V -9.5 to –16.5V

Operating Temperature
    Plastic Package
    Ceramic Packages
	T_{OP}	-55 to +85 °C or
		-55 to +125 °C

Table 6 Electrical Characteristics

Conditions: Tcase = rated operating temperature -55/+85°C or -55/+125°C
V+/- = +/-9.5 to +/-16.5V Unless otherwise noted.

PARAMETER	TEST CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
LOGIC INPUTS						
Input Voltage, Logic 1		V_{IH}	2.0		V+	V
Input Voltage, Logic 0		V_{IL}	-0.3		0.8	V
Input Current, Logic 1	VIN = 5.0V	I_{IH}	0		100	uA
Input Current, Logic 0	VIN = 0.0V	I_{IL}	0		-100	uA
ARINC OUTPUTS						

ARINC Output Voltage (Differential)
    One
    Null
    Zero
	Differential Output Voltage = 429OUTA – 429OUTB. No Load.	V_{DIF1}
		$V_{DIFnull}$
		V_{DIF0}
			9.0
			-0.5
			-9.0
				10.0
				0
				-10.0
					11.0
					+0.5
					-11.0
						V
						V
						V

ARINC Output Voltage (Single Ended)
    Hi
    Null
    Lo
	Referenced to Ground No Load.	Vo_{HI}
		$Vo_{null,}$
		Vo_{LO}
			4.5
			-0.25
			-5.5
				5.0
				0
				-5.0
					5.5
					+0.25
					-4.5
						V
						V
						V

Output Tristate Current	-5V to +5V	I_z	-10		+10	uA
ARINC Output Short Circuit Current	Outputs shorted to Ground.	Isc_{LO} Isc_{HI}		130 -130		mA mA

Output Resistance:
    DEI1073
    DEI1074
    DEI1075
	Room Temperature	Rout37
		Rout10
		Rout0
				37.5
				10
				0
						Ohms
						Ohms
						Ohms

Output Slew Rate, Hi Speed Lo to Hi and Hi to Lo transitions	HI/LO = 1 No Load 10% to 90% voltage amplitude of differential output.	T_{HI}	1.0		2.0	uS
Output Slew Rate, Lo Speed Lo to Hi and Hi to Lo transitions	HI/LO = 0 No Load Measured from 10% to 90% voltage amplitude of differential output.	T_{LO}	5		15	uS
Output skew time between A and B outputs.	HI/LO = 1 Measured at 50% voltage amplitude of both outputs	Tskew			200	nS
SUPPLY CURRENT						

Quiescent Operating Supply Current:
    IV+
    IV-
	V+ =15V, V- = -15V HI/LO = 0 or 1 TTLIN0=TTLIN1= 0V No Load	I_{V+}
		I_{V-}
			-
			-14.0
				6.0
				-6.0
					14.0
					-
						mA
						mA

DESIGN CONSIDERATIONS
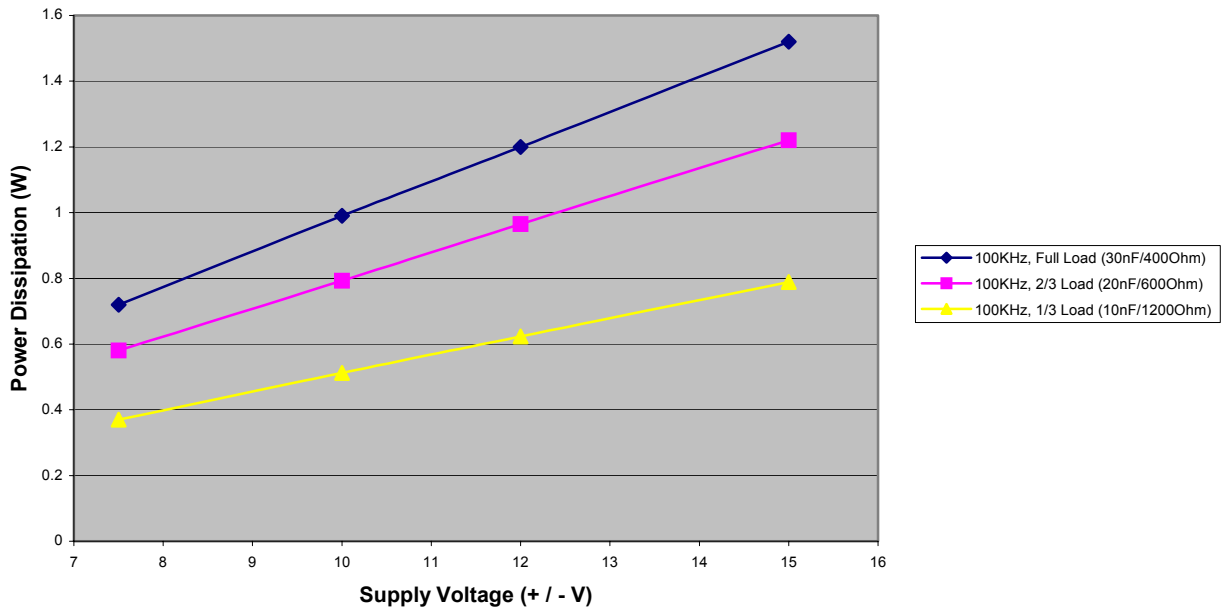
Transient Voltage Protection

External transient voltage suppressing devices are required to protect the device from stress such as that defined by DO160D Section 22, Lightning Induced Transient Susceptibility. The output stage of the driver includes intrinsic clamp diodes to the V+ and V- power rails. Consider using the 0 Ohm output option to allow use of an external 36 Ohm current limiting resistor and transient voltage suppressor. Transients at the device must be limited to less than one diode drop beyond the power rails to prevent excessive current to the device.

Thermal Management

Device power dissipation varies greatly as a function of data rate, load capacitance, data duty cycle, and supply voltage. Proper thermal management is important in designs operating at the HI speed data rate (100KBS) with high capacitive loads and high data duty cycles. Dissipation may be estimated from the graph below which shows the approximate power dissipation for various loads and supply voltages. It is calculated for 100% data duty cycle at 100KBS with no word gap null times and must be reduced by the appropriate data duty cycle. Adjust for the application data duty cycle using a factor of (total bits transmitted in 10 sec period / 1,000,000) = (32 x total ARINC words transmitted in 10 sec period / 1,000,000).
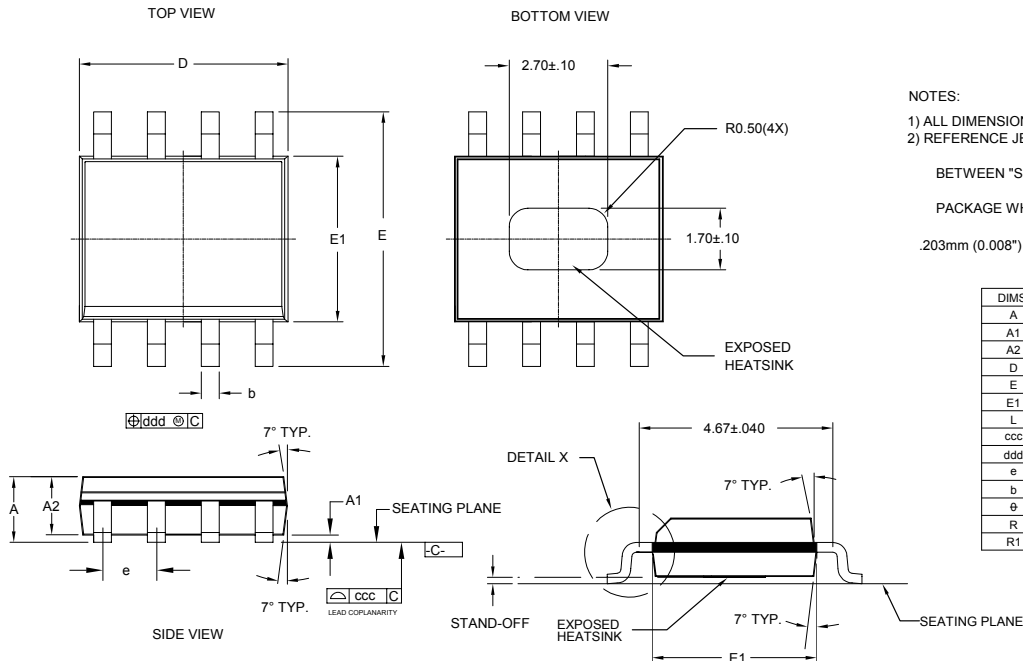
Heat transfer from the IC package should be maximized. Use maximum trace width on all power and signal connections at the IC. The exposed heat sink pad of the SOIC package should be soldered to a heat spreader land on the PCB. The pad is electrically isolated. Maximize land size by extending beyond the IC outline if possible. Place vias on the signal/power traces close to the IC and on the heat spreader land to maximize heat flow to the internal power planes.

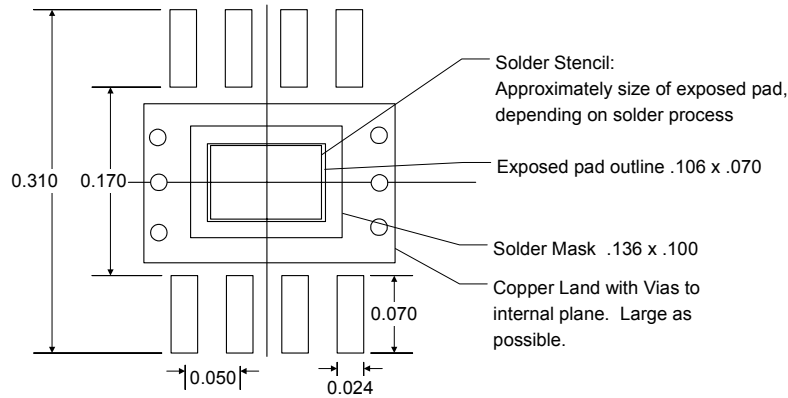**429 DRIVER DEVICE POWER DISSIPATION (100kbs, 100% DC)**

Legend:
- 100KHz, Full Load (30nF/400Ohm)
- 100KHz, 2/3 Load (20nF/600Ohm)
- 100KHz, 1/3 Load (10nF/1200Ohm)

X-axis: Supply Voltage (+ / - V)
Y-axis: Power Dissipation (W)

PACKAGE DESCRIPTION

8 Lead EDQUAD SOIC

TOP VIEW

BOTTOM VIEW

2.70±.10

R0.50(4X)

1.70±.10

EXPOSED HEATSINK

NOTES:
1) ALL DIMENSIONS IN MILLIMETER.
2) REFERENCE JEDEC SPEC: MS-012

BETWEEN "SEATING PLANE" AND THE

PACKAGE WHICH EVER IS LOWER.

.203mm (0.008") THICK.

7° TYP.

DETAIL X

4.67±.040

7° TYP.

SEATING PLANE

SEATING PLANE

A2

A1

SEATING PLANE

-C-

7° TYP.

ccc C
LEAD COPLANARITY

STAND-OFF

EXPOSED HEATSINK

7° TYP.

E1

SIDE VIEW

ddd C

DIMS.	TOLS.	N	8
A	MAX.		1.60
A1	±.05		0.05
A2	±.10		1.40
D	±.10		4.90
E	±.20		6.00
E1	±.10		3.90
L	±.15		0.60
ccc	MAX.		0.10
ddd	MAX.		0.10
e	BASIC		1.27
b	±.05		0.43
θ			0° ~ 8D
R	MAX.		0.20
R1	TYP.		0.13

0.310   0.170

0.070

0.050   0.024

Solder Stencil:
Approximately size of exposed pad, depending on solder process

Exposed pad outline .106 x .070

Solder Mask .136 x .100

Copper Land with Vias to internal plane. Large as possible.
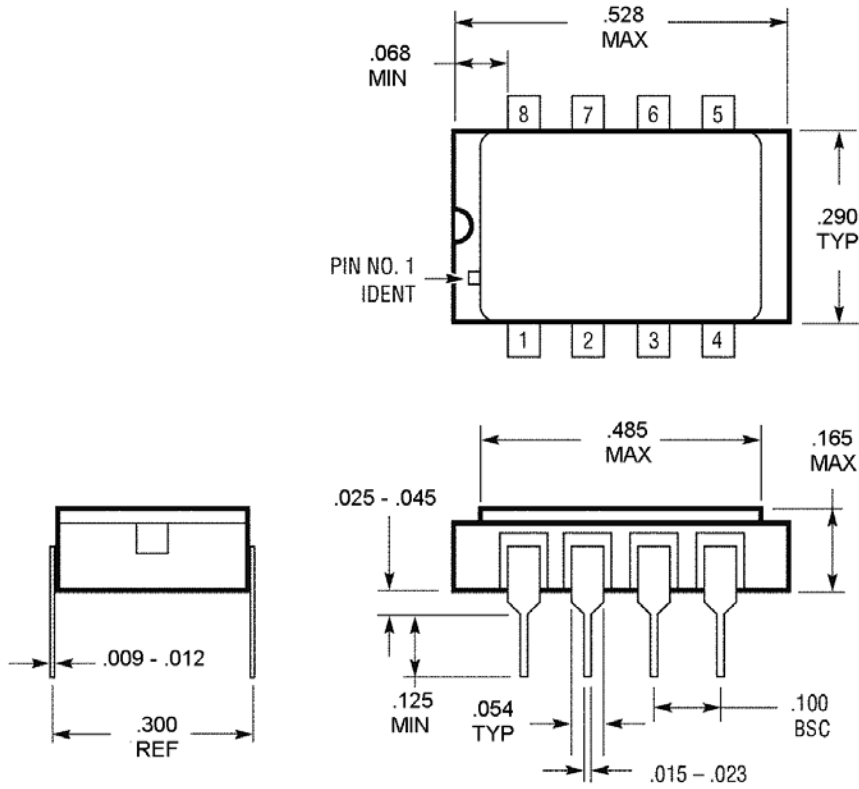
Suggested Land Pattern (Dimensions in inches)

Table 7 8 Lead EDQUAD SOIC Characteristics

SYMBOL	DESCRIPTION	VALUE	UNITS
$Theta_{ja}$	Junction to Ambient. 4 layer board with 2 internal power planes. Exposed pad soldered to PCB heat spreader land.	59	°C/W
MSL	JEDEC Moisture Sensitivity Level Peak Body Temperature	2 235	- °C

8 Lead Ceramic Sidebrazed DIP

SYMBOL	DESCRIPTION	VALUE	UNITS
Theta$_{jc}$	Junction to Case	55	°C/W
Theta$_{ja}$	Junction to Ambient.	125	°C/W

Table 3 Process Flow

PROCESS STEP	STANDARD	BURN-IN
PRE-BURN-IN Electrical Test	N/A	YES
BURN IN (1)	N/A	96hrs @ +125 °C
FINAL ELECTRICAL TEST, Room Temperature	100%	100%
FINAL ELECTRICAL TEST, High Temperature	100% @ +85 or +125°C	100% @ +85 or +125°C
FINAL ELECTRICAL TEST, Low Temperature	0.65% AQL @ -55°C	0.65% AQL @ -55°C

NOTES:
1. Burn-in conditions: 125°C, 96 hrs, V+/V- = +/-15.0V Inputs = 0V, Outputs open.

ORDERING INFORMATION

Table 8 Ordering Information

Part Number	Marking	Package	Output Resistor	Burn-In	Temperature
DEI1073-SES	DEI1073 / SES	8L EQ SOIC	37	No	-55 / +85 ºC
DEI1074-SES	DEI1074 / SES	8L EQ SOIC	10	No	-55 / +85 ºC
DEI1075-SES	DEI1075 / SES	8L EQ SOIC	0	No	-55 / +85 ºC
DEI1073-SMB	DEI1073 / SMB	8L EQ SOIC	37	Yes	-55 / +125 ºC
DEI1074-SMB	DEI1074 / SMB	8L EQ SOIC	10	Yes	-55 / +125 ºC
DEI1075-SMB	DEI1075 / SMB	8L EQ SOIC	0	Yes	-55 / +125 ºC
DEI1073-DMS	DEI1073 / DMS	8L SB DIP	37	No	-55 / +125 ºC
DEI1074-DMS	DEI1074 / DMS	8L SB DIP	10	No	-55 / +125 ºC
DEI1075-DMS	DEI1075 / DMS	8L SB DIP	0	No	-55 / +125 ºC
DEI1073-DMB	DEI1073 / DMB	8L SB DIP	37	Yes	-55 / +125 ºC
DEI1074-DMB	DEI1074 / DMB	8L SB DIP	10	Yes	-55 / +125 ºC
DEI1075-DMB	DEI1075 / DMB	8L SB DIP	0	Yes	-55 / +125 ºC
DEI1073-SMS	DEI1073 / SMS	8L EQ SOIC	37	No	-55 / +125 ºC
DEI1074-SMS	DEI1074 / SMS	8L EQ SOIC	10	No	-55 / +125 ºC
DEI1075-SMS	DEI1075 / SMS	8L EQ SOIC	0	No	-55 / +125 ºC