Features

- **Full Field Image Sensor 3500 x 2300 Pixels**
- **Pixel 10 µm x 10 µm Photo-MOS with 100% Aperture**
- **Image Zone: 35 mm x 23 mm**
- **Frame Readout Through One, Two or Four Outputs**
- **Built-in Region of Interest Structure**
- **Data Rates Up to 4 x 25 MHz (Compatibility with 10 Frames/Seconds)**
- **High Dynamic Range (Up to 3000), at Room Temperature and at 25 MHz Frequency**
- **Very Low Dark Current (MPP Mode)**
- **Optimized Resolution and Responsivity in the 400 - 1100 nm Spectrum**
- **Additional Full-frame Operating Modes**
  - **2627 x 2300 pixels of 10 µm x 10 µm (3 zones)**
  - **Binning 4 x 4 Pixels (Format 875 x 575 Pixels of 40 µm x 40 µm)**
  - **Binning 2 x 2 Pixels (Format 1750 x 1150 Pixels of 20 µm x 20 µm)**
- **On-request Frame Transfer Architecture**
  - **1750 Active Lines, One Memory Zone with Frame Readout Through One or Two Outputs**
  - **1750 Active Lines, Two Memories Zones with Frame Readout Through Two or Four Outputs**
- **Flexibility and Performance Make Device Suitable for Digital Photography, Graphic Arts, Medical and Industrial Applications**

Description

Atmel's AT71200M is a full-frame sensor based on charge-coupled device (CCD) technology. It can be used in a wide range of applications thanks to operating mode flexibility, very high definition and high dynamic range.

The nominal photosensitive area is made up of 2300 x 3500 useful pixels and is split into four independent zones that are driven separately by four independant four-phase clocksets. Thus the sensor can be used in up to 15 main modes.

The large format and high definition make the device suitable for any application requiring precision and accuracy.

The high sensitivity of the 10 µm x 10 µm pixels with 100% aperture provides a large bandwidth of response with up to 1100 nm wavelength.

Two serial registers and four independent output amplifiers offer a high-frequency functionality of up to 17 frames per second and a 12-bit dynamic range.

8M-pixel Image Sensor

AT71200M

Rev. 2134A–IMAGE–02/03

Pinout

Figure 1. AT71200M Pinout

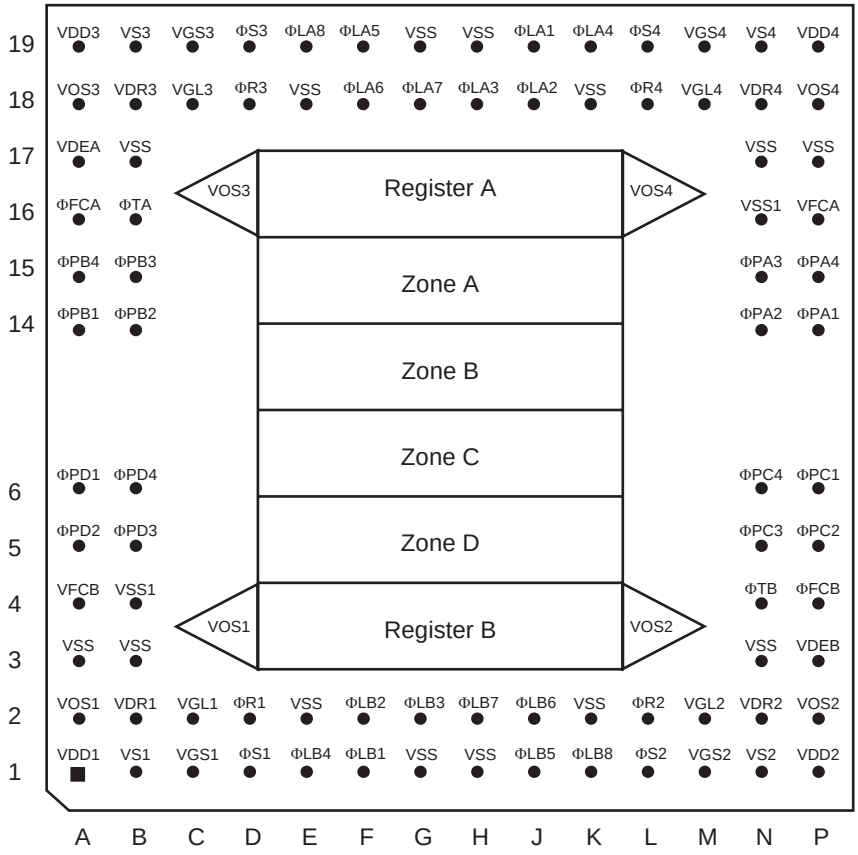
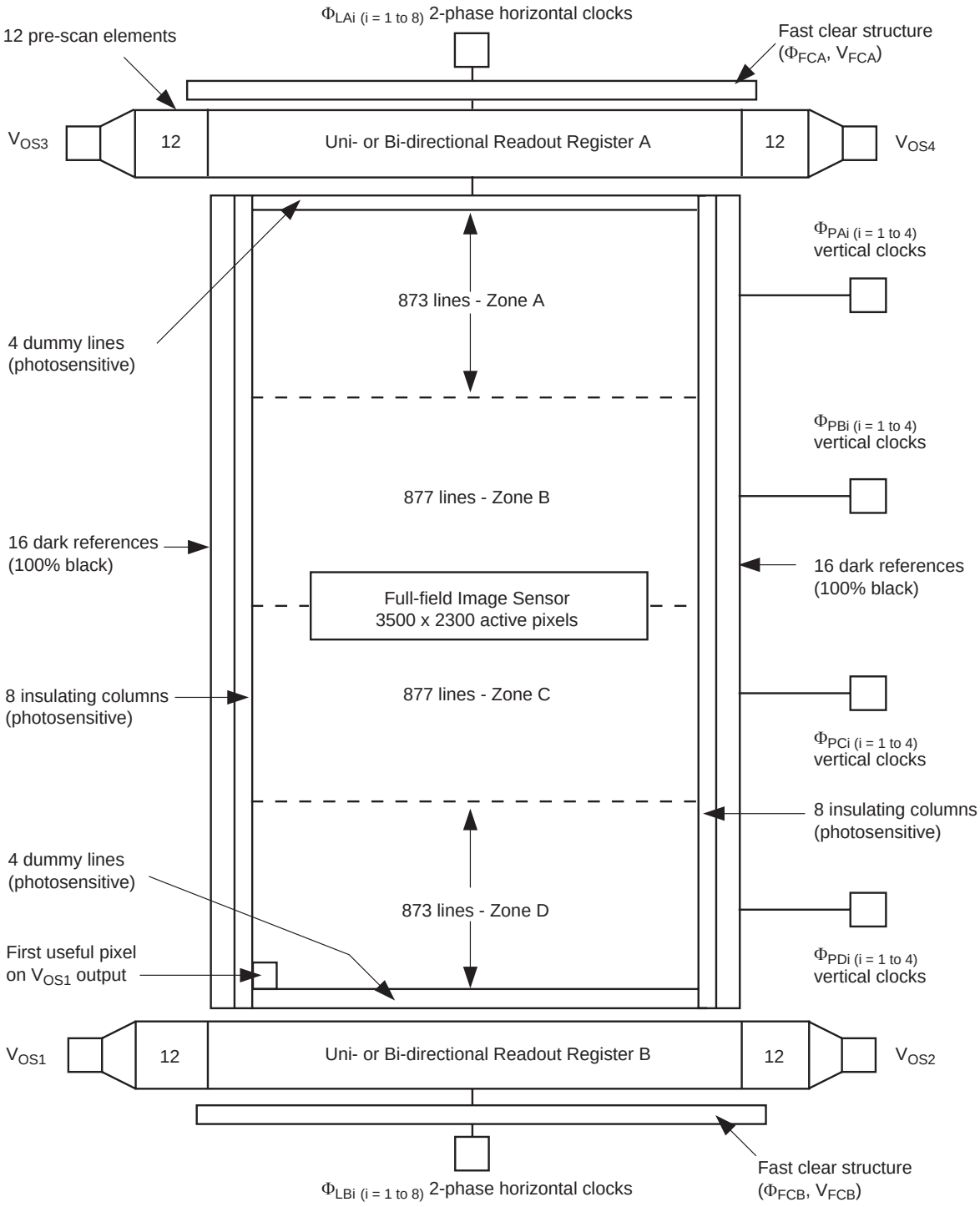


Table 1. AT71200M Pinout

Signal Name	Pin Number	Function
ΦLB[1:8]	F1, F2, G2, E1, J1, J2, H2, K1	B readout register clocks
ΦLA[1:8]	J19, J18, H18, K19, F19, F18, G18, E19	A readout register clocks
ΦS[1:4]	D1, L1, D19, L19	Summing clocks of the outputs 1, 2, 3 and 4
VGL[1:4]	C2, M2, C18, M18	Readout gate bias of the outputs 1, 2, 3 and 4
VGS[1:4]	C1, M1, C19, M19	Output gate bias of the outputs 1, 2, 3 and 4
VOS[1:4]	A2, P2, A18, P18	Output video signals 1, 2, 3 and 4
VDD[1:4]	A1, P1, A19, P19	Output amplifier drain supplies of the outputs 1, 2, 3 and 4
VS[1:4]	B1, N1, B19, N19	Output amplifier source biases of the outputs 1, 2, 3 and 4
ΦR[1:4]	D2, L2, D18, L18	Reset clocks of the outputs 1, 2, 3 and 4
VDR[1:4]	B2, N2, B18, N18	Reset bias of the outputs 1, 2, 3 and 4
ΦPA[1:4]	P14, N14, N15, P15	A image zone clocks
ΦPB[1:4]	A14, B14, B15, A15	B image zone clocks
ΦPC[1:4]	P6, P5, N5, N6	C image zone clocks
ΦPD[1:4]	A6, A5, B5, B6	D image zone clocks
ΦTA, ΦTB	B16, N4	Transfer gates from the image zone to the readout registers A and B respectively
VDEA, VDEB	A17, P3	Shield drains
VFCA, VFCB	P16, A4	Region of interest drains
ΦFCA, ΦFCB	A16, P4	Region of interest clocks
VSS	A3, B3, B4, E2, G1, H1, K2, M3, B17, E18, G19, H19, K18, N16, N17, P17	Substrate bias

Block Diagram

Figure 2. AT71200M Block Diagram – Top View



Architectural Overview

General Parameters

Table 2. General Parameters

Parameters	Value
Pixel size	10 µm x 10 µm
Number of useful pixels on one line	2300
Number of useful lines	3500
Number of readout register	2
Number of outputs	4(1)
MPP technology	yes
Region of interest structures on readout registers	yes
Built-in antiblooming	no
Pixel mode	4-phase
Readout register mode	2-phase

Note: 1. The design allows the full frame to be read through one, two or four outputs.

Vertical Characteristics – Top to Bottom

AT71200M is made up of four zones, A, B, C and D. The configuration of each zone is shown in Table 3.

Table 3. Vertical Characteristics

Zone	Configuration
A	4 dummy photosensitive lines
	873 active lines, 100% photosensitive
B	877 active lines, 100% photosensitive
C	877 active lines, 100% photosensitive
D	873 active lines, 100% photosensitive
	4 dummy photosensitive lines

Horizontal Characteristics

Table 4 gives information on the characteristics seen by one output (V_{OS1}, V_{OS2}, V_{OS3} or V_{OS4}) in different readout modes.

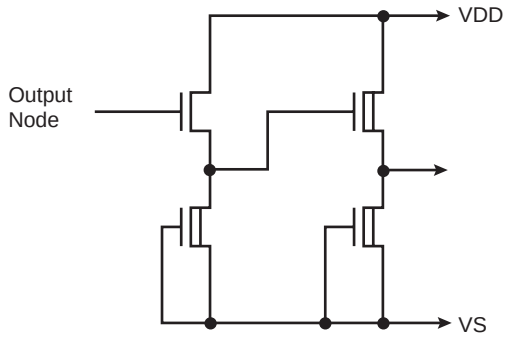
Table 4. Horizontal Characteristics and Readout Modes

	Readout Mode	
Characteristic	**One Output**	**Two Outputs on Same Register**
Pre-scan elements	12	12
Dark references	16	16
Insulating elements	8	8
Useful pixels	2300	1150

Output Amplifiers

The charge packets are clocked to the output nodes and the charges are converted to voltages. The potential at the output node is read through two stage source follower amplifiers. Refer to Figure 3.

Figure 3. On-chip Output Amplifier Structure



Absolute Maximum Ratings*

Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	-40°C to +85°C
Thermal Cycling	15°C/mn

*NOTICE: Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Electrical limits of applied signals are given in Table 5.

Shorting the video output to V_{SS} or V_{DD}, even temporarily, can permanently damage the output amplifier.

Due to MPP mode or negative voltages, image zone gates and region of interest gates do not include ESD protection. To avoid degradation, the devices (including pins and package) should be handled with a grounded bracelet and stored on conductive layer used for shipment.

Table 5. Maximum Applied Voltages(1)

Signal Name	Parameter	Min	Max	Unit
ΦLA[1:8]	Readout A Register Clocks	-0.3	+15	V
ΦLB[1:8]	Readout B Register Clocks	-0.3	+15	V
ΦS[1:4]	Summing Gate	-0.3	+15	V
VGL[1:4]	Readout Gate	-0.3	+15	V
VGS[1:4]	Output Gate	-0.3	+15	V
VOS[1:4]	Output Video Signal	-0.3	+15	V
VDD[1:4]	Amplifier Drain Supply	-0.3	+15	V
VS[1:4]	Source Bias	-0.3	+15	V
ΦR[1:4]	Reset Gate	-0.3	+15	V
VDR[1:4]	Reset Bias	-0.3	+15	V
ΦPA[1:4]	Image Zone A Clocks	-15 and ΦPA[other] - 20	+15 and ΦPA[other] + 20	V
ΦPB[1:4]	Image Zone B Clocks	-15 and ΦPB[other] - 20	+15 andΦPB[other] + 20	V
ΦPC[1:4]	Image Zone C Clocks	-15 and ΦPC[other] - 20	+15 and ΦPC[other] + 20	V
ΦPD[1:4]	Image Zone D Clocks	-15 and ΦPD[other] - 20	+15 and ΦPD[other]+20	V
ΦTA	Transfer Gates Zone A	ΦLA - 15 and ΦPA[4] - 15	+15 and ΦPA[4] + 15	V
ΦTB	Transfer Gates Zone B	ΦLB - 15 and ΦPD[4] - 15	+15 and ΦPD[4] +15	V
VDEA, VDEB	Shield Drains	-0.3	+15	V
VFCA, VFCB	Region Of Interest Drains	-0.3	+15	V
ΦFCA	Region Of Interest GatesZone A	ΦLA[1:8] - 15	+15	V
ΦFCB	Region Of Interest Gates Zone B	ΦLB[1:8] - 15	+15	V
VSS	Substrate Bias		0	V

Note: 1. If not specified, all voltages are applied with respect to the substrate VSS.

DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Typical Currents
V_S (1)	Source bias	0	0	1	V	<12 mA
V_{DD} (1)	Amplifier drain supply	14.5	15	15.5	V	<12 mA
V_{SS}	Substrate bias	0	0		V	–
V_{GS}	Output gate	7	7.5	8	V	<1 µA
V_{DR}	Reset diode	13.5	14	14.5	V	<5 µA
V_{GL}	Readout gate	3	3.5	4	V	<1 µA
	Readout gate - Binning mode	11	12	13	V	<1 µA
V_{DE}	Shield drain	3	5	6	V	<1 µA
VFC	Region of interest drains	12.5	13	13.5	V	<5 µA

Note: 1. If corresponds to inactive output, may be stated to [3V, 7V] in order to reduce power consumption.

Drive Clock Characteristics

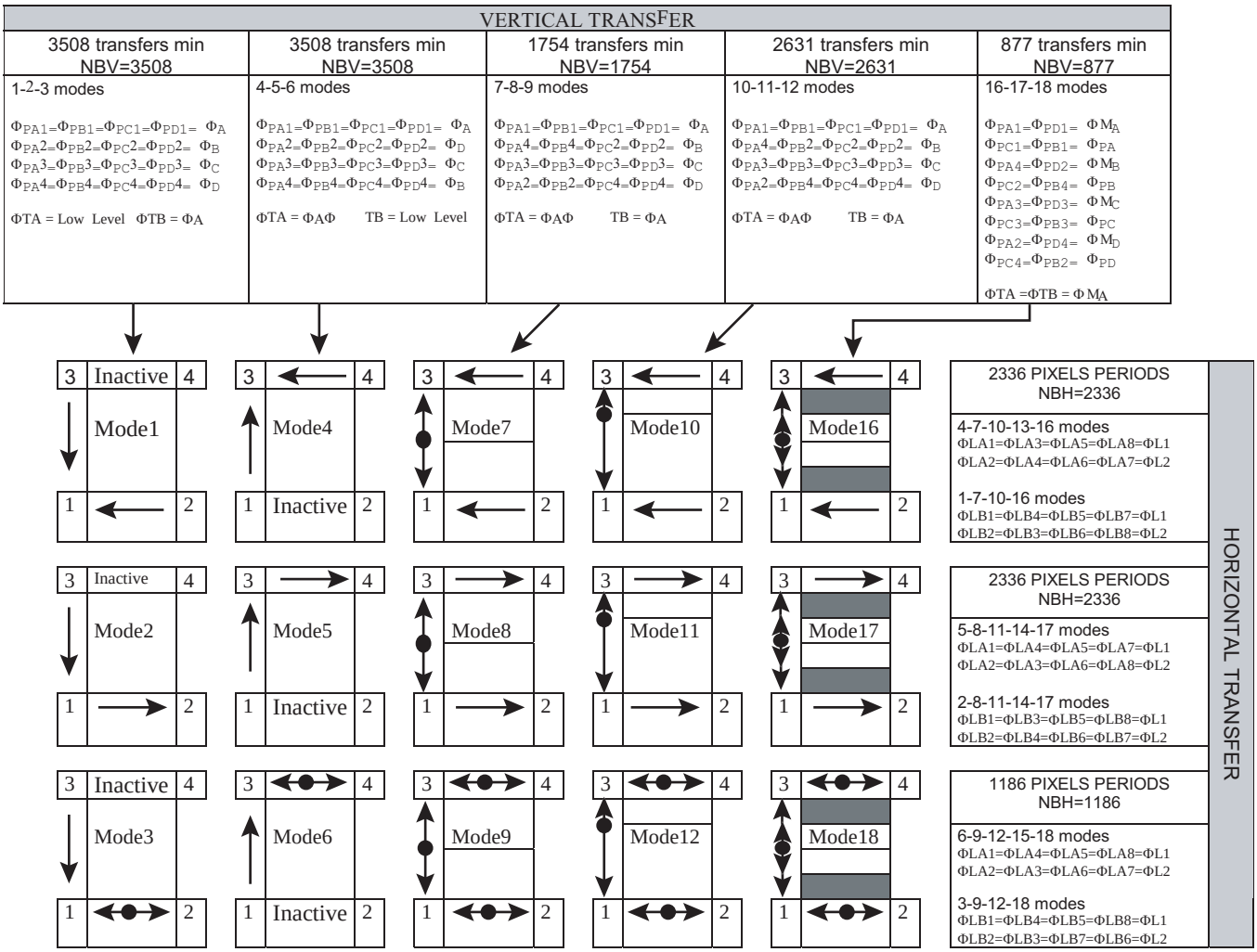
Symbol	Parameter	State	Minimum	Typical	Maximum	Unit	Remarks
Φ_{Pij}(1)(2)	Image Zone Clocks	Low	-10	-9	-8	V	For each A, B, C and D zone, the typical capacitances to drive are C_{Pij} approx. 12 nF
		High	+2.5	+3	+3.5	V	
Φ_{Lmn}(3)(4)	Readout Register Clocks	Low	0	0	+0.5	V	After the eight clocks have been grouped together to form the two clocks Φ_{L1} and Φ_{L2}, the typical capacitances to drive for each register A or B are $C_{\Phi L1}$ approx. 310 pF and $C_{\Phi L2}$ approx. 310 pF
		High	+7.5	+8	+9	V	
Φ_{Sj}(2)	Summing Gates	Low	0	0	+0.5	V	For each Φ_{Sj}, the typical capacitances to drive is $C_{\Phi Sj}$ approx. 40 pF
		High	+7.5	+8	+9	V	
Φ_{Rj}(2)	Reset Gates	Low	+1	+2	+3	V	For each Φ_{Rj}, the typical capacitance to drive is $C_{\Phi Rj}$ approx. 40 pF
		High	+8	+9	+10	V	
Φ_{Tm}(3)	Transfer Gates	Low	-6	-5	-4	V	For each Φ_{Tm}, the typical capacitance to drive is $C_{\Phi Tm}$ approx. 150 pF
		High	+2.5	+3	+3.5	V	
Φ_{FCm}(3)	Region of Interest Gates	FC inactive	-3.5	-2.5	-2	V	For each Φ_{FCm}, the typical capacitance to drive is $C_{\Phi FCm}$ approx. 50 pF
		Low	0	0	+0.5	V	
		High	+3.5	+4	+4.5	V	

Notes:
1. i = A, B, C or D
2. j = 1, 2, 3 or 4
3. m = A or B
4. n = 1, 2, 3, 4, 5, 6, 7 or 8

Operating Modes

For the required readout mode, the vertical and horizontal clocks must be tied together externally as shown in Figure 4.

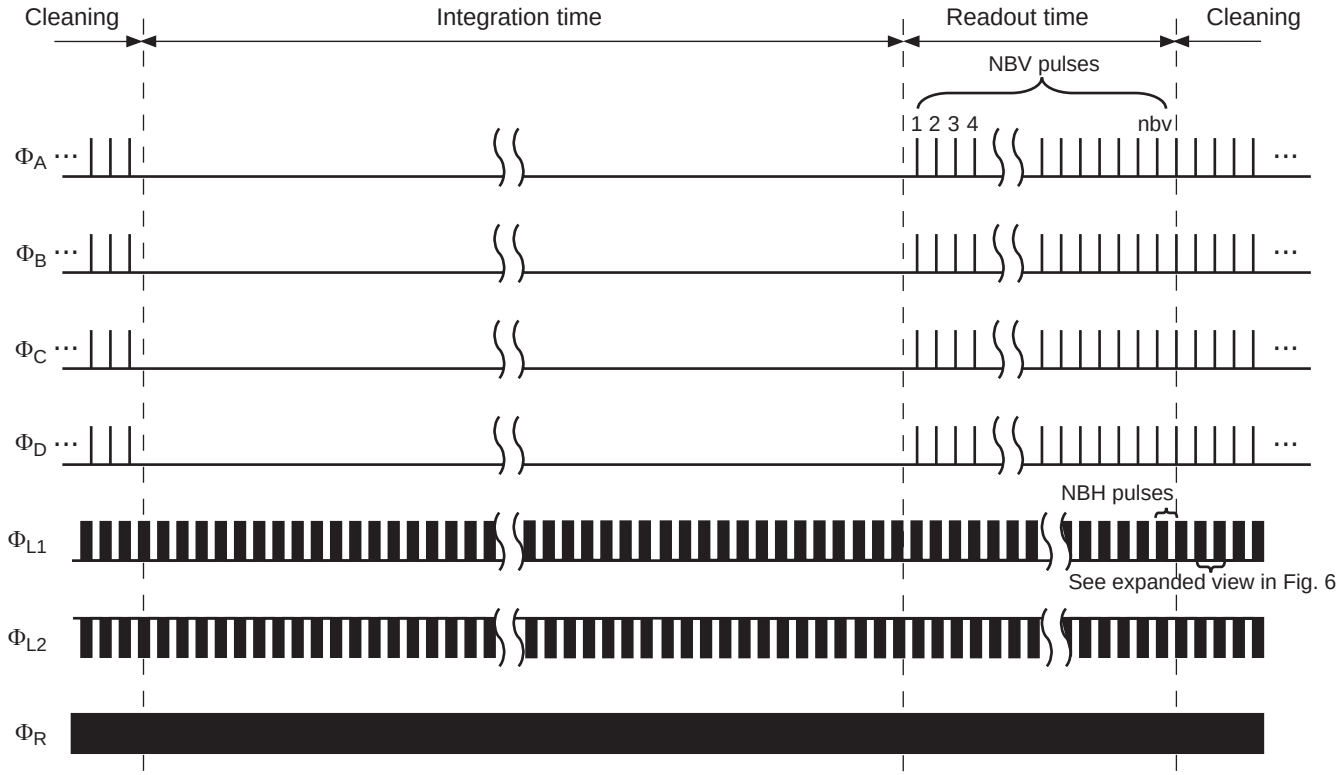
Figure 4. Operating Modes



Note: Symbols ΦA, ΦB, ΦC and ΦD correspond to the clocks described in the full-frame mode timing diagrams and the symbols ΦMA, ΦMB, ΦMC and ΦMD correspond to the clocks described in the frame transfer mode timing diagrams. Abbreviations NBV and NBH correspond respectively to the vertical and horizontal number of transfers.
The unused horizontal clocks (ΦL, ΦR, ΦS) must be stated to higher level of ΦL.

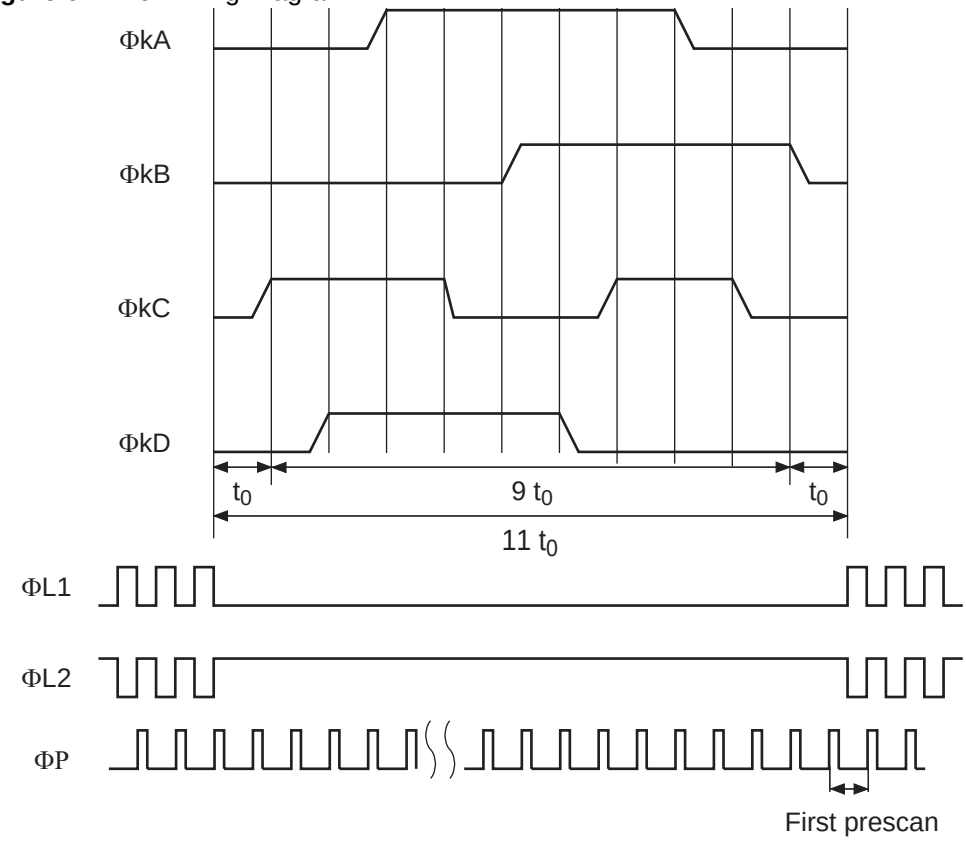
Timing Diagrams

Figure 5. Full-frame Mode Timing Diagram



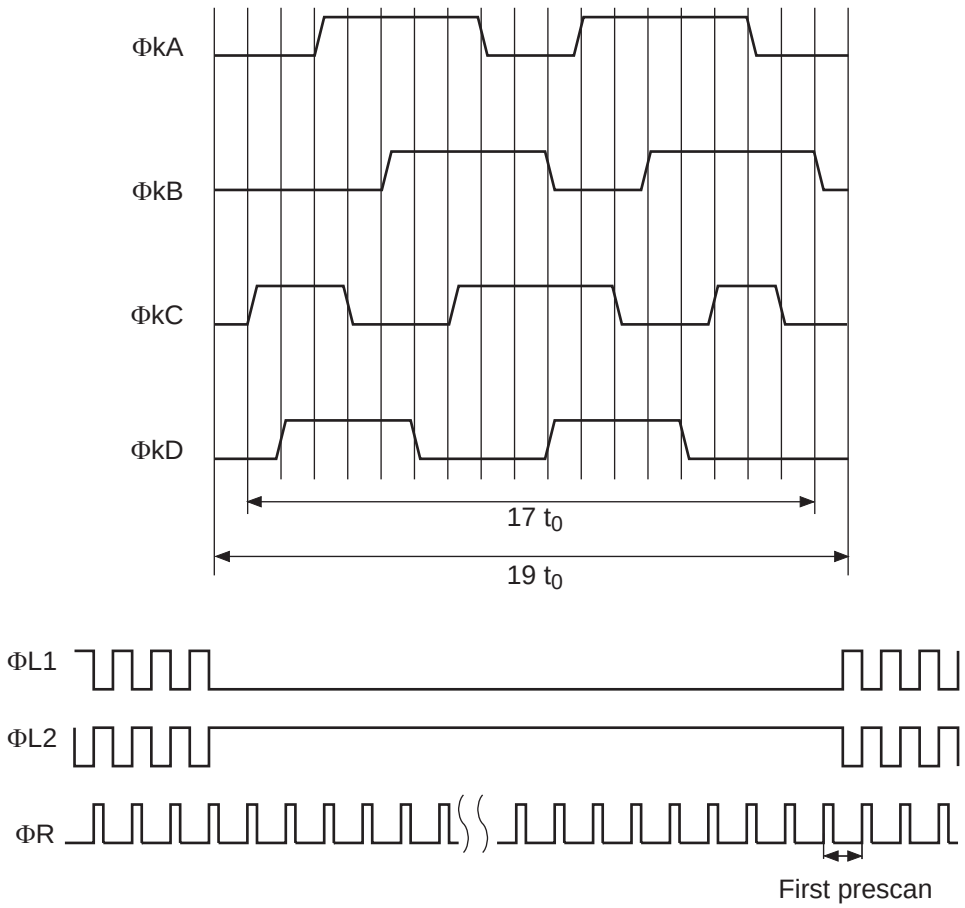
Note: ΦA, ΦB, ΦC, ΦD, ΦL1 and ΦL2 (command phases) and NBV, NBH (number of vertical transfer and number of horizontal transfer respectively) are defined in Figure 4.

Figure 6. Line Timing Diagram



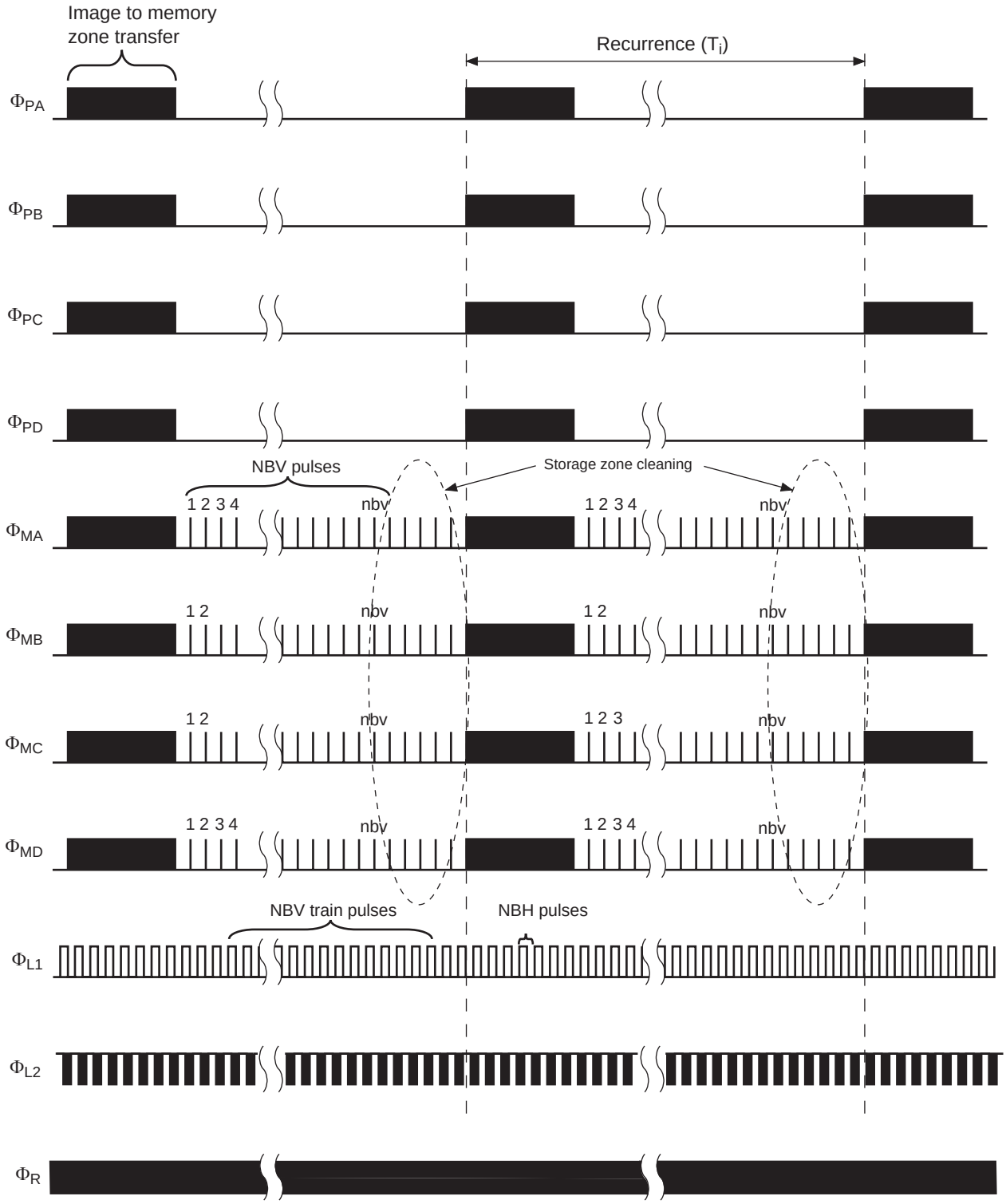
Note: k = P, M
t_o = see Table 9

Figure 7. Two Lines Summation Timing Diagram



Note: k = P, M

Figure 8. Frame Transfer Mode Timing Diagram (Without Summation)



Note: ΦA, ΦB, ΦC, ΦD, ΦL1 and ΦL2 (command phases) and NBV, NBH (number of vertical transfer and number of horizontal transfer respectively) are defined in Figure 4.

Figure 9. ΦP and ΦM Phases During Fast Image Zone to Memory Zone Transfer – Timing Diagram

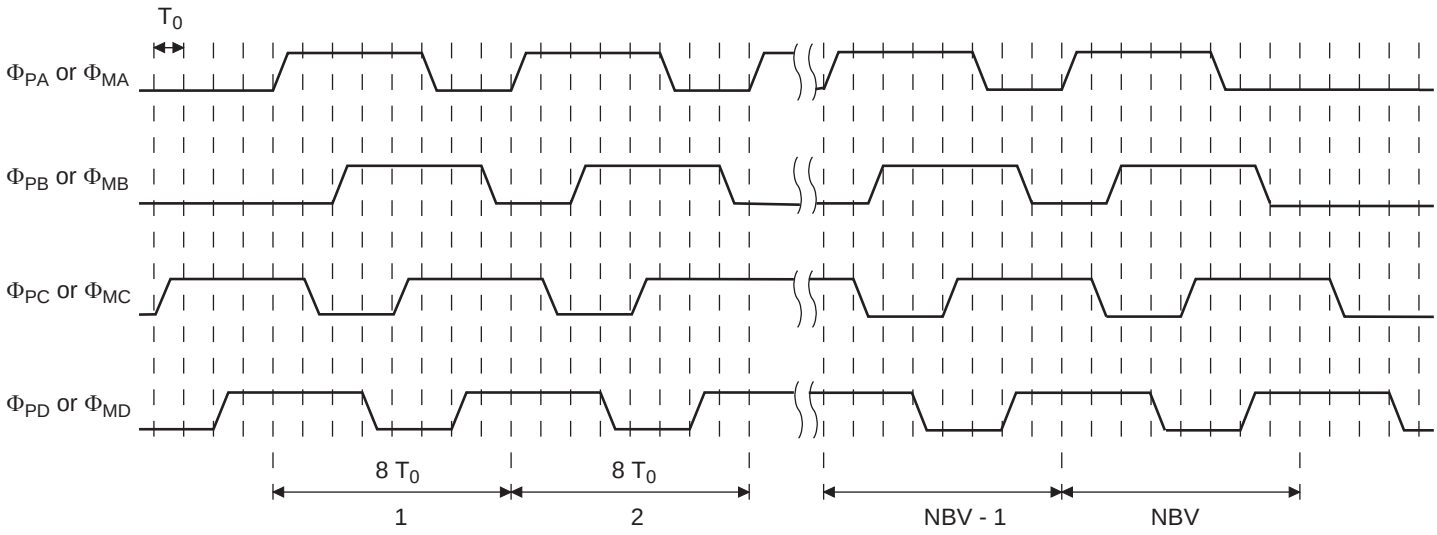


Figure 10. Readout Register Transfer in Summation Mode – Timing Diagram

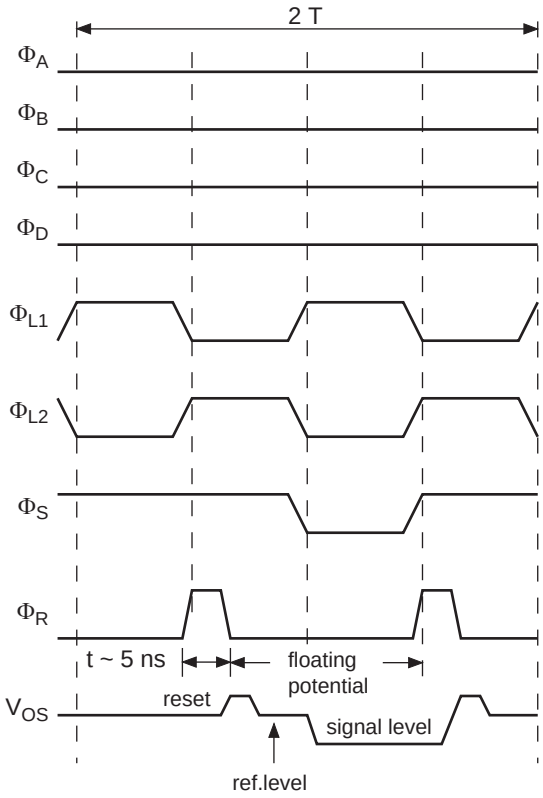
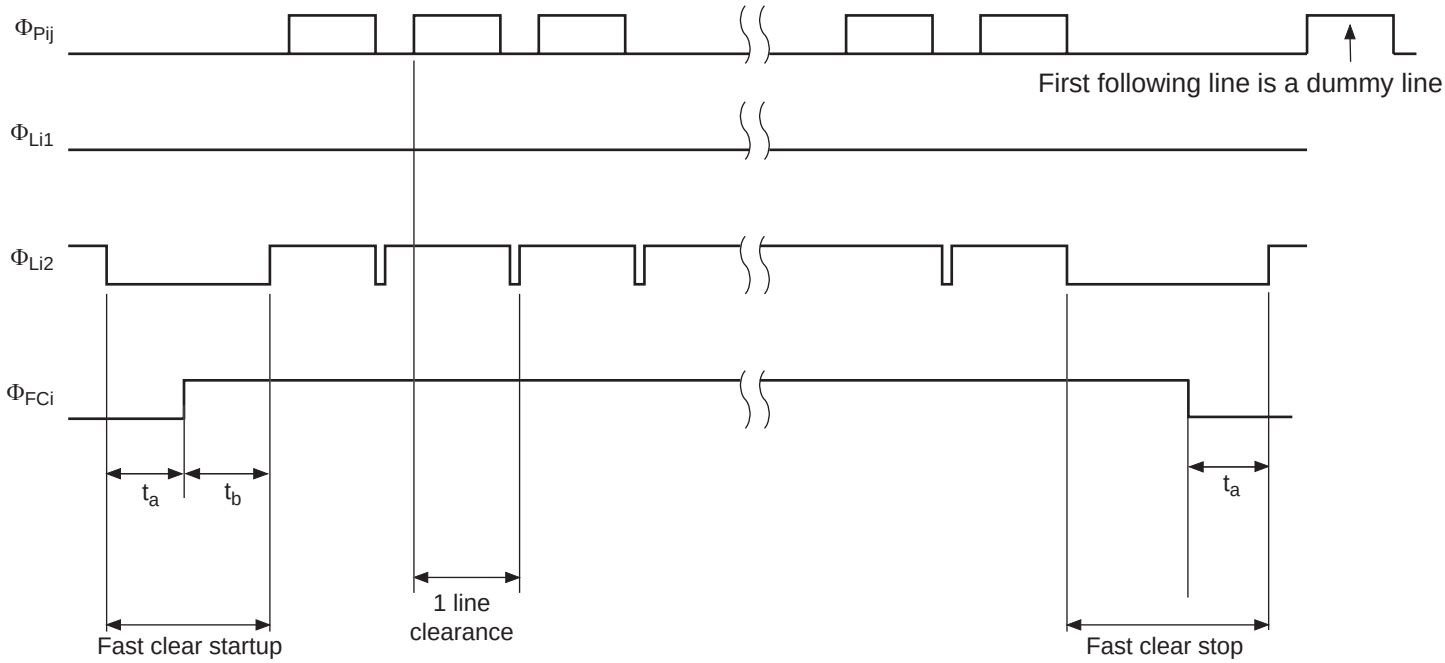


Figure 11. Region of Interest Operating Mode



Note: Typical values $t_a \geq 150$ ns, $t_b \geq 150$ ns

Table 6. Typical TR and TF (Time Rise, Time Fall) for Phases

Phase	Time
Φ_{P1}	500 ns
Φ_{P2}	500 ns
Φ_{P3}	500 ns
Φ_{P4}	500 ns
Φ_{FC}	50 ns
V_{FC}	50 ns
Φ_{L1}	10 ns
Φ_{L2}	10 ns
Φ_{S}	10 ns
Φ_{R}	4 ns

Frame Rate Characteristics

Table 7. Frame Rate Characteristics

	One Output (Modes 1, 2, 3, 4)	Two Outputs (Modes 13, 14)	Four Outputs (Mode 15)
Without binning	Typical 2.8 fps	Typical 5.1 fps	Typical 10.2 fps
With 2 x 2 binning	Typical 5.1 fps	Typical 8.7 fps	Typical 17.3 fps

Note: Table 7 gives typical values for full-frame mode where:

- Horizontal pixel frequency = 25 MHz
- Vertical transfer time $T_V = 11xt_0 = 10$ µs
  (delay times before and after line transfer $t_1 = t_2 = t_0$)
- Integration time = 0 s

Table 8. Electrical and Miscellaneous Characteristics

Symbol	Parameters	Minimum	Typical	Maximum	Unit
V_{REF}	DC output level		10		V
Z_{OUT}	Output impedance		230		Ohms
I_{DD} (1)	Output amplifier supply current		10	15	mA
C_{VF}	Charge-to-voltage conversion factor – Standard mode	7.3	7.6	8.0	µV/e-
	Charge-to-voltage conversion factor – Binning mode	4.8	5.1	5.4	
T_V	Vertical transfer time	6	10	–	µs
FH	Maximum readout pixel frequency	25	–	–	MHz

Note: 1. For each output.

Electrooptical Data

Table 9. Performance Data(1)

Symbol	Parameters	Minimum	Typical	Maximum	Unit
V_{SAT}	Pixel saturation output voltage	500	600	700	mV
	Saturation output voltage in binning modes(2)	1320	1550	1780	mV
R	Responsivity	4.3	4.9	5.5	V/(µJ/cm^2)
PRNU	Photo response non uniformity, σ		1	3	% |VOS|
DSI1	Dark signal image zone MPP mode		0.3		mV/s
DSI2	Dark signal image zone non-MPP mode		60		mV/s
DSR	Dark signal readout register (non-MPP mode)		150		mV/s
VDS(3)	Average dark signal		7	20	mV
DSNU(3)	Dark signal non-uniformity, σ		3.5	5.5	mV
V_N	Temporal RMS noise in darkness @ BW = 150 MHz		270		µV
DR	Dynamic range		67		dB
	Linearity		1		%
MTF	Modulated transfer function		45		%
VCTE(4)	Vertical charge transfer efficiency (per stage)	0.99995	0.999998		–
HCTE(4)	Horizontal charge transfer efficiency (per stage)	0.99995	0.999998		–

Notes: 1. Measurement conditions:
T_C = 25°C (chip temperature)
Vertical transfer time: T_V = 10 µs
Readout pixel frequency: F_H = 5 MHz
Readout through 4 outputs and standard mode 9 (see Figure 4)
3200K Halogen lamp with 2 mm BG38 filter at f/11 aperture
2. See additional operating modes
3. Integration Time Ti = 10 s in darkness
4. Output voltage > 10% VSAT

Figure 12. Typical Spectral Response

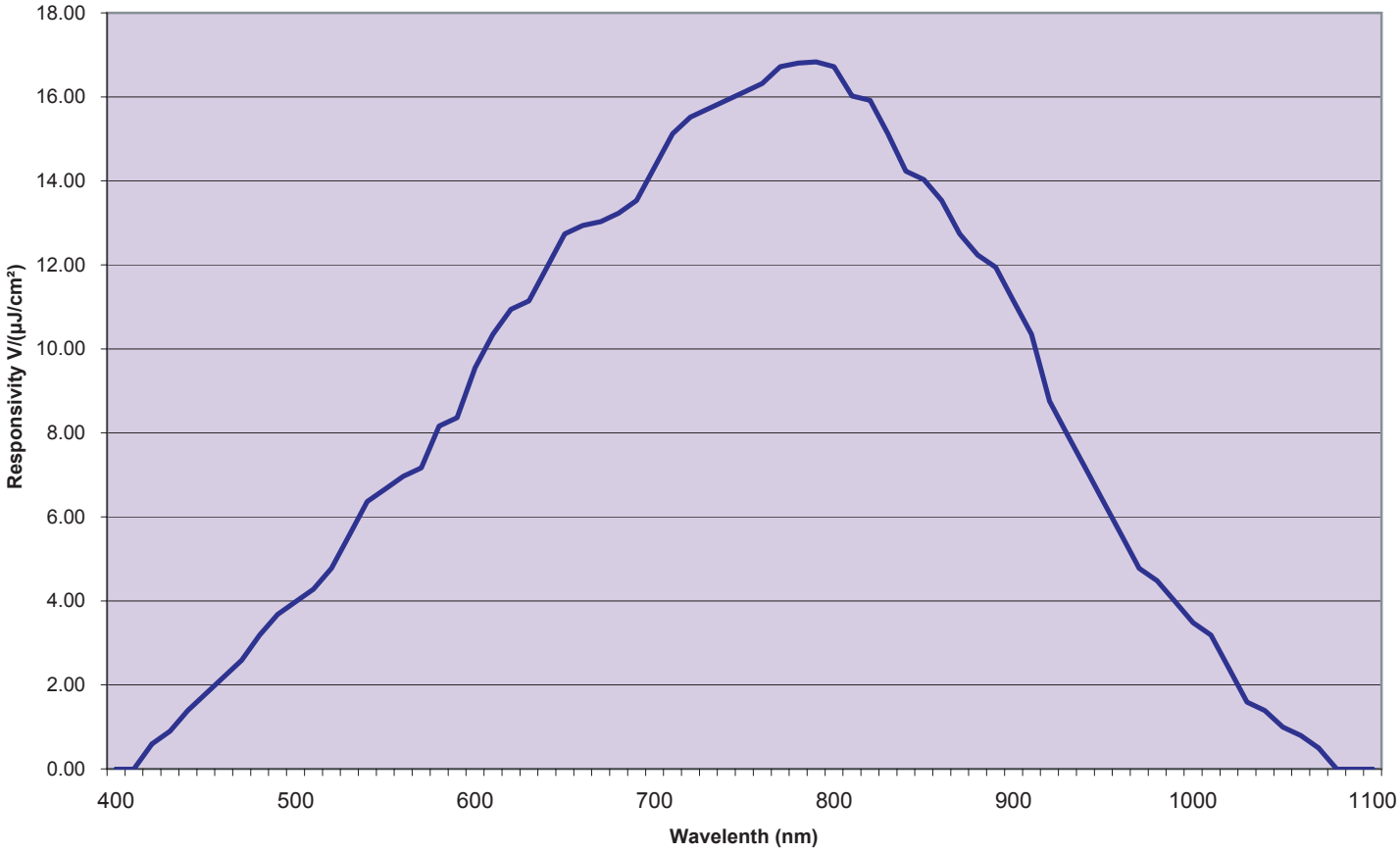


Image Grade

Table 10 gives results of image grade testing.

Table 10. Image Grade[1]

	Blemishes		Cluster 1		Cluster 2		Column	
Grade	**Total**	**D min[2]**	**Total**	**D min[2]**	**Total**	**D min[2]**	**Total**	**D min[2]**
E	≤ 500	3	≤ 30	50	≤ 6	100	≤ 3	150
H	≤ 300	3	≤ 10	50	0		0	

Notes: 1. Testing has been carried out under the following conditions:
Operating temperature: 25°C (unless otherwise specified)
Illumination conditions: 3200K Halogen lamp with BG38 Infrared filter and f/11 aperture
Integration time = 10s in darkness
Test under illumination at 50% of saturation level
Standard mode, T_V = 10 µs, FH = 5 MHz
2. D min: Minimum number of pixels separating defects in any direction. All occurences are non-contiguous.

Definitions

Table 11. Defect Sizes

Type	Description
Blemish	1 x 1 defect
Cluster	Blemish grouping of not more than a given number of adjacent defects: 1 x 1 < cluster 1 size ≤ 2 x 2 2 x 2 < cluster 2 size ≤ 5 x 5
Column	One-pixel-wide column with more than seven contiguous defective pixels

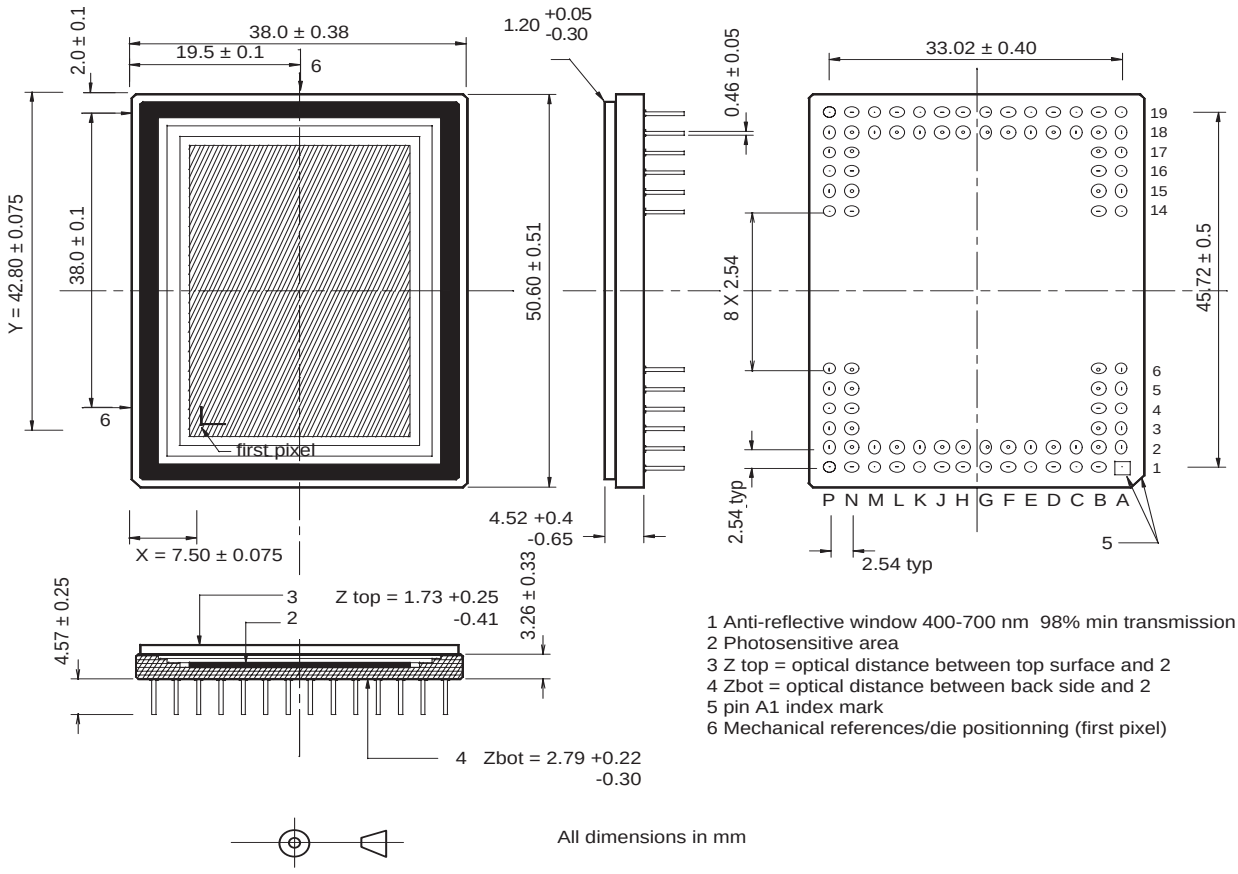
Table 12. Defects in Darkness

Type	Description
Blemish/Cluster	Pixel signal deviation of more than 200 mV from the average output signal
Column	Column signal deviation of more than 20 mV from the average output signal

Table 13. Defects under Illumination

Type	Description
Blemish/Cluster	Pixel deviation of more than ±20% from the average output signal
Column	Column deviation of more than 10% from the average output signal

Package Drawing

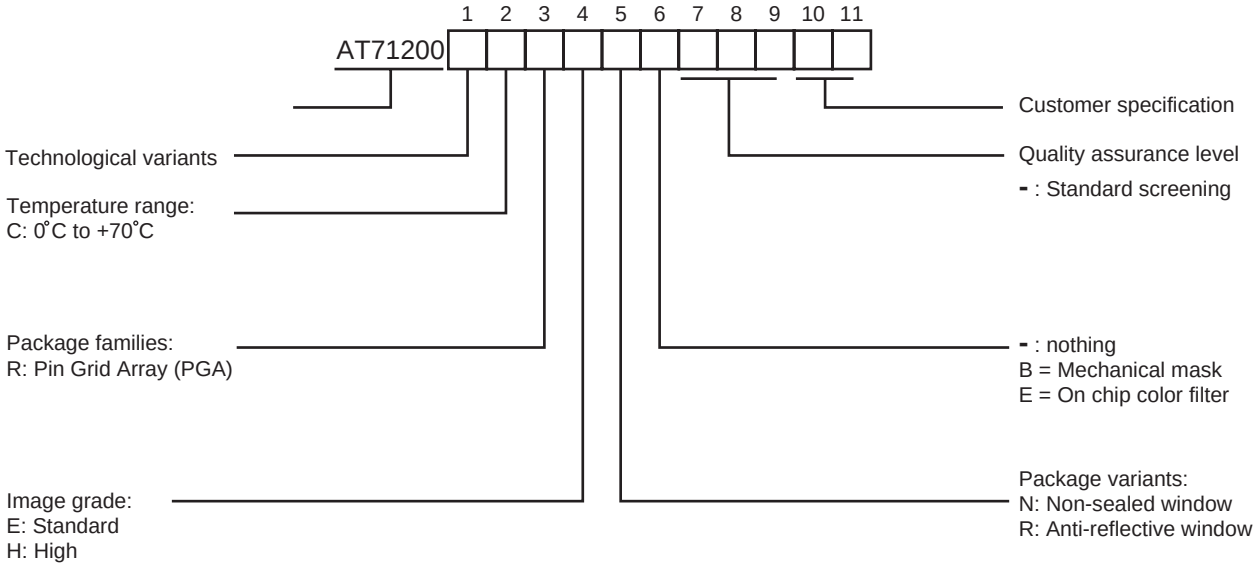


1 Anti-reflective window 400-700 nm 98% min transmission
2 Photosensitive area
3 Z top = optical distance between top surface and 2
4 Zbot = optical distance between back side and 2
5 pin A1 index mark
6 Mechanical references/die positionning (first pixel)

All dimensions in mm

Ordering Information

Figure 13. Ordering Information Key



The following part numbers are available:

- AT71200MCRER: full frame version grade E
- AT71200MCRHR: full frame version grade H
- AT71200MCRERB: frame transfer version with two memories zones

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