TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6C61

COLUMN DRIVER FOR A DOT MATRIX LCD

The T6C61 is a 160-channel-output column driver for an STN dot matrix LCD.
The T6C61 features a 42-V LCD drive voltage and a 25-MHz maximum operating frequency. The T6C61 is able to drive LCD panels with a duty ratio of up to 1 / 480.
It is recommended for use with the T6C14.

Unit: mm

T6C61	LEAD PITCH	
	IN	OUT
(UAN, 3NS)	0.48	0.08

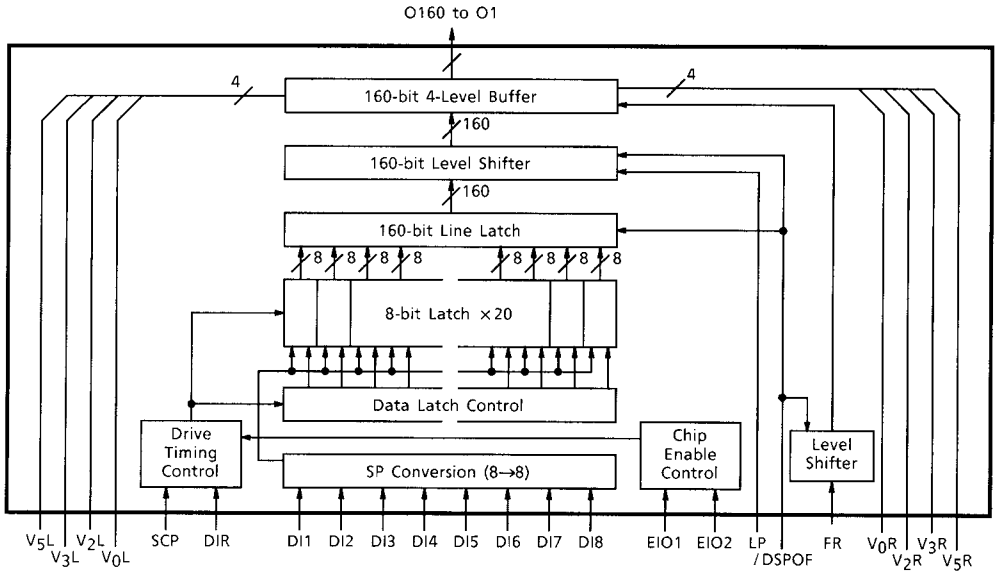
Please contact Toshiba or an authorized Toshiba dealer for information on package dimensions.

TCP (Tape Carrier Package)

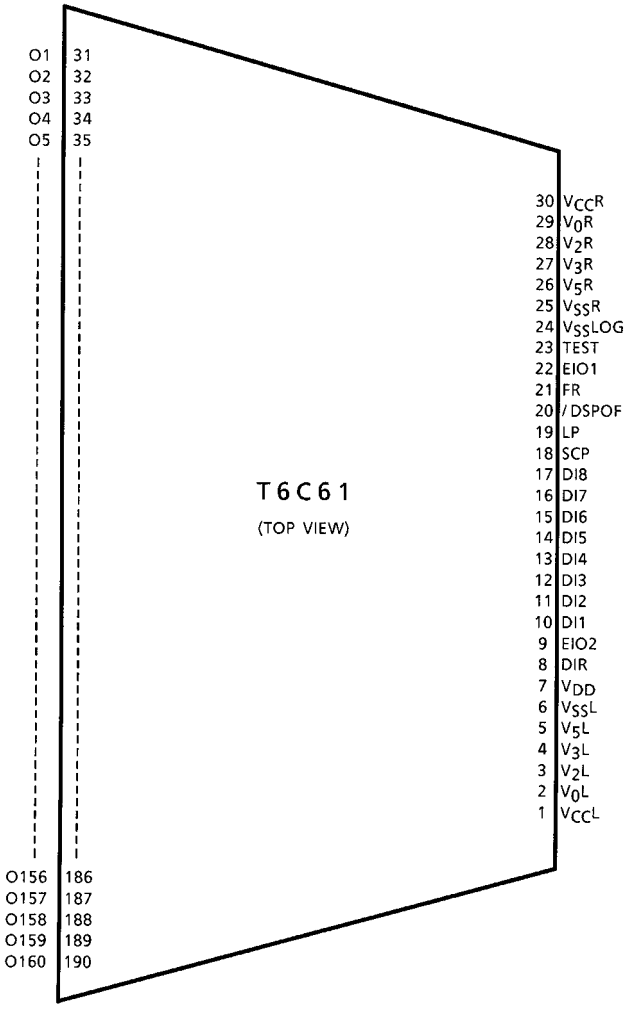
FEATURES

- Display duty application : to 1/480
- LCD drive signal : 160
- Data transfer : 8-bit bidirectional
- Operating frequency : 25 MHz (V_{DD} = 4.5 V)
  13 MHz (V_{DD} = 2.7 V)
- LCD drive voltage : 14 to 42 V (max 45 V)
- Power supply voltage : 2.7 to 5.5 V
- Operating temperature : −20 to 75°C
- LCD drive output resistance : 700 Ω (typ.), 1200 Ω (max) (20 V, 1 / 13 bias)
- Display-off function : When / DSPOF is L, all LCD drive outputs (O1 to O160) remain at the V_5 level.
- Low power consumption : Cascade connection and auto enable transfer functions are available.

BLOCK DIAGRAM



PIN ASSIGNMENT



The above diagram shows the pin configuration of the LSI chip, not that of the tape carrier package.

PIN FUNCTIONS

PIN NAME	I / O	FUNCTIONS	LEVEL
O1 to O160	Output	Output for LCD drive signal	V_0 to V_5
EIO1, EIO2	I / O	Input / output for enable signal DIR selects In or Out. Connect EIO (IN) of 1st LSI to L. For a cascade connection, connect EIO (OUT) to EIO (IN) of next LSI. When DIR is high level, refer to as below. SCP rising edge that input after falling edge of EIO1 (IN) is set to be enable. At SCP 20 th clock, all 160-bit data latched, When EIO2 (OUT) is disenable, it is always set to high level. IN SCP rising edge to next SCP rising edge after 20 clock from chip enable, it is set to low level.	V_{DD} to V_{SS}
DI1 to DI8	Input	Input for data signal	
DIR	Input	(Direction) Input for data flow direction select	
/ DSPOF	Input	(Display Off) / DSPOF = L : Display-off mode, (O1 to O160) remain at the V_5 level. / DSPOF = H: Function mode, (O1 to O160) are operational.	
LP	Input	(Latch Pulse) Input for latch pulse Display data is latched on the falling edge of LP. When EIO (IN) = L, setting SCP ·LP = H enables the 1st LSI. When EIO (IN) is fixed to low level, 1st LSI in cascade connectio nis latched chip enable at /SCP LP = high level.	
FR	Input	(Frame) Input for frame signal	
SCP	Input	(Shift Clock Pulse) Input for shift clock pulse	
TEST	Input	(Test) Fix to L or open	
V_{DD}	—	Power supply for internal logic (5 V)	—
V_{SS}LOG	—	Power supply for internal logic (0 V)	
V_{SS}L·R	—	Power supply for LCD drive circuit	
V_5L·R	—	Power supply for LCD drive circuit	
V_3L·R	—	Power supply for LCD drive circuit	
V_2L·R	—	Power supply for LCD drive circuit	
V_0L·R	—	Power supply for LCD drive circuit	
V_{CC}L·R	—	Power supply for LCD drive circuit	

RELATION BETWEEN FR, DATA INPUT AND OUTPUT LEVEL

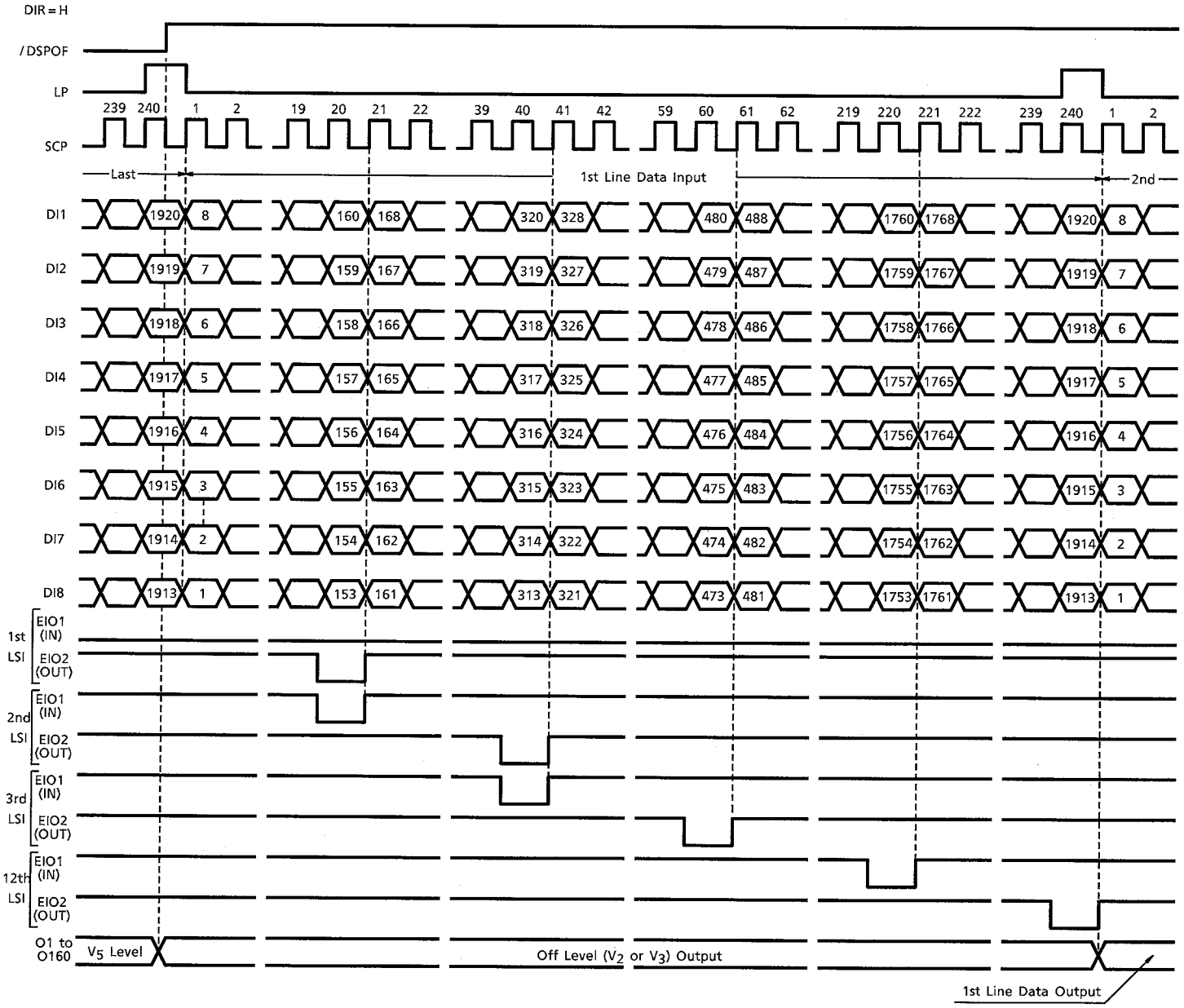
F R	DATA INPUT (DI1 to DI8)	/ DSPOF	OUTPUT LEVEL
H	L	H	V_2
H	H	H	V_0
L	L	H	V_3
L	H	H	V_5
—	—	L	V_5

DATA INPUT FORMAT

DIR	ENABLE PIN		(*1)	INPUT DATA LINE AND OUTPUT BUFFERS							
	EIO1	EIO2		DI1	DI2	DI3	DI4	DI5	DI6	DI7	DI8
H	IN	OUT	L	O160	O159	O158	O157	O156	O155	O154	O153
			F	O8	O7	O6	O5	O4	O3	O2	O1
L	OUT	IN	L	O1	O2	O3	O4	O5	O6	O7	O8
			F	O153	O154	O155	O156	O157	O158	O159	O160

*1 : L: Last Data F: First Data

TIMING DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

(Ensure that the following conditions are maintained, $V_{CC} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq V_{SS}$)

ITEM	SYMBOL	PIN NAME	RATING	UNIT
Supply Voltage 1	V_{DD}	V_{DD}	− 0.3 to 6.5	V
Supply Voltage 2	V_{CC}	V_{CC}L / R	−0.3 to 45.0	
Supply Voltage 3	V_0, V_2	V_OL / R, V_2L / R	−0.3 to V_{CC} +0.3	
Supply Voltage 4	V_3, V_5	V_3L / R, V_5L / R	−0.3 to V_{CC} +0.3	
Input Voltage	V_{IN}	(*2)	−0.3 to V_{DD} +0.3	
Operating Temperature	T_{opr}	—	−20 to 75	°C
Storage Temperature	T_{stg}	—	−40 to 125	

*2 : SCP, FR, LP, DIR, EIO1, EIO2, DI1 to DI8, / DSPOF, TEST

ELECTRICAL CHARACTERISTICS
DC CHARACTERISTICS
(Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, V_{CC} = 14 to 42 V, Ta = −20 to 75°C)

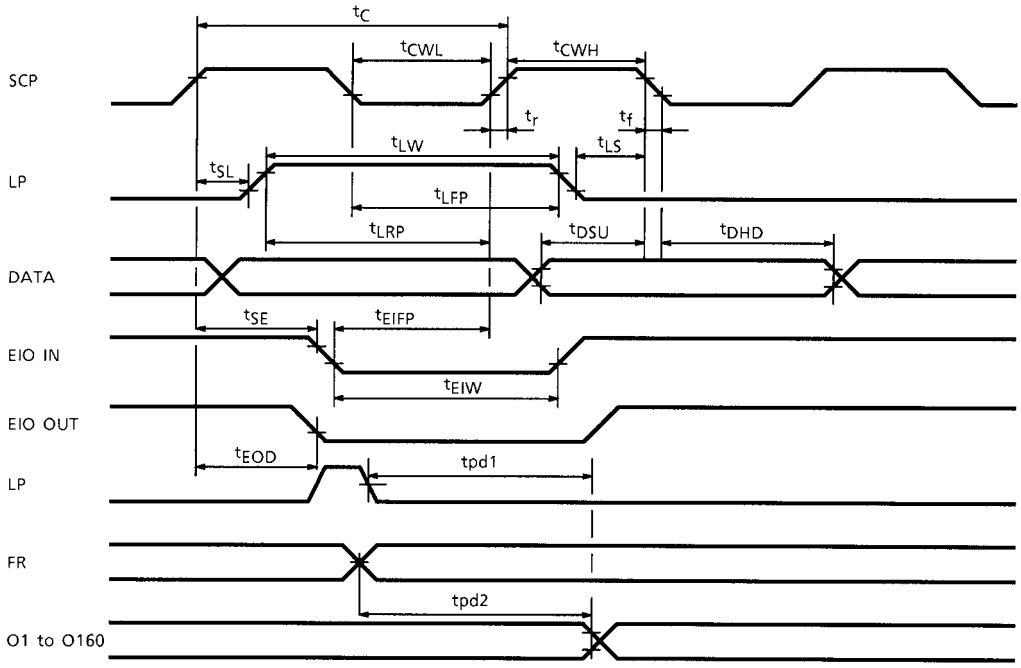
ITEM		SYMBOL	TEST CIR-CUIT	TEST CONDITION			MIN	TYP.	MAX	UNIT	PIN NAME
Supply Voltage 1		V_{DD}	—	—			2.7	5.0	5.5	V	V_{DD}
Supply Voltage 2		V_{CC}	—	—			14	—	42		V_{CC}L / R
Input Voltage	H Level	V_{IH}	—	—			0.8 V_{DD}	—	V_{DD}		SCP, FR, LP, DIR, EIO1, EIO2, DI1 to DI8, / DSPOF, TEST
	L Level	V_{IL}		—			0	—	0.2 V_{DD}		
Output Voltage	H Level	V_{OH}	—	I_{OH} = −0.5 mA			V_{DD} −0.5	—	VDD		EIO1, EIO2
	L Level	V_{OL}		I_{OL} = 0.5 mA			0	—	0.5		
Output Resistance	H Level	R_{OH}	—	V_{OUT} = V_0 − 0.5 V		(*3)	—	700	1200	Ω	O1 to O160
	M Level	R_{OM}		V_{OUT} = V_2 ± 0.5 V		(*3)	—	700	1200		
				V_{OUT} = V_3 ±0.5 V		(*3)	—	700	1200		
	L Level	R_{OL}		V_{OUT} = V_5 + 0.5 V		(*3)	—	700	1200		
Input Current		I_{IL}	—	V_{DD}	V_{CC}	CONDITION	−10	—	10	μA	V_0L / R V_2L / R V_3L / R V_5L / R
				5.0	42	Standby					
Current Consumption		I_{DD} Ope	—	5.0	20	Function (*4)	—	—	5.0	mA	V_{DD}
				2.7			—	—	2.5		
		I_{DD} St / by		5.0		Function (*5)	—	—	2.0		
				2.7			—	—	1.0		
		I_{CC} Leak		5.0	42	Standby	−10	—	10	μA	V_{CC}L / R

*3 : V_{CC} = 20 V, 1 / 13 bias

*4 : f_{scp} = 13 MHz, f_{LP} = 54 kHz, f_{FR} = 13.5 kHz, f_{EIO} = 650 kHz
Data Format: every bit inverted, while internal data receiver is operating

*5 : f_{scp} = 13 MHz, f_{LP} = 54 kHz, f_{FR} = 13.5 kHz
Data Format: every bit inverted, while internal data receiver is sleeping

AC CHARACTERISTICS



TEST CONDITIONS (1)

(Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, V_{CC} = 14 to 42 V, Ta = −20 to 75°C)

ITEM	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Clock Cycle	t_C	—	40	—	—	ns
SCP Pulse Width	t_{CWH}	—	15	—	—	
	t_{CWL}	—	15	—	—	
Data Set-Up Time	t_{DSU}	—	10	—	—	
Data Hold Time	t_{DHD}	—	10	—	—	
SCP Rise / Fall Time	t_r, t_f	—	—	—	(*6)	
LP Rise Time	t_{LRP}	—	15	—	—	
LP Fall Time	t_{LFP}	—	10	—	—	
LP Pulse Width	t_{LW}	—	10	—	—	
SCP-to-LP Delay Time	t_{SL}	—	5	—	—	
LP-to-SCP Delay Time	t_{LS}	—	10	—	—	
EIO-IN Rise Time	t_{EIFP}	—	20	—	—	
EIO-IN Pulse Width	t_{EIW}	—	10	—	—	
SCP-to-EIO Delay Time	t_{SE}	—	5	—	—	
EIO-OUT Delay Time	t_{EOD}	(*7)	—	—	20	
Output Delay Time 1 (LP → OUT)	t_{pd1}	—	—	—	400	
Output Delay Time 2 (FR → OUT)	t_{pd2}	—	—	—	400	
Output Delay Time Variation	(*8)	—	—	0	30	

*6 : t_r, $t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$ and t_r, $t_f \leq 50$ ns

*7 : C_L = 10 pF

*8 : Variation in t_{pd1} and t_{pd2}

TEST CONDITIONS (2)

(Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 2.7 to 4.5 V, V_{CC} = 14 to 42 V, Ta = −20 to 75°C)

ITEM	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Clock Cycle	t_C	—	76	—	—	ns
SCP Pulse Width	t_{CWH}	—	30	—	—	
	t_{CWL}	—	30	—	—	
Data Set-Up Time	t_{DSU}	—	28	—	—	
Data Hold Time	t_{DHD}	—	28	—	—	
SCP Rise / Fall Time	t_r, t_f	—	—	—	(*9)	
LP Rise Time	t_{LRP}	—	28	—	—	
LP Fall Time	t_{LFP}	—	28	—	—	
LP Pulse Width	t_{LW}	—	5	—	—	
SCP-to-LP Delay Time	t_{SL}	—	10	—	—	
LP-to-SCP Delay Time	t_{LS}	—	40	—	—	
EIO-IN Rise Time	t_{EIFP}	—	28	—	—	
EIO-IN Pulse Width	t_{EIW}	—	5	—	—	
SCP-to-EIO Delay Time	t_{SE}	—		—	—	
EIO-OUT Delay Time	t_{EOD}	(*10)	—	—	35	
Output Delay Time 1 (LP → OUT)	t_{pd1}	—	—	—	500	
Output Delay Time 2 (FR → OUT)	t_{pd2}	—	—	—	500	
Output Delay Time Variation	(*11)	—	—	0	50	

*9 : t_r, $t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$ and t_r, $t_f \leq 50$ ns

*10 : C_L = 10 pF

*11 : Variation in t_{pd1} and t_{pd2}

NOTE : Insert the bypass capacitor (0.1μF) between V_{DD} and V_{SS}, and between V_{CC} and V_{SS} to decrease power supply noise.
Place the bypass capacitor as close to the LSI as possible.

RESTRICTIONS ON PRODUCT USE

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