ATMEL
WIRELESS & µC ®

e1217X
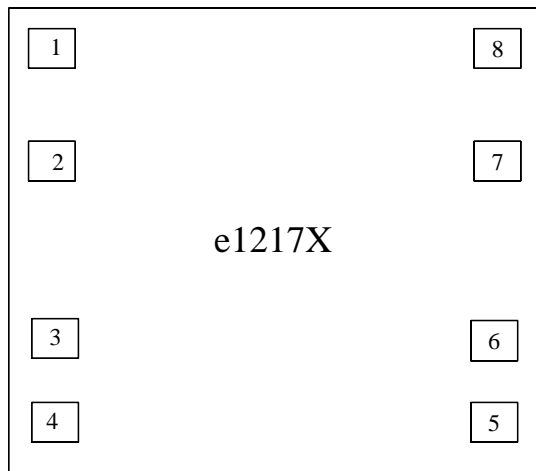
32-kHz Standard Watch CMOS IC

Features

- 32-kHz oscillator
- 1.3 V to 1.8 V operating-voltage range
- 180 nA typical current consumption
- Voltage regulator
- Integrated capacitors, mask selectable
- Mask options for pad designation, motor period and motor pulse width
- Low resistance outputs for bipolar stepping motor
- Motor fast-test function

Pad Configuration

95 9979

Figure 1. Chip size 1.06 mm x 1.02 mm
Pad size: 112 µm x 112 µm
Pad window: 100 µm x 100 µm

General Description

The e1217X is an integrated circuit in CMOS Silicon Gate Technology for analog watches. It consists of a 32-kHz oscillator, frequency dividers down to 1/64 Hz, output pulse formers and push-pull motor drivers. For tuning of the crystal, integrated capacitors are provided (selectable mask option). Low current consumption and high oscillator stability are enabled by an on-chip voltage regulator.

Pin	Symbol	Function
1, 4	V_{SS}	Negative supply voltage
5, 6, 8	V_{DD}	Positive supply voltage
1 to 4	OSCIN/ OSCOUT	Oscillator input/output
(7/5) or (7/6)	MOT 1/2	Motor drive outputs
1 to 5, 8	RESET	Reset input
1 to 5, 8	TEST	Test input/output

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	V_{SS}	–0.3 to +5	V
Input voltage range, all inputs	V_{IN}	$(V_{SS}–0.3\ V) \le V_{IN} \le (V_{DD} + 0.3\ V)$	V
Output short circuit duration		indefinite	
Power dissipation (DIL package)	P_{tot}	125	mW
Operating ambient temperature range	T_{amb}	–20 to +70	°C
Storage temperature range	T_{stg}	–40 to +125	°C
Lead temperature during soldering at 2 mm distance, 10 s	T_{sld}	260	°C

Absolute maximum ratings define parameter limits which, if exceeded, may permanently change or damage the device.

All inputs and outputs on Atmel Wireless & Microcontrollers' circuits are protected against electrostatic discharges. However, precautions to minimize the build-up of electrostatic charges during handling are recommended.

The circuit is protected against supply-voltage reversal for typically 5 minutes.

e1217X

Functional Description

Voltage Regulator

An integrated voltage regulator provides the oscillator with a well controlled negative supply voltage V_{REG}. This improves the stability of the oscillator and keeps current consumption at a minimum.

Oscillator

An oscillator inverter with feedback resistor is provided for generation of the 32768 Hz clock frequency. A total capacitance of 24 pF is integrated.This can be selected for C_{OSCOUT} in 2 pF increments via a mask option.

Frequency Divider

A 21-bit binary counter is provided, dividing the oscillator frequency down to 1/64 Hz. The leading six stages are connected to V_{DD} and V_{REG}, while the remaining 15 stages are connected to V_{DD} and V_{SS}.

Motor Drive Output

The e1217X contains two push-pull output buffers for driving bipolar stepping motors. During a motor pulse, the n-channel device of one buffer and the p-channel device of the other buffer are activated. The p-channel devices of both buffers are active (figure 3) between two the pulses.

Cycle time and pulse width can be chosen via a metal-mask option (table1).

RESET

A debounced RESET input is provided. Connecting the RESET input to V_{DD} resets the low order 12 stages of the frequency divider, thus disabling further motor pulses. Motor pulses in progress when the reset function is applied are completed. After releasing the RESET pad from V_{DD}, the next motor pulse appears with a delay of one half motor cycle on the drive output opposed to the former (figure 4). Due to the debounce circuitry on the RESET input, V_{DD} must be applied for at least 31.2 ms. During RESET the input current is limited to 8 nA typically.

Test

A test frequency of 512 Hz is output to this pad which can be measured with a high resistance probe ($R \geq 10\ M\Omega$, $C \leq 20\ pF$). This signal can be used for testing and tuning the oscillator. Connecting TEST to V_{DD} for at least 4 ms changes the motor cycle time from the selected value to the test cycle time (mask options), while the motor pulse width remains unchanged (figure 3).

This feature can be used to reduce the amount of time required for testing the mechanical parts of the watch.

Table 1 Motor options

Cycle time T_M	= 2, 4, 6, 8, 10, 12, 20, 24, 30, 40, 60, 80, 120 s
Motor pulse width t_M	= 0.98 to 14.65 ms in increments of 0.98 ms
Motor test cycle time T_{MT}	= 250, 125, 62.5 ms

Operating Characteristics

V_{DD} = 0 V; V_{SS} = –1.55 V; T_{amb} = +25°C; C_{TR} = 15 pF, unless otherwise specified.
All voltage levels are measured with reference to V_{DD}. Test crystal as specified below.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Operating voltage	Functional test (figure 2)	V_{SS}	–1.3		–1.8	V
Operating current	C_{oscout} = 16 pF, R_L = ∞	I_{SS}		–180	–300	nA
RESET input current	RESET = V_{DD}	I_R		8		nA
Motor outputs						
Motor output current	R_L = 2 kΩ, V_{SS} = –1.55 V	I_M	± 0.7			mA
Motor period		T_M				s
Motor pulse width		T_M	See option list			ms
Motor test period		T_{MT}				ms
Oscillator						
Stability	ΔV_{SS} = 100 mV, C_{TR} = 5 pF,	$\Delta f/f$		0.1		ppm
Start-up voltage	Startup within 2 s	V_{ST}	–1.3			V
Integrated input capacitor		$C_{OSC\ IN}$	See option list			pF
Integrated output capacitor	$C_{OSCOUTmax}$ = 24 pF	$C_{OSC\ OUT}$	See option list			pF

Note 1: Typical parameters represent the statistical mean values

95 9980
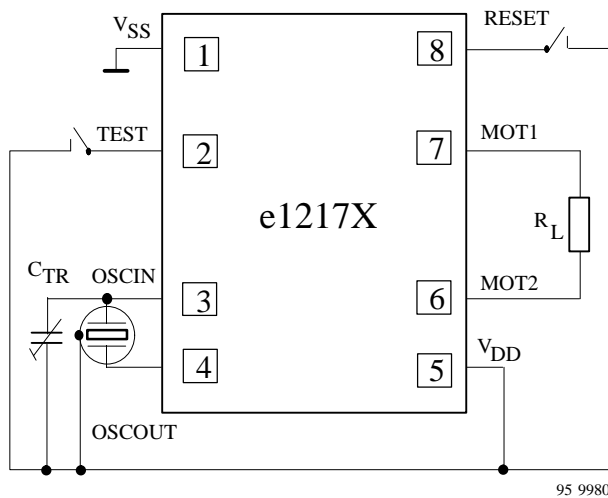
Figure 2. Functional test circuit

Range of trimmer capacitance:
C_{TR} = 5 pF to 30 pF

Test Crystal Specification

Frequency   f = 32768 Hz
Series resistance R_S = 30 kΩ
Static capacitance C_0 = 1.5 pF
Dynamic capacitance C_1 = 3 fF
Load capacitance C_L = 8 pF

Additional Notes

1. It is recommended to connect the quartz case to V_{DD} (by conductive epoxy).

2. Capacitive coupling of TEST to OSCIN must be minimized by appropriate layout of the PCB to avoid disturbance of the oscillator.
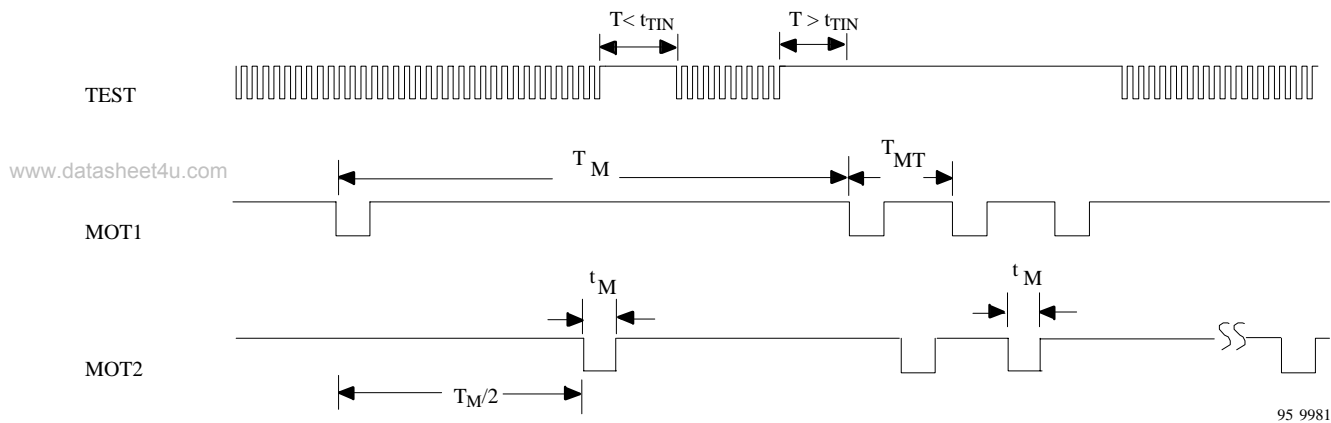
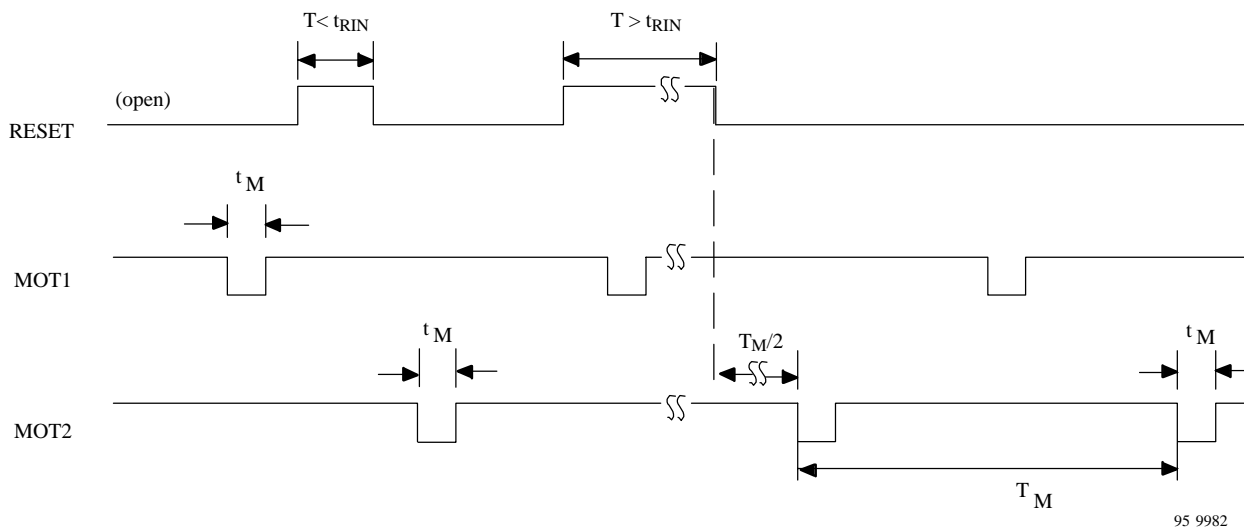Figure 3. Motor drive outputs in normal mode and motor test

Figure 4. Motor drive outputs and RESET

Table 2 Option list e1217X–

Option	Motor			Integrated Capacitance *)		Pad 1	Pad 2	Pad 3	Pad 4	Pad 5	Pad 6	Pad 7	Pad 8
	Cycle (T_M) s	Pulse (t_M) ms	Test (T_{MT}) ms	C_{OSCIN} pF	C_{OSCOUT} pF								
–B	2	3.9	125	2	14	V_{SS}	TEST	OSCIN	OSC-OUT	V_{DD}	MOT2	MOT1	RESET
–E	2	6.8	125	2	14	V_{SS}	TEST	OSCIN	OSC-OUT	V_{DD}	MOT2	MOT1	RESET
–I	2	7.8	125	2	14	V_{SS}	TEST	OSCIN	OSC-OUT	V_{DD}	MOT2	MOT1	RESET
–S	2	5.9	125	2	14	V_{SS}	TEST	OSCIN	OSC-OUT	V_{DD}	MOT2	MOT1	RESET
–VA	2	4.9	62.5	4	14	V_{SS}	TEST	OSC-OUT	OSCIN	V_{DD}	MOT2	MOT1	RESET
–VB	2	4.9	125	4	14	OSCIN	OSC-OUT	RESET	V_{SS}	TEST	MOT2	MOT1	V_{DD}
–VC	40	5.9	125	2	14	OSCIN	OSC-OUT	RESET	V_{SS}	TEST	MOT2	MOT1	V_{DD}
–VE	2	5.9	62.5	2	14	OSC-OUT	OSCIN	V_{DD}	V_{SS}	TEST	MOT2	MOT1	RESET
–VF	2	3.9	62.5	4	14	OSCIN	OSC-OUT	RESET	V_{SS}	MOT2	VDD	MOT1	TEST
–VH	2	3.9	62.5	4	14	V_{SS}	TEST	OSC-OUT	OSCIN	V_{DD}	MOT2	MOT1	RESET
–WB	2	4.9	125	4	14	V_{SS}	TEST	OSCIN	OSC-OUT	V_{DD}	MOT2	MOT1	RESET
–WG	20	5.9	125	2	14	V_{SS}	TEST	OSCIN	OSC-OUT	V_{DD}	MOT2	MOT1	RESET
–WH	40	6.8	62.5	2	14	V_{SS}	TEST	OSCIN	OSC-OUT	V_{DD}	MOT2	MOT1	RESET

*) On-chip stray capacitance included