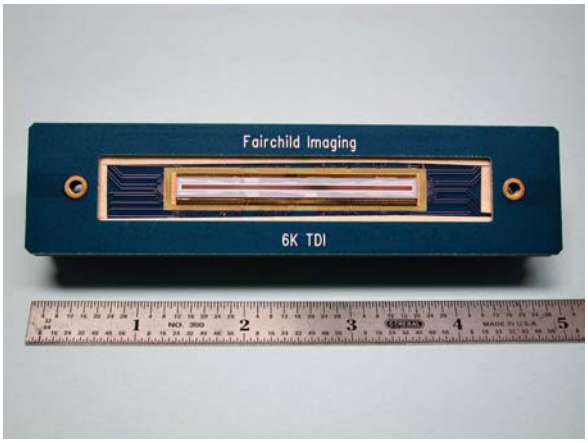
CCD5061
6K x 128 Element
TDI – Time, Delay and Integration Sensor

FEATURES

- **6144 pixels per line**
- **128 lines of integration**
- **8.75µm x 8.75µm pixel size**
- **# of TDI stages selectable from 128, 64, 32, 16, 8, 4**
- **Bi-directional TDI line shifting (shift up or down)**
- **4 outputs—each capable of 20MHz data rate—80MHz total data rate**
- **100% fill factor**
- **On-chip binning capability**



GENERAL DESCRIPTION

The CCD5061 is a 6144 pixel x 128 line, high speed TDI sensor. The active imaging area is organized as 6144 vertical columns and 128 horizontal TDI rows. The array is set up for bi-directional operation. There are identical output registers and amplifiers on both the top and the bottom of the array. The outputs to be used (either top or bottom) are user-selectable and controlled by the vertical clock phasing. In addition, the exposure level can be controlled by reducing the number of TDI rows from 128 to 64, 32, 16, 8 or 4. This is also user-selectable and is accomplished by supplying the appropriate phasing for the vertical clocks within each section. For instance, if 64 lines of TDI were required, the vertical clocks for lines 65-128 would be connected to a high potential, which would drain these unused rows out to the opposite side (unused) of the array to be dumped in the drain. With four outputs, each running at 20MHz, the CCD5061 can provide a total data rate of 80MHz enabling the CCD to run at better than 12KHz line rate. Utilizing Fairchild Imaging proprietary buried channel CCD process, the CCD5061 achieves consistent, superior TDI performance.

The active imaging area is separated from the four horizontal output registers by 21 isolation rows. These isolation rows are covered by a metal lightshield to protect them while charge transfers to the output registers. Both the active imaging area and the isolation region utilize 3-phase clocking.

The four horizontal output registers utilize 4-phase clocking. Special design techniques have been implemented to maximize charge transfer efficiency especially at low light levels. The output amplifier is a 3-stage source follower configuration. This allows maximum scale factor (charge to voltage conversion) and maximum bandwidth.

The CCD5061 is housed in a custom 176 pin (100 mil grid) ceramic PGA package. It has an AR coated window.

FUNCTIONAL DESCRIPTION

The following functional elements are illustrated in the block diagram:

Image Sensing Elements: These are elements of a line of 6144 image sensors separated by channel stops and covered by a passivation layer. Incident photons pass through a transparent polycrystalline silicon gate structure creating electron hole pairs. The resulting photoelectrons are collected in the photosites during the integration period. The amount of charge accumulated in each photosite is a linear function of the localized incident illumination intensity and integration period.

Transfer Gates: This gate is a structure adjacent to the row of image sensor elements. The charge packets accumulated in the photosites are transferred in parallel via the transfer gate to the transport shift

registers whenever the transfer gate voltage goes high.

Shift Registers: The vertical shift register is 3-phase and the horizontal shift register is 4-phase.

Time Delay and Integration: This function is accomplished by scanning the image scene across the array at the same rate as the vertical shift register moves the signal charge. This results in an effective increase in the integration time.

Output Amplifier: The CCD5061 is designed for either uni-directional for bi-directional operation. There are four identical output registers and amplifiers on both the top and bottom of the array. There are three-stage source follower amplifiers with a reset MOSFET tied to the input gate.

Charge packets are clocked to a pre-charged capacitor whose potential changes linearly in response to the number of electrons delivered. This potential is applied to the input gate of an NMOS amplifier producing a signal at the output V_{out} pin. The capacitor is reset with ϕR to a pre-charge level prior to the arrival of the next charge packet except when horizontally binning. It is reset by use of the reset MOSFET.

The output amplifier drain is tied to VDD. The source is connected to an external load resistor to ground. The source constitutes the video output from the device.

DEFINITION OF TERMS

Charge-Coupled Device: A charge-coupled device is a monolithic silicon structure in which discrete packets of electron charge are transported from position to position by sequential clocking of an array of gates.

Isolation Rows: There are 21 isolation rows between the image area and the horizontal shift register. These non-imaging rows are used as buffer rows to eliminate crosstalk to the horizontal shift register.

Dynamic Range: The ratio of saturation output voltage to RMS noise in the dark. The peak-to-peak random noise is 4-6 times the RMS noise output.

RMS Noise Equivalent Exposure: The exposure level that gives an output signal equal to the RMS noise level at the output in the dark.

Saturation Exposure: The minimum exposure level that produces an output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the product of light intensity and integration time.

Charge Transfer Efficiency: Percentage of valid charge information that is transferred between each successive stage of the transport register.

Responsivity: The output signal voltage per unit of exposure.

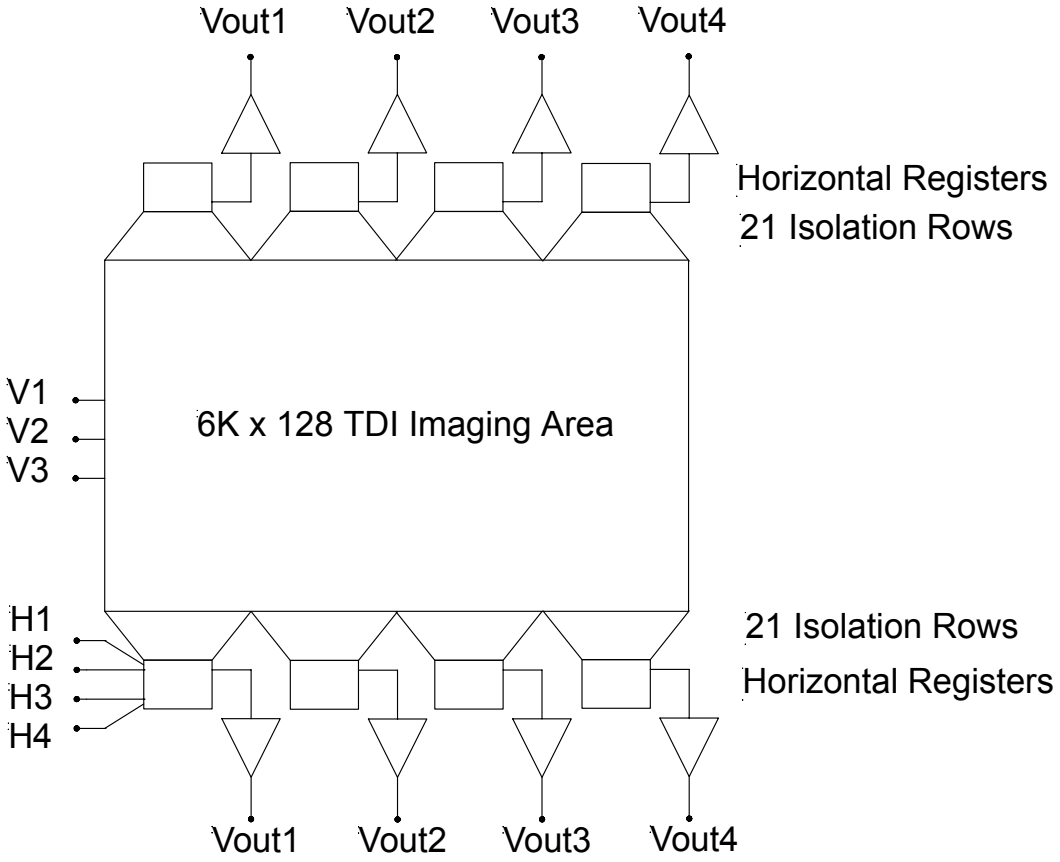
Photo-Response Non-Uniformity: The difference of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.

Dark Signal: The output signal caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

Integration Time: The time interval between the falling edges of any two successive transfer pulses is the integration time shown in the timing diagram. The integration time is the time allowed for the photosites to collect charge.

Pixel: Picture element or sensor element, also called photoelement or photosite.

BLOCK DIAGRAM



Fairchild imaging

CCD5061
6K x 128 Element
TDI – Time, Delay and Integration Sensor

Device Architecture		
Array Size	6144 pixels per line; 128 lines of integration	TDI
Pixel Size	8.75µm x 8.75µm	
Image Format	53.76 x 1.12	mm^2
Number of Outputs	8	4 Top, 4 Bottom
Pixel Output Rate	80MHz	20MHz x 4 Outputs
Number of Vertical Clocks	3	
Number of Isolation Rows	21 top, 21 bottom	
Number of Horizontal Clocks	4	
Pixel Rate per Output	20MHz	

Performance Specifications					
Symbol	***Parameter***	***Min.***	***Nominal***	***Max.***	***Units/Remarks***
V_{SAT}	Saturation Voltage		1.5		V
Q_{SAT}	Saturation Charge	350	450		Ke- at 12KHz
VLIN	Linearity		1%	5%	10% to 90% Full Well
SF	Scale Factor	2.5	3.3		µV/e-
DR	Dynamic Range		10,000		
HCTE	Horizontal CTE	.99998	0.999990		Per Transfer
VCTE	Vertical CTE	.9998	0.99990		Per Transfer
NE	Read Noise		40	50	e-rms
PRNU	Photoresponse Non-Uniformity		5	20	%
	Device Flatness		30		µm

TEST CONDITIONS

All testing performed at 25ºC (nominal) with horizontal clock frequency of 20MHz per output and vertical clock frequency of 12KHz.

CCD HANDLING PRECAUTIONS TO PREVENT ESD DAMAGE

By their very nature, CCDs are very sensitive to electro-static discharge (ESD) damage. Special ESD-control equipment and personnel training are mandatory, particularly when installing or removing the CCD from a camera system. See Fairchild Imaging application note “Prevention of ESD Damage in CCD Image Sensors” for details. Key points:

- Use ESD-safe workbench surfaces. Cover metallic workbench surfaces with ESD-safe grounded mats. Remove non-ESD-safe materials (paper, tools with plastic handles, etc.) from work area.
- Use wrist straps or equivalent (~1MΩ to ground), ESD-safe lab coat or equivalent (buttoned—not open), and ESD-safe gloves or finger cots. Test wrist strap before handling CCDs.
- Relative humidity must be 40% min.; >50% recommended.
- Use ionizing air blowers; type: AC (not pulsed DC), balance $\leq|\pm 20V|$ max., $\leq|\pm 10V|$ recommended. Performance spec at work area: voltage decay from 1000V to 100V in <10 seconds. Measure this periodically; air ionizers require maintenance.
- Allow devices to slowly discharge in the ionized air stream when removing devices from their 1st-level container, and when removing devices from test sockets.
- The receiving socket and associated circuitry must be adequately grounded.
- Store CCDs with all pins shorted together by shorting bars, conductive foam, or the equivalent.

ESD damage invalidates the warranty.

CCD5061 Output Amplifier Voltages & External Load						
Symbol	**Parameter**	**Range**			**Unit**	**Remarks**
		Min	**Nom**	**Max**		
VDD	Amplifier DC Supply		23		V	$I_{DD} \leq$ +15mA /pin, depending on Rout. See note 1
VRD	Reset Drain		16		V	See note 1
VOFD	Overflow Drain		16		V	See note 2
VSRC	Current source (“signal gnd”) from amplifier 1st & 2nd stages		2.5		V	$I_{SRC} \cong$ -1.5mA /pin
VGT	Bias voltage, amplifier 1st & 2nd-stage constant-current-source FETs		4		V	I_{GT} << 1nA /pin
VOG	Output Gate DC bias		-4		V	I_{OG} << 1nA /pin
VSS	Substrate [Ground]		0		V	
Rout	Output Load on each VOUT pin to VSS	0.75	1.0		kΩ	At 20MHz/output, use 1.0kΩ total of external load resistor + preamp input impedance

Note 1: Whenever VDD>+12V, VRD must be biased at not less than 12V less than VDD:

$$VRD \geq (VDD-12V) \text{ for all } VDD>+12V$$

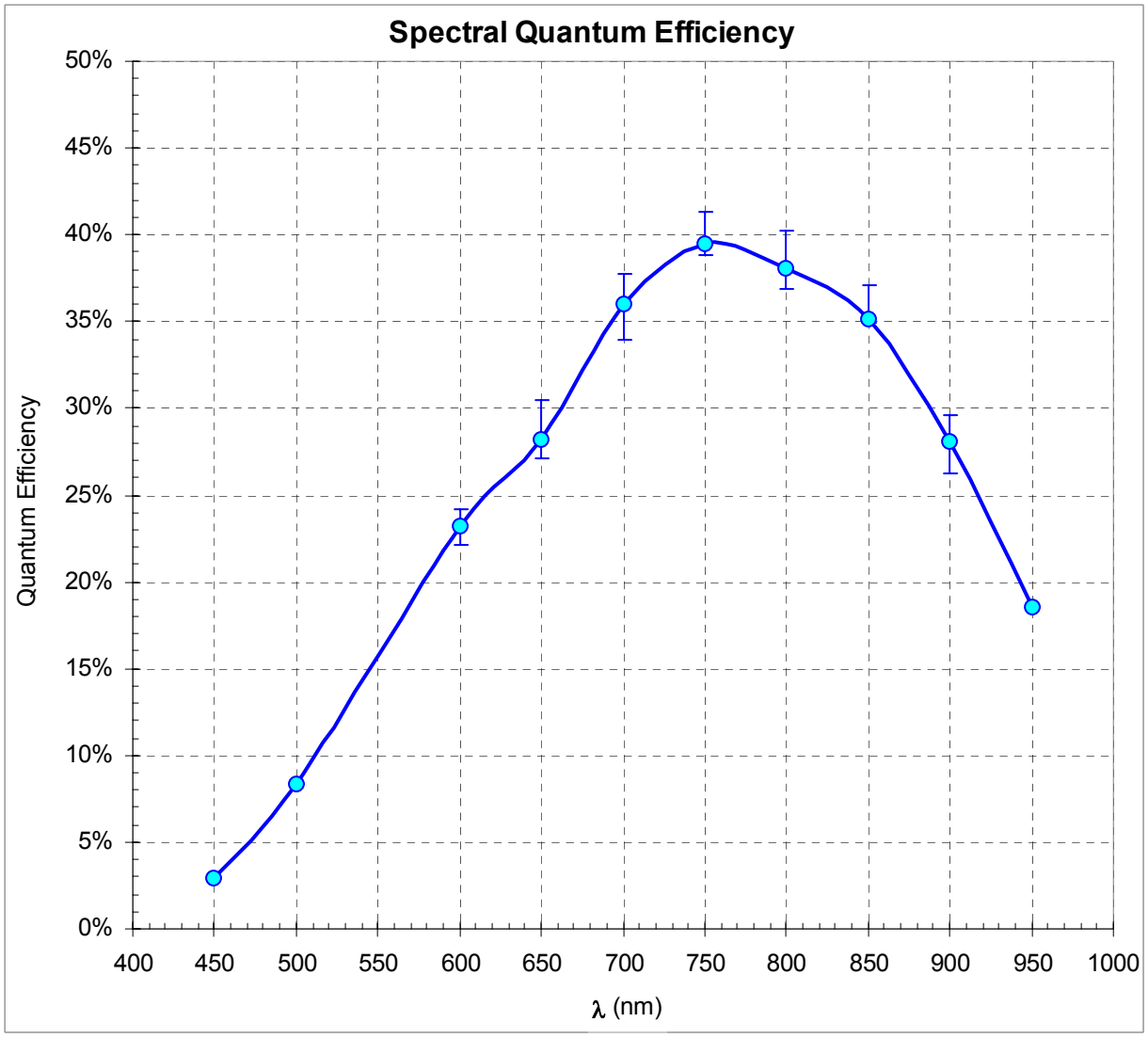
A zener diode circuit is recommended to ensure that this condition is always met. If this condition is not met, even momentarily, then permanent damage to the amplifier may result.

Note 2: (VRD-2V)<VOFD<(VRD+2V) If this condition is not met, even momentarily (for example, during power up or power down), then permanent damage to the CCD gates may result.

CCD5061 Clock Voltages						
Symbol	**Parameter**	**Range**			**Unit**	**Remarks**
		Min	**Nom**	**Max**		
V1	Slow vertical shift register clock					
V2	Clock-High		+18		V	
V3	Clock-Low		0		V	
	V-dump		+15		V	
V1-HS	Fast vertical shift register clocks					
V2-HS	Clock-High		+15		V	
V3-HS	Clock-Low		0		V	
	V-dump		+15		V	
H1	Horizontal shift register clock,					
	and V→H transfer clock					
	Trilevel (V→H transfer)		+5		V	
	Clock-High (transport only)		0		V	Note 1
	Clock-Low (transport only)		-5		V	Note 1
	H-dump		+3		V	
H2	Horizontal shift register clock					
H3	Clock-High		0		V	Note 1
H4	Clock-Low		-5		V	Note 1
	H-dump		+3		V	Note 1
ϕOG	Clocked output gate					
	Clock-High		1		V	Note 1
	Clock-Low		-5		V	Note 1
	H-dump		+3		V	
ϕR	Reset Gate Clock					
	Clock-High		+15		V	
	Clock-Low		+4		V	

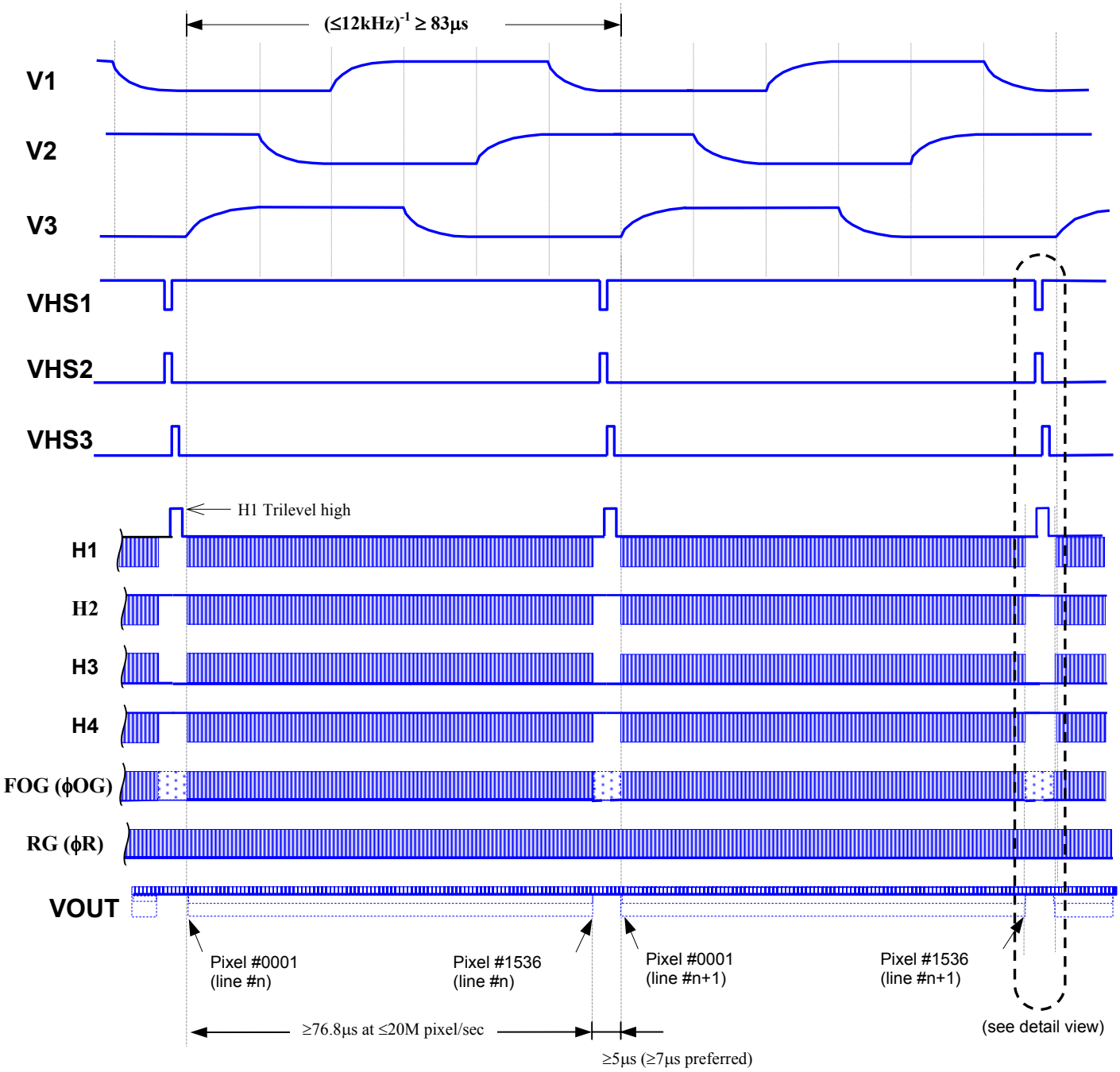
Note 1: May require individually tuned voltages for optimum performance especially at high speed.

CCD5061 Clock Capacitance						
Symbol	**Parameter**	**Range**			**Unit**	**Remarks**
		Min	**Nom**	**Max**		
Photosite rows: V1, V2, V3: capacitance per row						
	V1 to VSS		16		pF	
	V1 to V2		19		pF	
	V1 to V3		18		pF	
	V2 to VSS		24		pF	
	V2 to V3		22		pF	
	V3 to VSS		22		pF	
Isolation and high-speed rows: capacitance per row						
	V1 to VSS		20		pF	
	V1 to V2		19		pF	
	V1 to V3		18		pF	
	V2 to VSS		30		pF	
	V2 to V1 (see above)					
	V2 to V3		22		pF	
	V3 to VSS		31		pF	
	V3 to V1 (see above)					
	V3 to V2 (see above)					
Horizontal transport gate capacitance per 1536-element output section						
	H1		90	110	pf	Including inter-phase coupling capacitance (typical 50 pf)
	H2		90	110	pf	
	H3		90	110	pf	
	H4		110	130	pf	



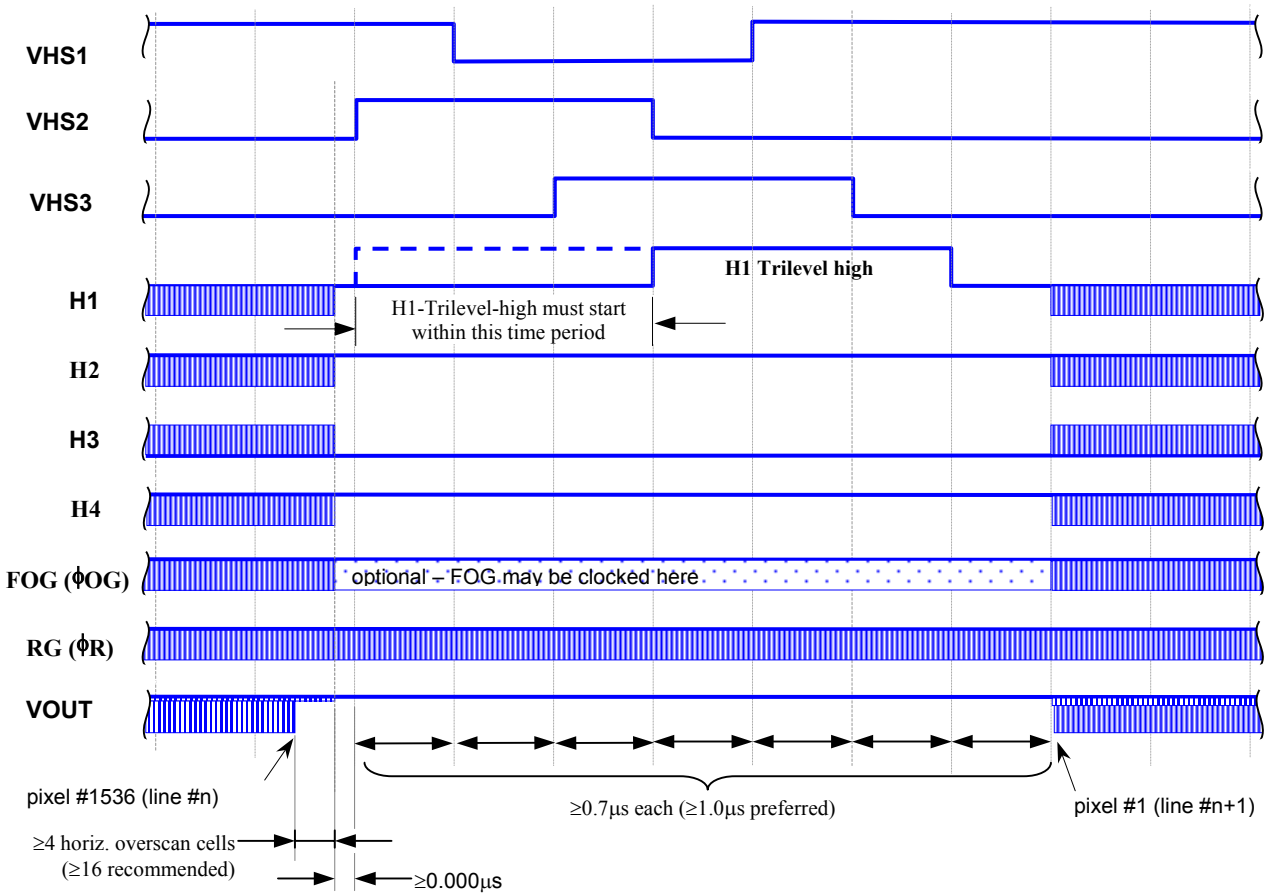
Typical QE Curve for CCD5061

Clock Timing Overview (1x1 full-resolution mode)

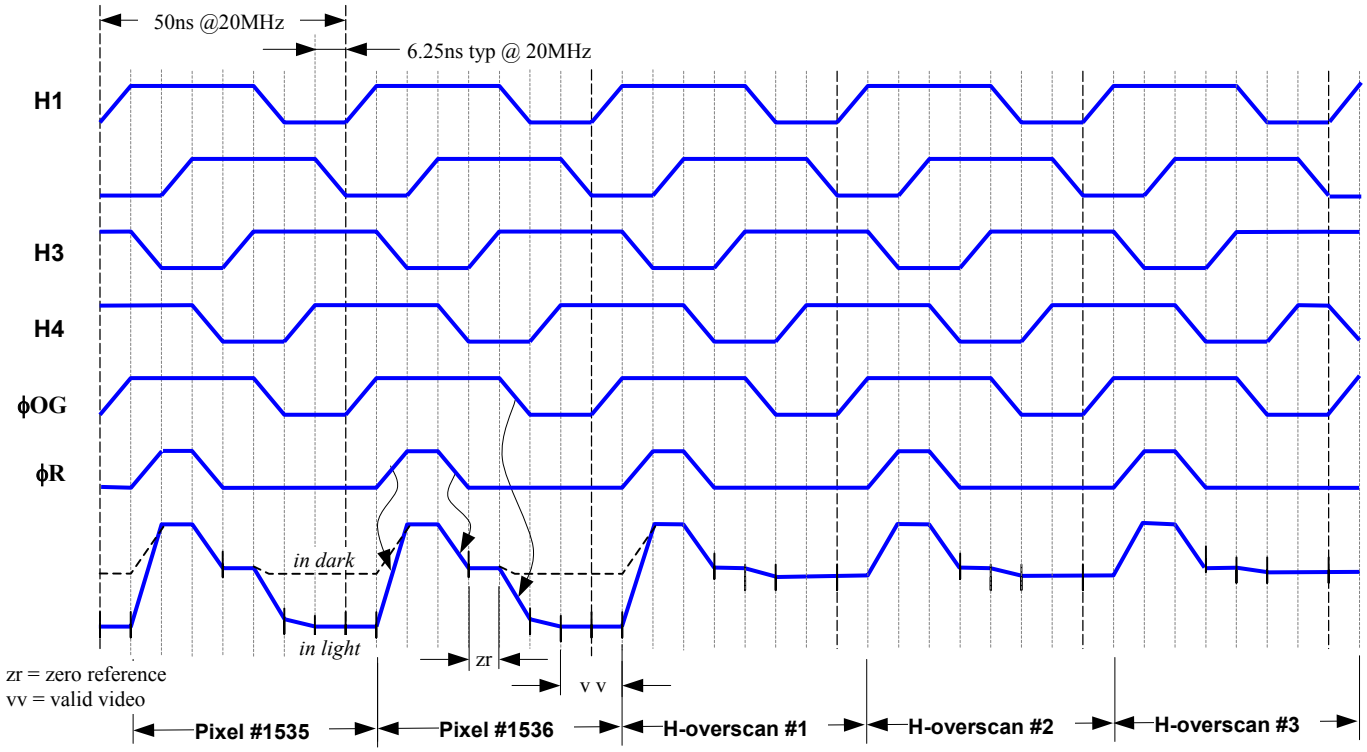


Note: For 12K-TDI, to maximize full well (QSAT) at (20MHz H-clocks, 12kHz V-clocks), use:
for V1 & V2: t_{RISE}(0%~90%) = t_{FALL}(100%~10%) = 4µs
for V3:……. t_{RISE}(0%~90%) = t_{FALL}(100%~10%) = 7µs

Vertical-to-Horizontal Clock Timing (1x1 full-resolution mode)



4-phase Horizontal Clock Timing (1x1 full-resolution mode)



CCD5061 Pin Name and Description

Pin Name	Signal Description	Remarks
VTG-T	Vertical Transfer Gate – Top	
V1HS-T	High Speed Vertical Shift Phase 1 Gates—Top, rows 1-3	
V2HS-T	High Speed Vertical Shift Phase 2 Gates—Top, rows1-3	
V3HS-T	High Speed Vertical Shift Phase 3 Gates—Top, rows 1-3	
V3X-T	Vertical Register Phase 3 – Top, isolation rows 1-18	
V1X-T	Vertical Register Phase 1 – Top, isolation rows 1-18	
V2X-T	Vertical Register Phase 2 – Top, isolation rows 1-18	
VSW12B-D	Vertical Register Phase 3 Gate - pixel row 1	Turn off for TDI-128 down
V1A-T	Vertical Register Phase 1 Gate - pixel rows 1-4	
V2A-T	Vertical Register Phase 2 Gate - pixel rows 1-4	
V3A-T	Vertical Register Phase 3 Gate - pixel rows 1-4	
VSW4-U	Vertical Register Phase 3 Gate - pixel rows 5	Turn off for TDI-4 up
V1C-T	Vertical Register Phase 1 Gate - pixel rows 5-8	
V2C-T	Vertical Register Phase 2 Gate - pixel rows 5-8	
V3C-T	Vertical Register Phase 3 Gate - pixel rows 6-8	
VSW8-U	Vertical Register Phase 3 Gate - pixel row 9	Turn off for TDI-8 up
V1D-T	Vertical Register Phase 1 Gate - pixel rows 9-16	
V2D-T	Vertical Register Phase 2 Gate - pixel rows 9-16	
V3D-T	Vertical Register Phase 3 Gate - pixel rows 10-16	
VSW16-U	Vertical Register Phase 3 Gate - pixel row 17	Turn off for TDI-16 up
V1E-T	Vertical Register Phase 1 Gate - pixel rows 17-32	
V2E-T	Vertical Register Phase 2 Gate - pixel rows 17-32	
V3E-T	Vertical Register Phase 3 Gate - pixel rows 18-32	
VSW32-U	Vertical Register Phase 3 Gate - pixel row 33	Turn off for TDI-32 up
V1F-T	Vertical Register Phase 1 Gate - pixel rows 33-64	
V2F-T	Vertical Register Phase 2 Gate - pixel rows 33-64	
V3F-T	Vertical Register Phase 3 Gate - pixel rows 34-64	
VSW64	Vertical Register Phase 3 Gate - pixel row 65	Turn off for TDI-64 up/down
V1F-B	Vertical Register Phase 1 Gate - pixel rows 65-96	

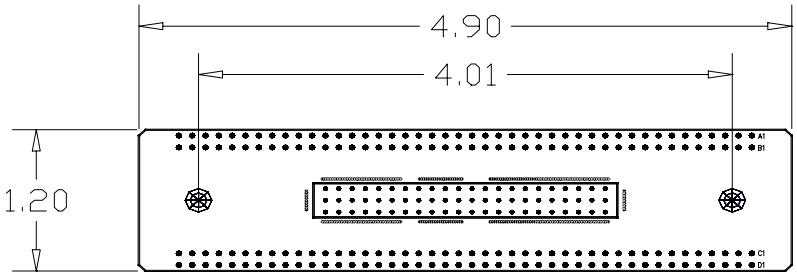
Pin Name	Signal Description	Remarks
V2F-B	Vertical Register Phase 2 Gate - pixel rows 65-96	
V3F-B	Vertical Register Phase 3 Gate - pixel rows 66-96	
VSW32-D	Vertical Register Phase 3 Gate - pixel row 97	Turn off for TDI-32 down
V1E-B	Vertical Register Phase 1 Gate - pixel rows 97-112	
V2E-B	Vertical Register Phase 2 Gate - pixel rows 97-112	
V3E-B	Vertical Register Phase 3 Gate - pixel rows 98-112	
VSW16-D	Vertical Register Phase 3 Gate - pixel row 113	Turn off for TDI-16 down
V1D-B	Vertical Register Phase 1 Gate - pixel rows 113-120	
V2D-B	Vertical Register Phase 2 Gate - pixel rows 113-120	
V3D-B	Vertical Register Phase 3 Gate - pixel rows 114-120	
VSW8-D	Vertical Register Phase 3 Gate - pixel row 121	Turn off for TDI-8 down
V1C-B	Vertical Register Phase 1 Gate - pixel rows 121-124	
V2C-B	Vertical Register Phase 2 Gate - pixel rows 121-124	
V3C-B	Vertical Register Phase 3 Gate - pixel rows 122-124	
VSW4-D	Vertical Register Phase 3 Gate - pixel row 125	Turn off for TDI-4 down
V1A-B	Vertical Register Phase 1 Gate - pixel rows 125-128	
V2A-B	Vertical Register Phase 2 Gate - pixel rows 125-128	
V3A-B	Vertical Register Phase 3 Gate - pixel rows 125-128	
VSW128-U	Vertical Register Phase 3 Gate - isolation row 1	Turn off for TDI-128 up
V1X-B	Vertical Register Phase 1 Gate—Bottom isolation rows 1-18	
V2X-B	Vertical Register Phase 2 Gate - Bottom isolation rows 1-18	
V3X-B	Vertical Register Phase 3 Gate - Bottom isolation rows 1-18	
V1HS-B	High Speed Vertical Shift Phase 1 Gates – Bottom rows 1-3	
V2HS-B	High Speed Vertical Shift Phase 2 Gates – Bottom rows 1-3	
V3HS-B	High Speed Vertical Shift Phase 3 Gates – Bottom rows 1-3	
VTG-B	Vertical Transfer Gate - Bottom	

Pinout Diagram

	A	B		C	D	
1	VSS	VSS		VSS	VSS	1
2	V1F-T	V2F-T		VSW64	V3F-B	2
3	V1E-T	V2E-T		VSW32-D	V3E-B	3
4	V1D-T	V2D-T		VSW16-D	V3D-B	4
5	V1C-T	V2C-T		VSW8-D	V3C-B	5
6	V1A-T	V2A-T		VSW4-D	V3A-B	6
7	V1HS-T	V2HS-T		VSW128-U	V3X-B	7
8	VTG-T	V3HS-T		V1X-B	V2X-B	8
9	ΦOG-T1, T2	ΦR-T1, T2		ΦR-B1, B2	ΦOG-B1, B2	9
10	N/C	VSS		N/C	AGND	10
11	N/C	N/C		N/C	N/C	11
12	AGND	N/C		VSS	N/C	12
13	H2-T1, T2	H3-T1, T2		H4-B1, B2	H1-B1, B2	13
14	VSRC-1	VSS		VRD-B1	AGND	14
15	VOUT-T1	VDD-T1		VDD-B1	VOUT-B1	15
16	AGND	VRD-T1		VGT-B	VOG-1	16
17	H1-T1, T2	H4-T1, T2		H3-B1, B2	H2-B1, B2	17
18	VSRC-2	VOFD-T		VRD-B2	AGND	18
19	VOUT-T2	VDD-T2		VDD-B2	VOUT-B2	19
20	AGND	VRD-T2		VSS	VOG-2	20
21	N/C	N/C		N/C	N/C	21
22	N/C	VSS		VSS	N/C	22
23	N/C	VSS		VSS	N/C	23
24	N/C	N/C		N/C	N/C	24
25	VOG-3	VSS		VRD-B3	AGND	25
26	VOUT-T3	VDD-T3		VDD-B3	VOUT-B3	26
27	AGND	VRD-T3		VOFD-B	VSRC-3	27
28	H2-T3, T4	H3-T3, T4		H4-B3, B4	H1-B3, B4	28
29	VOG-4	VGT-T		VRD-B4	AGND	29
30	VOUT-T4	VDD-T4		VDD-B4	VOUT-B4	30
31	AGND	VRD-T4		VSS	VSRC-4	31
32	H1-T3, T4	H4-T3, T4		H3-B3, B4	H2-B3, B4	32
33	N/C	VSS		N/C	AGND	33
34	N/C	N/C		N/C	N/C	34
35	AGND	N/C		VSS	N/C	35
36	ΦOG-T3, T4	ΦR-T3, T4		ΦR-B3, B4	ΦOG-B3, B4	36
37	V1X-T	V2X-T		V3HS-B	VTG-B	37
38	V3X-T	VSW128-D		V1HS-B	V2HS-B	38
39	V3A-T	VSW4-U		V1A-B	V2A-B	39
40	V3C-T	VSW8-U		V1C-B	V2C-B	40
41	V3D-T	VSW16-U		V1D-B	V2D-B	41
42	V3E-T	VSW32-U		V1E-B	V2E-B	42
43	V3F-T	VSW64		V1F-B	V2F-B	43
44	VSS	VSS		VSS	VSS	44

Package Diagram

BOTTOM VIEW



TOP VIEW

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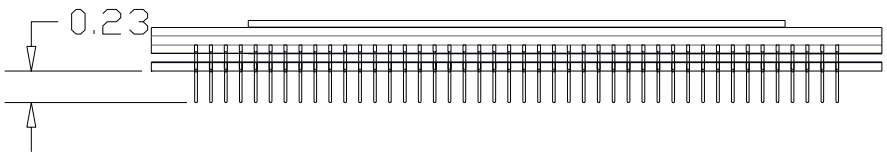

SIDE VIEW

COSMETIC GRADING
Device grading helps to establish a ranking for the image quality that a CCD will provide. Blemishes are characterized as spurious pixels exceeding 10% of V_{SAT} with respect to neighboring elements. Blemish content is determined in the dark, at various illumination levels and at different operating temperatures.

WARRANTY
Fairchild Imaging warrants that its products will be free of defects in material and workmanship under normal use and service for one year from date of shipment.

CERTIFICATION
Fairchild Imaging certifies that all products are carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specifications under which it is furnished.

This product is designed, manufactured and distributed utilizing the ISO 9000:2000 Business Management System

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