8BIT 250MSPS DAC BW2010D

GENERAL DESCRIPTION

This is CMOS 8-bit Triple D/A Converter for general applications.Its typical conversion rate is 250MHz and Supply voltage is 3.3V

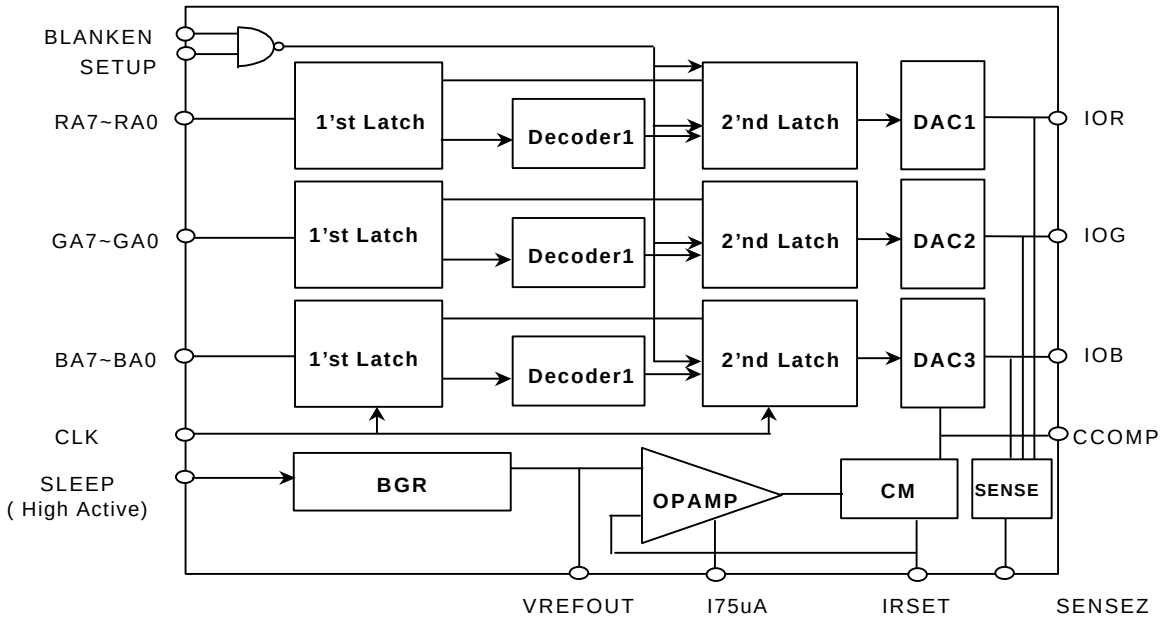
TYPICAL APPLICATIONS

- Graphic display
- Digital TV
- General purpose high-speed digital-to-analog conversion

FEATURES

- **250MHz Operation**
- **+3.3V power supply**
- **Optional 7.5IRE Mode**
- **BGR (Internal / External)**
- **RS-343A output level**
- **8bit Voltage parallel Input**
- **0 ~ 1V Output Swing**
- **Power Down mode(High active)**

FUNCTIONAL BLOCK DIAGRAM



CORE PIN DESCRIPTION

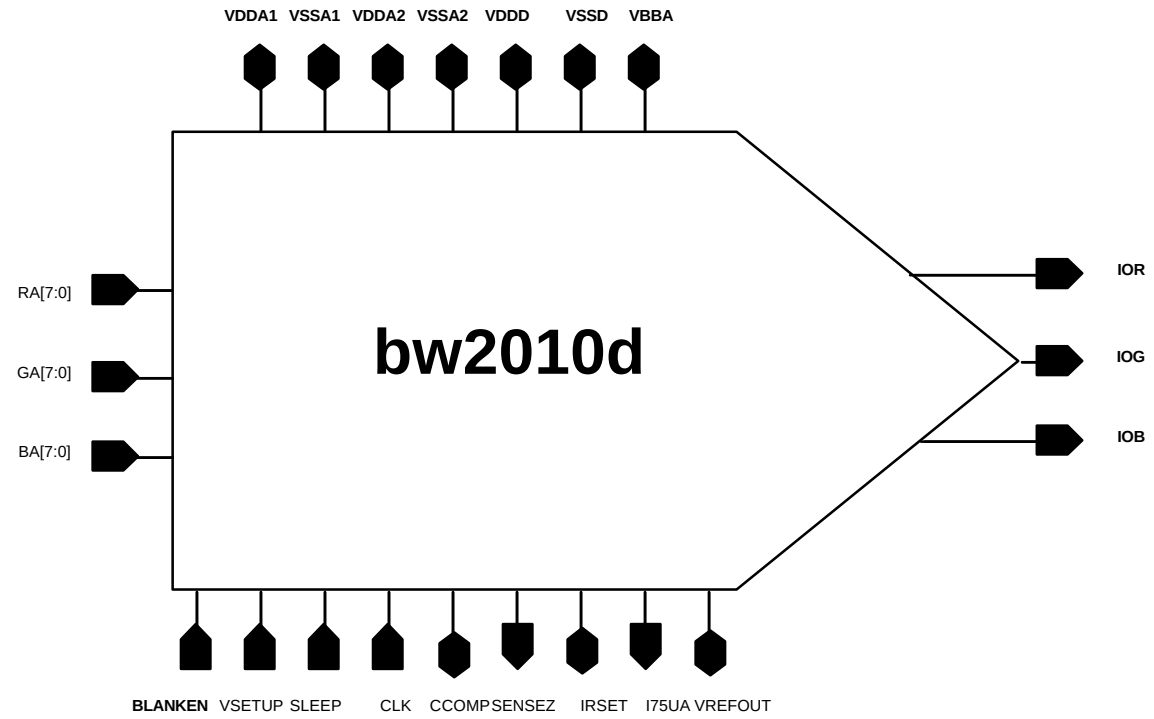
NAME	I/O TYPE	I/O PAD	PIN DESCRIPTION
IOR,IOG,IOB	AO	poa_bb_50option	Analog DAC output (Red,Green,Blue)
RA0:RA7	DI	picc_bb	Video signal RED Digital input
GA0:GA7	DI	picc_bb	Video signal GREEN Digital input
BA0:BA7	DI	picc_bb	Video signal BLUE Digital input
CLK	DI	picc_bb	Clock
SLEEP	DI	picc_bb	Power down mode (hign active)
VREFOUT	AB	poa_bb_50option	Reference voltage input & monitoring
CCOMP	AB	poa_bb_50option	External capacitance connection
I75uA	AO	poa_bb	RAM drive 150 [uA] (for RAMDAC)
SENSEZ	AO	poar50_bb	DAC output sensing (for RAMDAC)
IRSET	AB	poa_bb_50option	external resistor connection
VSETUP	DI	picc_bb	Blank enable pin
BLANKEN	DI	picc_bb	7.5 IRE level enable
VDDA1	AP	vdda	Analog Power
VDDA2	AP	vdda	Analog Power
VDDD	DP	vddd	Digital Power
VSSA1	AG	vssa	Analog Ground
VSSA2	AG	vssa	Analog Ground
VSSD	DG	vssd	Digital Ground
VBBA	AG	vbba	Analog Ground

I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Analog Output

- AP : Analog Power
- DP : Digital Power
- AG : Analog Ground
- DG : Digital Ground
- AB : Analog Bi-direction
- DB : Analog Bi-direction

CORE CONFIGURATION



FUNCTIONAL DESCRIPTION

This Core is 8bit 250MSPS digital to analog data converter and uses segment architecture for 4bits of MSB sides and binary-weighted architecture for 4bits of LSB side. It contains of First Latch Block, Decoder Block ,Second Latch Block, OPA Block, BGR Block, Switch Buffer Block, Sleep Block for power down, CM(current mirror) Block and Analog Switch Block. This core uses reference current to decide the 1LSB current size by dividing the reference current by 122times. So the reference current must be constant and the switch's physical real size can be constant by using OPA block with high DC gain. The most significant block of this core is analog switch block and it must maintain the uniformity at each switch, so Layout designer must care about the matching characteristics on analog switch and CM block. And more than 80% of supply current is dissipated at Analog Switch Block and OPA Block. And it uses samsung(SEC) standard cell as all digital cell of latch, decoder and buffer. And to adjust full current output, you must decide the "Rset" resistor value(connected to IRSET pin) and "Vbias" voltage value(connected to VREFOUT pin). Its voltage output can be obtained by connecting RL1(connected to IOR,IOG,IOB pin) .

Linearity Error : Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Monotonicity : A D/A converter is monotonic if the output either increases or remains constants as the digital input increases.

Offset Error : The deviation of the output current from the ideal of zero is called offset error. For IO , 0mV output expected when the inputs are all 0s.

Gain Errors : The difference between the actual andideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Output Compliance Range : The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown resulting in nonlinear performance.

Settling Time : The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition

Glitch Impulse : Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	SYMBOL	VALUES	UNIT
Supply Voltage	VDDA1 VDDA2 VDDA	-0.3 TO 7.0	V
Voltage on any Digital Voltage	Vin	VSSA-0.3 to VDDA+0.3	V
Storage Temperature Range	Tstg	-45 to 150	ºC

NOTES

1. It is strongly recommended that to avoid power latch-up all the supply Pins(VDDA1,VDDA2,VSSA1,VSSA2,VDDA,VSSA) be driven from the same source.

2. Absolute Maximum Rating values applied individually while all other parameters are within specified operating conditions. Function operation under any of these conditions is not implied.

3. Applied voltage must be current limited to specified range.

4. Absolute Maximum Ratings are value beyond which the device may be damaged permanently. Normal operation is not guaranteed.

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
Operating Supply Voltage	VDDA	3.15	3.3	3.45	V
Digital input Voltage HIGH LOW	Vih Vil	0.7VDDA -	- -	- 0.3VDDA	V
Operating Temperature Range	Topr	0	25	70	ºC

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
Resolution	-	-	8	-	Bits
Differential Linearity Error	DLE	-1	0.1	+1	LSB
Integral Linearity Error	ILE	-1	0.2	+1	LSB
Monotonicity	-	-	Guaranteed	-	-
White to Black Pedestral Voltage	-	0.55	0.6	0.65	V
Maximum Output Compliance	Voc	-0.3	-	+1.3	V
Exteranl Reference Voltage (option)	-	1.2	1.235	1.27	V
Internal BGR Reference Voltage	-	1.15	1.235	1.25	V
Power Supply Current	Is	60	66	67	mA

NOTES

1. White to Black Pedestal Voltage can be changed by using external RSET resistor
2. Converter Specifications (unless otherwise specified)
   VDDA=3.3V VSSA=GND
   Ta=25°C RL=37.5Ohm , VREFOUT=1.235V

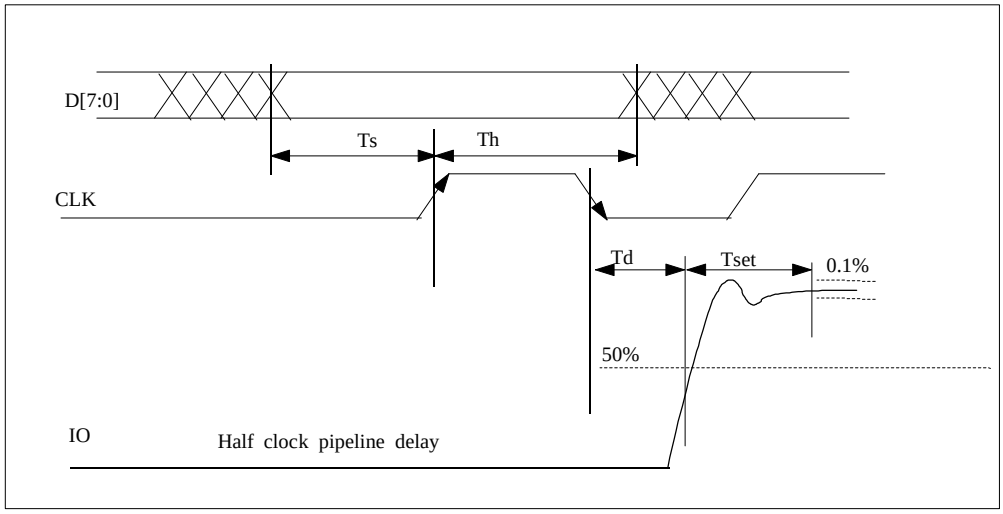
AC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
Conversion Speed	Fop	-	250	300	MHz
Analog Output Delay	Td	-	1	-	ns
Analog Output Rise Time	Tr	-	0.5	1	ns
Analog Output Fall Time	Tf	-	0.5	1	ns
Analog Output Settling Time	Ts	-	40	55	ns
Glitch Impulse	GI	-	50	70	pVsec
Feedthrough	fdth	17	18	-	dB
Setup Time	Ts	-	0.3	0.5	nsec
Hold Time	Th	-	0.3	0.5	nsec
Output Compliance	Voc	-0.3	-	1.3	V
THD(Total Harmonic Distortion)	THD	-	0.125	-	%
SNDR(Fin=6MHz , Fck=300MHz)	SNDR	44	47	-	dB

NOTES

1.The above parameters are guaranteed over the full temperature range.
2.Clock and data feed-through is a function of the amount of overshoot and undershoot on the digital inputs .Settling time does not include clock and data feed-through . Glitch impulse include clock and data feed-through.
3.Setup and Hold Time are simulation values, not a test result

TIMING DIAGRAM (FOR ONE CHANNEL)



NOTES

1. Output delay measured from the 50% point of the rising edge of CLK to the full scale transition
2. Settling time measured from the 50% point of full scale transition to the output remaining within ±1, ±2LSB.
3. Output rise/fall time measured between the 10% and 90% points of full scale transition.
4. Power Down On Time : 5.5us , Power Down Off Time : 5.5ms

TIMING DIAGRAM (FOR ONE CHANNEL)

R/G/B output			
7.5 IRE disable		7.5 IRE enable	
mA	V	mA	V
17.6	0.66	19.04	0.714
0	0	1.44 0	0.54 0

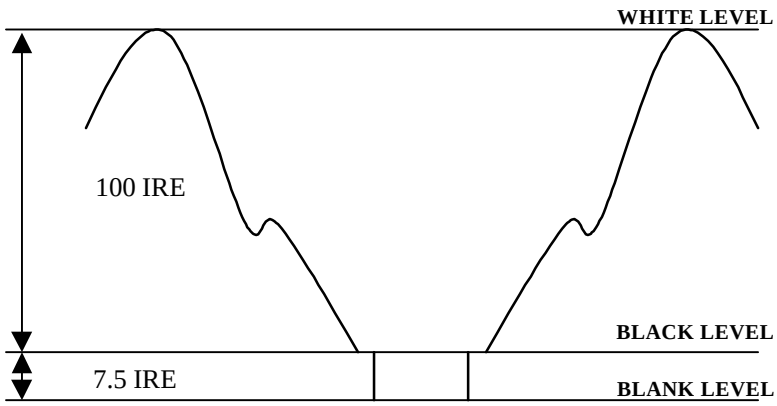
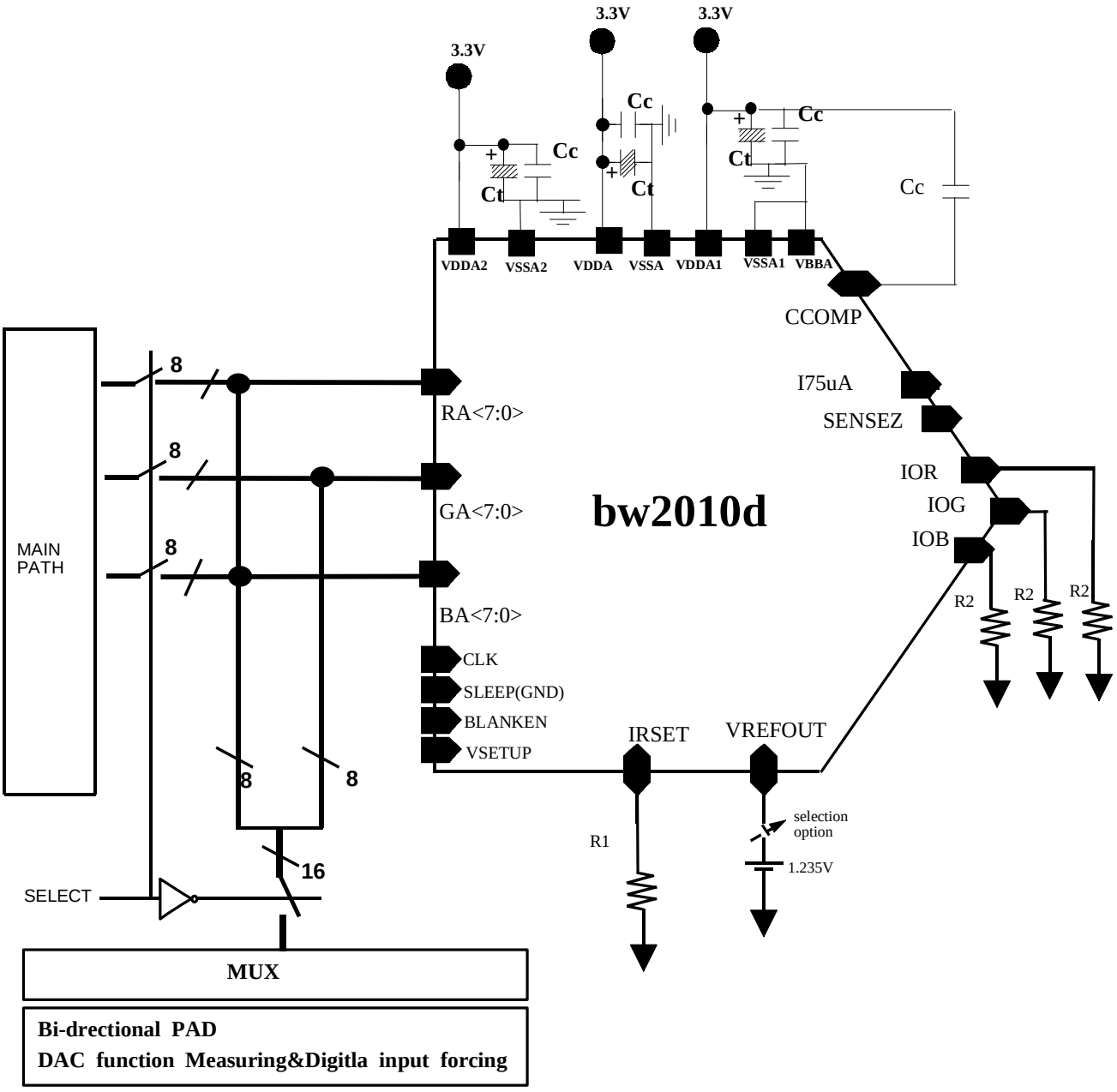


Figure2. RGB video output

NOTE:
1. OUTPUT CONNECTED TO A DOUBLY TERMINATED 75Ω LOAD
2. Vref =1.23V Rset=1.27 KΩ

7.5 IRE FUNCTION (FOR EACH CHANNEL)

BINARY INPUT				DAC OUTPUT CURRENT(mA) RL = 37.5 Ohm
VSETUP	BLANKEN	DATA	CODE	R,G,B channel
0	0	000H 3FFH	0 1023	1.44 19.04
1	0			
0	1			
1	1	000H 3FFH	0 1023	0 17.6



LOCATION	DESCRIPTION
Cc	0.1uF
R1	147 Ohm
R2	37.5 Ohm
Ct	10uF
Cc	0.1uF

1.Testability

Whether you use MUX or the internal logic for testability, it is required to be able to select the values of digital inputs ,TEST PATH block 16pins. See above figure. Only if it is, you can check the main function (Linearity) and output (IOR,IOG,IOB), VREFOUT ,IRSET and CCOMP pins are reserved for external use.

2. Analysis

The voltage applied to VREFOUT is measured at IRSET node . And the voltage value is proportioned to the reference current value of resistor which is connected to IRSET node. So you can estimate the full scale current value by measuring the voltage, and check the DC characteristics of the OPAMP. For reference, as VREFOUT applied to CCOMP node is given at IRSET node, the current flowing through IRSET is given as VREFOUT/RSET. The voltage is scaled factor of 1/122 for VIDEO. The full scale current is given as the decimal value equivalent to the digital code.

***Resolution**

If you want to change the resolution, use as many appear bits as you want and connect the rest lower bits to the ground as above diagram which is 8bit application.

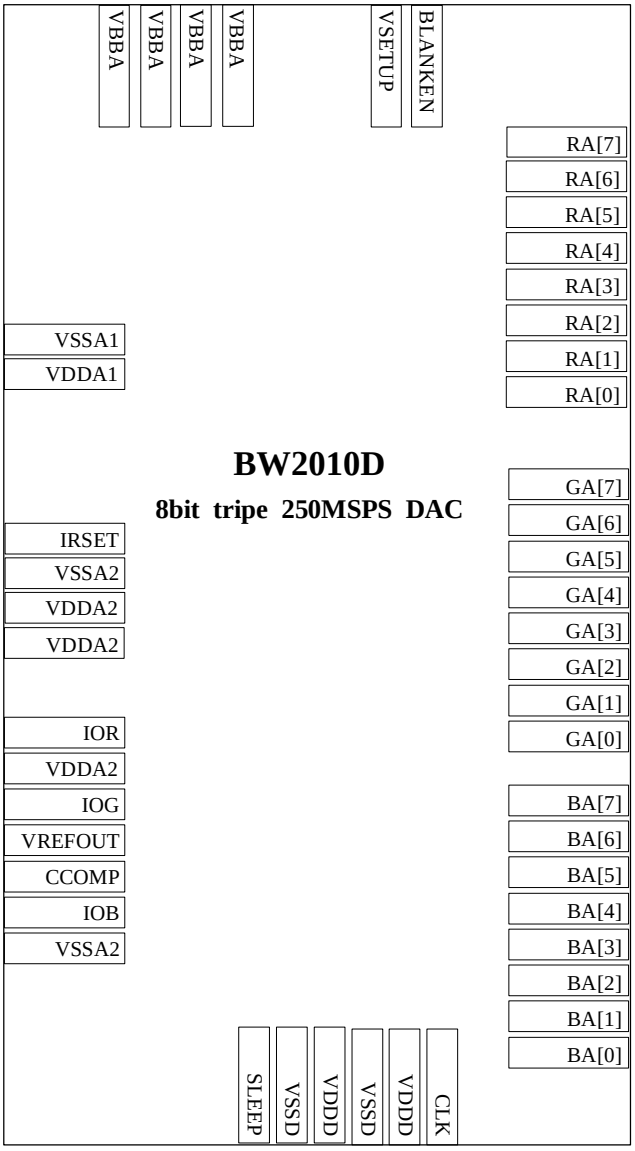
***Output Range Alteration**

In order to change the output swing, use following equation.

Vout = { VREFOUT/(RSET´122)}´DAC_CODE´Rio

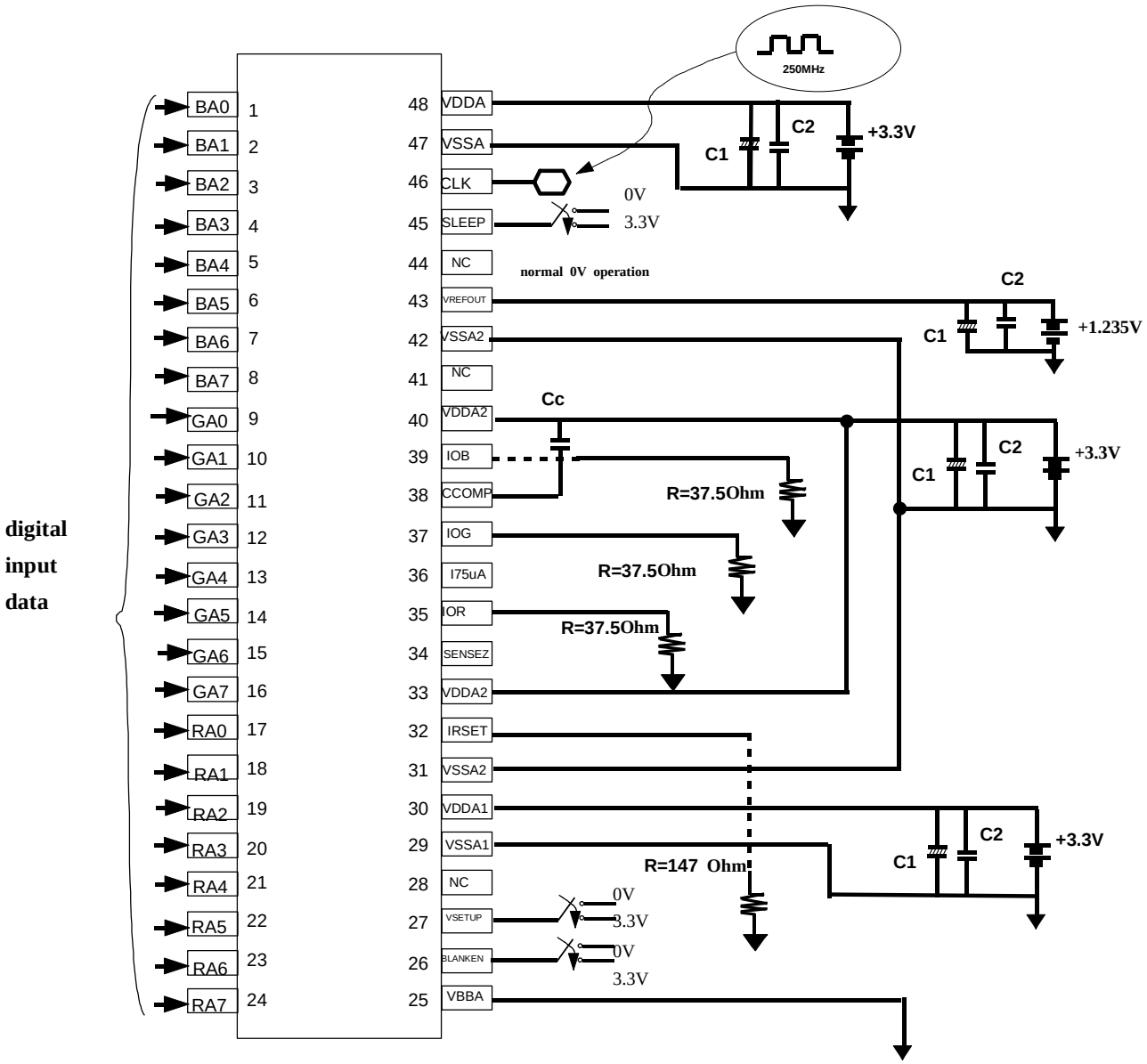
PHANTOM CELL INFORMATION

- Pins of the core can be assigned externally (Package pins) or internally (internal ports) depending on design methods.
  The term "External" implies that the pins should be assigned externally like power pins.
  The term "External/internal" implies that the applications of these pins depend on the user.



Pin Name	Pin Usage	Pin Layout Guide
VDDD	External	- Maintain the large width of lines as far as the pads. - place the port positions to minimize the length of power lines. - Do not merge the analog powers with another power from other blocks. - Use good power and ground source on board.
VSSD	External	
VBBA	External	
VDDA1	External	
VSSA1	External	
VDDA2	External	
VSSA2	External	
CCOMP	External/Internal	- Do not overlap with digtal lines.
VREFOUT	External/Internal	- Maintain the shortest path to pads.
IREF	External/Internal	- Separate from all other analog signals
IOR	External/Internal	- Maintain the larger width and the shorter length as far as the pads. - Separate from all other digital lines.
IOG	External/Internal	
IOB	External/Internal	
SLEEP	External/Internal	- Separated from the analog clean signals if possible. - Do not exceed the length by 1,000um.
BLANKEN	External/Internal	
VSETUP	External/Internal	
RA[7:0]	External/Internal	
GA[7:0]	External/Internal	
BA[7:0]	External/Internal	

PACKAGE CONFIGURATION



LOCATION	DESCRIPTION
Cc	0.1uF TANTALUM CAPACITOR
C1	10uF CAPACITOR
C2	0.1uF CERAMIC CAPACITOR
Rio	37.5 ohm 1% RESISTOR
RSET	147 ohm 1% METAL FILM RESISTOR

NOTES

1. Analog and digital supplies should be separated and de-coupled.
2. Supplies are not connected internally
3. All ground pins must be connected. One ground plane is preferred although it depends on the application

PACKAGE PIN DESCRIPTION

	NO	I/O TYPE	DESCRIPTION
BA<0:7>	1~8	DI	Video signal BLUE Digital input
GA<0:7>	9~16	DI	Video signal GREEN Digital input
RA<0:7>	17~24	DI	Video signal RED Digital input
VREFOUT	43	AI	Reference voltage input & monitoring
IRSET	32	AI	external resistor connection
SLEEP	45	DI	Power down mode (hign active)
BLANKEN	26	DI	Blank enable pin
VSETUP	27	DI	7.5 IRE level enable
CLK	46	DI	Clock
I75uA	36	AO	RAM drive (150 [uA])
CCOMP	38	AI	External capacitance connection
SENSEZ	34	AO	DAC output sensing
IOR	35	AO	Analog Voltage Output
IOG	37	AO	Analog Voltage Output
IOB	39	AO	Analog Voltage Output
VDDA	48	DP	Digital Power
VSSA	47	DG	Digital Ground
VBBA	25	AG	Bulk Bias Ground
VDDA1	30	AP	Analog Power
VDDA2	33,40	AP	Analog Power
VSSA1	29	AG	Analog Ground
VSSA2	31,42	AG	Analog Ground

NOTES

1.I/O TYPE PP and PG denote PAD Power and PAD Ground respectively.

FEEDBACK REQUEST

We appreciate your interest in out products. If you have further questions, please specify in the attached form. Thank you very much.

Characteristics	Min	Typ	Max	Unit	Remarks
Supply Voltage				V	
Power dissipation				mW	
Resolution				Bits	
Analog Output Voltage				V	
Operating Temperature				ºC	
Output Load Capacitor				pF	
Output Load Resistor				Ohm	
Integral Non-Linearity Error				LSB	
Differential Non-Linearity Error				LSB	
Maximum Conversion Rate				MHz	

VOLTAGE OUTPUT DAC					
Reference Voltage TOP BOTTOM				V	
Analog Output Voltage Range				V	
Digital Input Format	Binary Code or 2's Complement Code				

CURRENT OUTPUT DAC					
Analog Output Maximum Current				mA	
Analog Output Maximum Signal Frequency				MHz	
Reference Voltage				V	
External Resistor for Current Setting(RSET)				Ohm	
Pipeline Delay				sec	

- Do you want to Power down mode?
- Do you want to Internal Reference Voltage(BGR)?
- Which do you want to Serial Input TYPE or parallel Input TYPE?

VERSION LIST

Version	Date	Modified Items	Comments
Ver 1..0	98.05.01	Original version published	
Ver 1.4	99.12.13	1. Test configuration correction 2. Font correction	
Ver 1.5	20.02.23	1. font correction 2. layout guide correction	
Ver 1.6	02.0420	Add item (Phantom cell guide)	