MOTOROLA
Semiconductor Products Sector

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MS140132KT

Advance Information

Short Haul Loop Dual PCM Codec-Filter/SLIC Chipset with SPI Interface

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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CONTENTS

Section 1
Overview

Section 2
Applications

Section 3
Pin Descriptions

Section 4
Functional Characteristics of the SH-POTS System

Section 5
Electrical Characteristics

Section 6
Detailed Programming Description

Section 7
Mechanical Specifications

FIGURES

TABLES

SECTION 1
OVERVIEW

1.1 INTRODUCTION: MC1420233 CODSP AND MC1430132 SHLIC

The MS140132KT chipset provides all the functions necessary to connect analog telephone sets or other analog terminals (telefax, answering machines, modems, etc.) into digital communication systems. It provides an economical solution for the traditional “BORS(C)HT” [Battery, Overvoltage, Ringing, Supervision, (Codec), Hybrid, Test] functions found in central-office exchanges, but is optimized for short-range communication [e.g., up to 500 m with 5 RENs (Ringer Equivalence Number) attached]. Virtually all system-dependent parameters can be set under software control, giving an unprecedented flexibility to the system integrator, as well as optimizing the system cost. The digital interface to the SH-POTS (Short Haul, Plain Old Telephone System) chipset uses the PCM/SPI interface. The system architecture has been designed to offer the most cost-effective solution for short haul systems, yet offers the full flexibility required to meet worldwide analog telephony standards. The MS140132KT chipset is also suitable for Q.552 applications.

The MS140132KT chipset comprises three devices (see Figure 1-1): a pair of high-voltage devices, the Short Haul Line Interface Circuit (SHLIC) which provides the signal and power interface to the analog lines (one per line), and a low-voltage CMOS, DSP-based dual codec/control device (CODSP) which provides all signal processing and control functions for up to two lines.

1.2 KEY FEATURES

- Digitally Programmable Transmission and Signalling Characteristics Meet Worldwide Specification Requirements
- Integrated Ringing: Sine or Trapezoid with Auto Cadence
- Metering Injection (12 or 16 kHz)
- Support On-Hook Transmission: ADSI, CLIP
- Battery Reversal
- Codec and AC Parameters (Z_{CO} and Hybrid) are Fully Programmable (A-Law or μ-Law)
- Tone Generators for Signalling and Testing
- Loop Current Control and Monitoring are Programmable
- Minimal External Components
- Codec and SLIC Functions for Two Lines

- Low-Cost POTS Interface for Short Range
- Flexible IDL Interface with Timeslot Assigner
- Test Support (Test Load Switch, Loopback, Tone Generators)
- Supports up to –72 V on V_{BAT} Ring and –35 V on V_{BAT} Speech
- CODSP (Dual Codec) is 3.3 V with 5 V Tolerant Input for Low Power Consumption
- PCM Interface with Clock Frequency from 512 kHz to 8192 kHz in Steps of 512 kHz, Programmable up to128 Channels for Speech
- SPI Interface with Clock Frequency up to 8192 kHz to Control the PCM and SH-POTS Functions
- One Programmable Output Per Line for Signaling (Default: Off-Hook Detection)

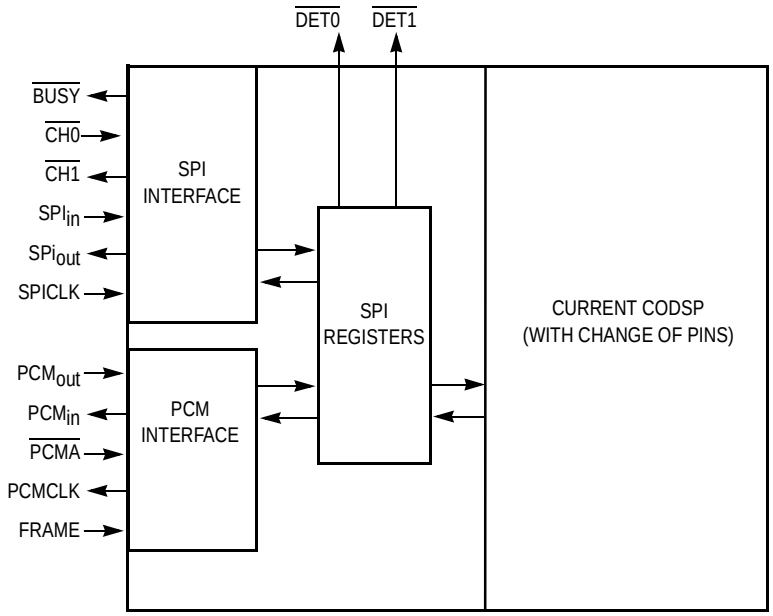


Figure 1-1. Block Diagram

SECTION 2
APPLICATIONS

Figure 2-1 shows a typical SH-POTS application using Motorola semiconductor chip solutions. The short haul dual PCM chipset provides all necessary functions to connect analog telephone sets or fax terminals to digital communications systems.

- Advanced ISDN NT (NTplus), Smart NT1 Personal Router
- Analog/Digital PABX
- Cable Telephone Systems (Set-Top Box)
- Remote Telephone Access Systems
  - — Fiber to the Curb
  - — Radio in the Loop
- Internet Telephones

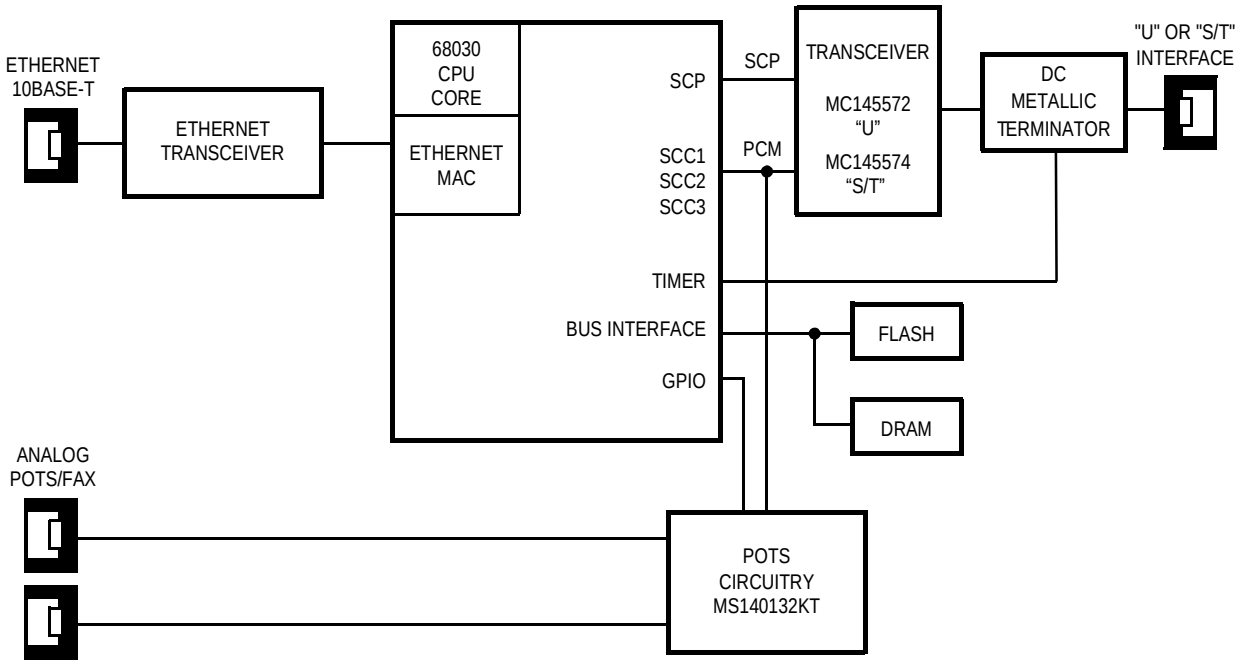


Figure 2-1. Typical SH-POTS Application

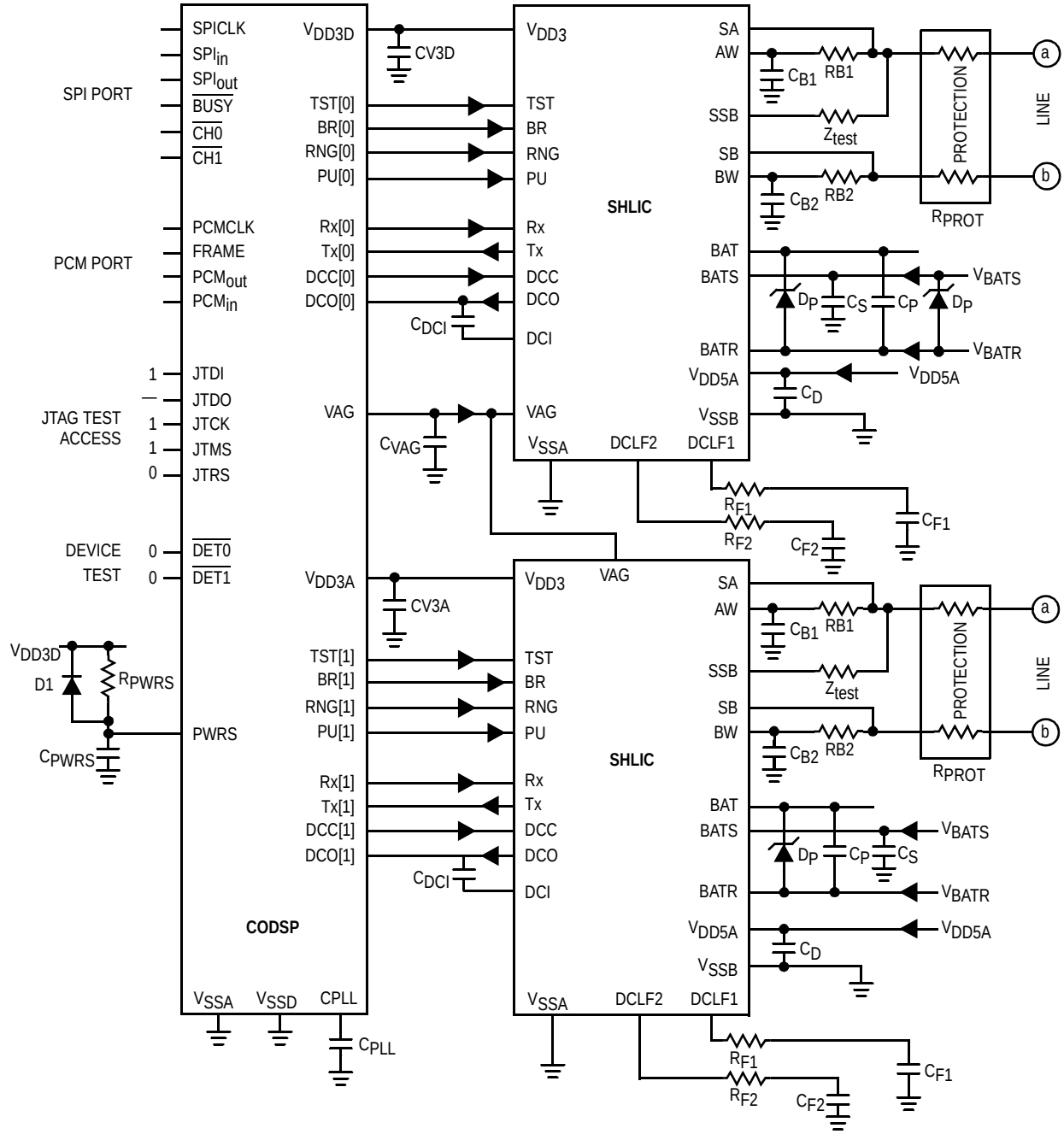


Figure 2-2. Application Schematic for Two Analog Lines

2.1 RECOMMENDED EXTERNAL COMPONENTS

Table 2-1. Recommended External Components

Component	Function	x	Comment
R_{B1}, R_{B2}	Feed resistor	50 Ω	1/4 W ±1% (see Note 1)
R_{PROT}	Protection resistance	2 x 10 Ω	
Z_{test}	Test resistor	510 Ω	1/4 W, optional
R_{F1}, R_{F2}	DC bias filter	10 kΩ	
C_{B1}, C_{B2}	No-load stabilization	1 nF	100 V (see Note 2)
C_{DCI}	DC feed separation	330 nF	5%
C_{F1}, C_{F2}	DC bias filter	470 nF	100 V, 10%
C_{VAG}	Analog ground decoupling	100 nF	
CV3A	Analog 3.3 V regulator decoupling	10 µF + 100 nF	
CV3D	Digital 3.3 V decoupling	10 µF + 100 nF	
C_S	Battery supply decoupling	100 nF	100 V
C_{PLL}	PLL loop filter	4.7 nF	
C_{PWRS}	Power-on reset delay	100 nF	
R_{PWS}	Power-on reset delay	100 kΩ	
D_1	Power loss reset	—	Any small signal diode
D_P	Battery input protection	—	BAT46 required depending on the power supplies
C_D	5 V power supply decoupling	100 nF	

NOTES: 1. A ±1% results in a maximum longitudinal balance of 40 dB. For higher values, more precise matching is required (e.g., ±0.1% for 46 dB).

2. Capacitors are generally not required. They are foreseen to stabilize the line driver outputs when active but driving no load (test condition only).

2.2 OVERVOLTAGE PROTECTION

There are several recommended overvoltage protection options. The application will determine the most appropriate one to chose (e.g., in-house only systems with minimal protection requirements, or systems with loops outside a protected environment requiring more extended protection).

The first external protection network to protect the line circuit against foreign voltages consist of resistors R_{PR1} and R_{PR2} and an overvoltage protection component (see Figure 2-3). Series resistors R_{PR1} and R_{PR2} can be PTC, poly-switch, or fusible components.

For further protection, the simplest and cheapest solution is a diode bridge between SA, SB and V_{SSB}, BATR, respectively. The diodes must be able to allow current peaks more than 20 A.

In case the battery BATR can not accept these high current peaks, add a voltage clamping component to V_{SS}, or a transient suppressor between each line and V_{SS}. The clamp voltage or protection voltage minimum must always be larger than the maximum used ringing battery BATR.

The protection components must be dimensioned in such a way that the transient energy on the chip pins AW, BW does not exceed 1 mJoule (or, the energy on-chip because of one lightning pulse).

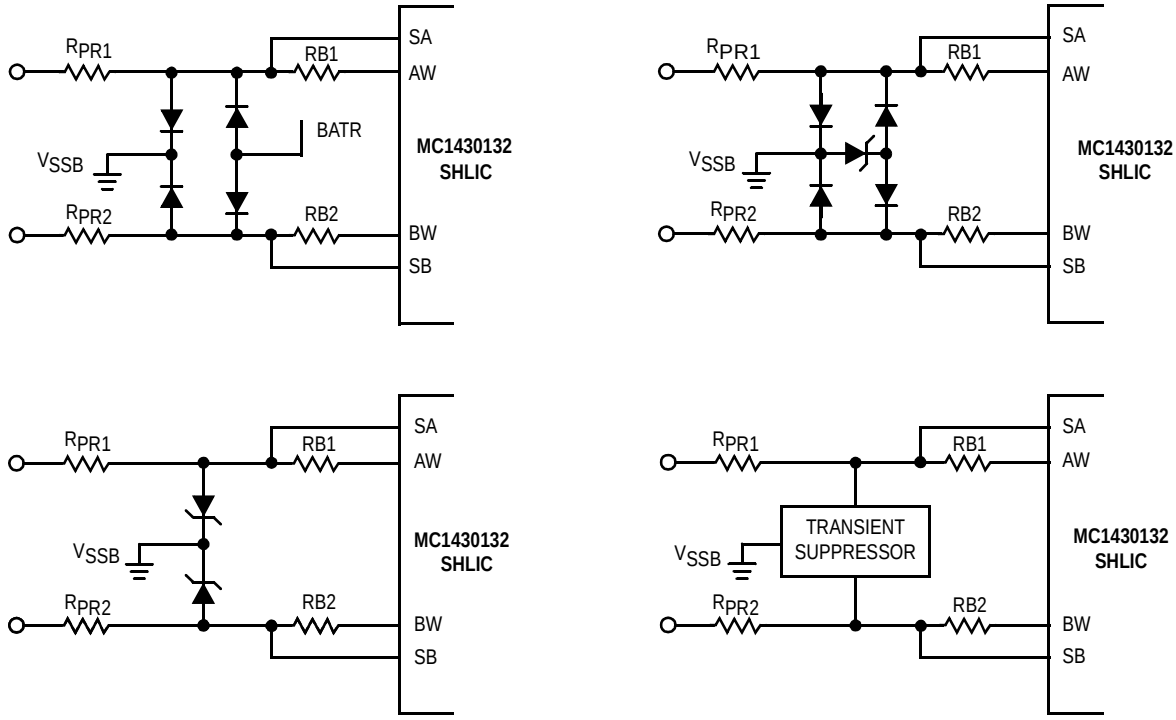


Figure 2-3. Recommended Overvoltage Protection Options

SECTION 3
PIN DESCRIPTIONS

3.1 DEVICE PINOUTS

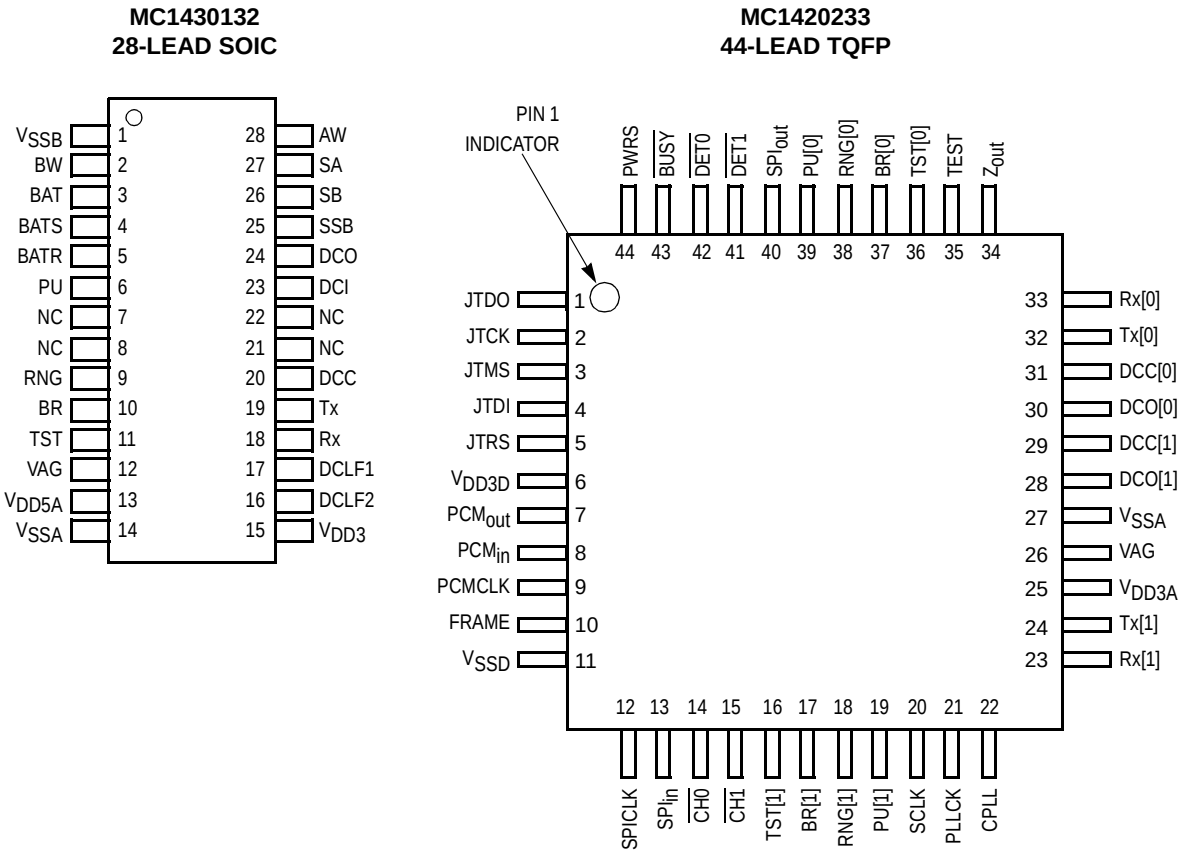


Figure 3-1. Pin Assignments

3.2 MC1420233 PIN DESCRIPTIONS

Table 3-1. Pin Descriptions for MC1420233 CODSP

Pin Name	Pin No.	Pin Description	Type (See Note)
JTDO	1	JTAG test port data out	DO
JTCK	2	JTAG test port clock	DIu
JTMS	3	JTAG test port mode select	DIu
JTDI	4	JTAG test port data in	DIu
JTRS	5	JTAG test port reset	DIu
V_{DD3D}	6	Digital section supply voltage	P
PCM_{out}	7	Three-state PCM transmit data output that is enabled based on FRAME	DO5
PCM_{in}	8	PCM receive data input, which is shifted into the CODSP following a programmed delay on the FRAME leading edge	DI5
PCMCLK	9	2.048 MHz clock input	DI5
FRAME	10	Transmits and receives frame sync pulse for line 0	DI5
V_{SSD}	11	Digital ground (0 V)	P
SPICLK	12	2.048 MHz control clock input	DI5
SPI_{in}	13	Bit serial data input	DI5
$\overline{CH0}$	14	Line 0 select, when $\overline{CH0}$ = 0, the SPI_{out} returns the data and the 8-bit control and programming data can input to the CODSP to control line 0 via SPI_{in}, when $\overline{CH0}$ goes from low to high, the data is latched	DI5
$\overline{CH1}$	15	Line 1 select, same functionality as $\overline{CH0}$	DI5
TST[1]	16	SHLIC 1 test select	DO
BR[1]	17	SHLIC 1 bat reverse control	DO
RNG[1]	18	SHLIC 1 ring control	DO
PU[1]	19	SHLIC 1 power-up control	DB
SCLK	20	System clock (test only)	DI
PLLCK	21	PLL clock (test only)	DIs
CPLL	22	PLL loop filter capacitor	AO
Rx[1]	23	SHLIC 1 Rx analog signal	AO
Tx[1]	24	SHLIC 1 Tx analog signal	AI
V_{DD3A}	25	Analog supply voltage	P
VAG	26	Analog ground reference voltage output	AO
V_{SSA}	27	Analog ground (0 V)	P
DCO[1]	28	SHLIC 1 DC loop output	AI
DCC[1]	29	SHLIC 1 DC loop control	AO

Table 3-1. Pin Descriptions for MC1420233 CODSP (continued)

Pin Name	Pin No.	Pin Description	Type (See Note)
DCO[0]	30	SHLIC 0 DC loop output	AI
DCC[0]	31	SHLIC 0 DC loop control	AO
Tx[0]	32	SHLIC 0 Tx analog signal	AI
Rx[0]	33	SHLIC 0 Rx analog signal	AO
Z_{out}	34	Digital I/O drive control (test only)	DB
TEST	35	Test mode select (test only)	DId
TST[0]	36	SHLIC 0 test select	DO
BR[0]	37	SHLIC 0 bat reverse control	DO
RNG[0]	38	SHLIC 0 ring control	DO
PU[0]	39	SHLIC 0 power-up control	DB
SPI_{out}	40	Bit serial data output	DO5
$\overline{DET1}$	41	On/off hook and ring trip detection output (line 1)	DO5
$\overline{DET0}$	42	On/off hook and ring trip detection output (line 0)	DO5
$\overline{BUSY}$	43	Indicates when a command is being executed	DO5
PWRS	44	Reset input	DIs

NOTE: The first letter differentiates between:
- D: Digital
- A: Analog
- P: Power

The second letter differentiates between:
- I: Input
- O: Output
- B: Bidirectional

The third letter differentiates between:
- d: Pin with internal pull-down
- u: Pin with internal pull-up
- s: Pin with Schmitt-trigger input
- 5: 5 V compatible input
- NC: No connect

3.3 MC1430132 PIN DESCRIPTIONS

Table 3-2. Pin Descriptions for MC1430132 SHLIC

Pin Name	Pin No.	Pin Description	Type
V_{SSB}	1	Battery ground (0 V)	P
BW	2	B wire output	AB
BAT	3	Battery voltage (output, do not connect)	P
BATS	4	Battery voltage input, SPEECH mode	P
BATR	5	Battery voltage input, RING mode	P
PU	6	Power-up control	DI
NC	7	Do not connect; thermal conduction pin	NC
NC	8	Do not connect; thermal conduction pin	NC
RNG	9	Ring mode control	DI
BR	10	Battery reverse control	DI
TST	11	Test mode control	DI
VAG	12	Analog ground reference input	P
V_{DD5A}	13	Analog supply voltage	P
V_{SSA}	14	Analog ground, 0 V	P
V_{DD3}	15	3 V regulator output	P
DCLF2	16	DC bias filter capacitor 2	AO
DCLF1	17	DC bias filter capacitor 1	AO
Rx	18	Analog receive signal	AO
Tx	19	Analog transmit signal	AI
DCC	20	DC loop control input	DI
NC	21	Do not connect; thermal conduction pin	NC
NC	22	Do not connect; thermal conduction pin	NC
DCI	23	DC loop control separation filter input	AI
DCO	24	DC loop control output	AO
SSB	25	Loop test resistor switch	AI
SB	26	B wire sense input	AI
SA	27	A wire sense input	AI
AW	28	A wire output	AB

NOTES: 1. A ±1% results in a maximum longitudinal balance of 40 dB. For higher values, more precise matching is required (e.g., ±0.1% for 46 dB).

2. Capacitors are generally not required. They are foreseen to stabilize the line driver outputs when active but driving no load (test condition only).

3.4 UNUSED PINS

3.4.1 CODSP

Table 3-3 lists the pins on the CODSP that are not connected. Pins that are not used in the application should be connected as described here. Failure to do so could result in excessive sensitivity to RFI or other erratic behavior. A 0 or 1 indicates that the pin should be connected to ground or to the device's digital supply. A "—" indicates that the pin is an output and must be left unconnected.

Table 3-3. MC1420233 CODSP
Unused Pin Connections

Pin Name	Pin No.	Connect To
JTDI	4	1 (V_{DD3D})
JTDO	1	—
JTCK	2	1 (V_{DD3D})
JTMS	3	1 (V_{DD3D})
JTRS	5	0 (V_{SS})
SCLK	20	V_{SS}
PLLCK	21	V_{SS}
Z_{out}	34	V_{SS}
TEST	35	V_{SS}

3.4.2 SHLIC

Table 3-4 lists the pins on the SHLIC that are not connected. The NC pins (7, 8, 21, and 22) are connected to the device substrate, which is at a voltage equal to the V_{BATR} supply pin, and may optionally be electrically connected to this pin.

Table 3-4. MC1430132 SHLIC
Unused Pin Connections

Pin Name	Pin No.	Connect To
BAT	3	No connect or see text above
NC	7	No connect or see text above
NC	8	No connect or see text above
NC	21	No connect or see text above
NC	22	No connect or see text above

The BAT pin is the internal supply to the line drivers, and adopts the voltage of V_{BATR} or V_{BATS}, plus the voltage drop across the internal switch, depending on the operating mode. In low-voltage only systems (very short connections), the BAT pins, V_{BATR} and V_{BATS}, may all be connected together and a single supply (e.g., –27 V) may be used for both ringing and speech modes. (In this mode, the voltage drop of the internal switches is avoided.)

3.5 NOTE ON DECOUPLING

As in any system, the PCB layout and supply decoupling can influence the system performance, particularly with respect to noise.

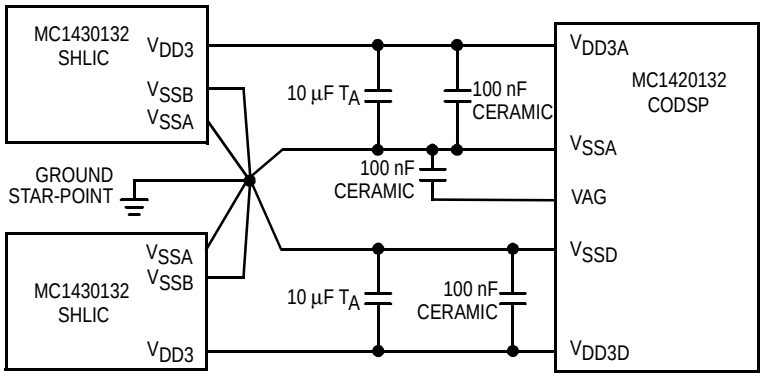
3.5.1 CODSP Decoupling

- It is recommended to connect V_{DD3D} and V_{DD3A} (digital and analog supply pins) in a star configuration from the supply (either from the SHLIC or from an external supply), and each pin be independently decoupled using 10 µF in parallel with 100 nF.

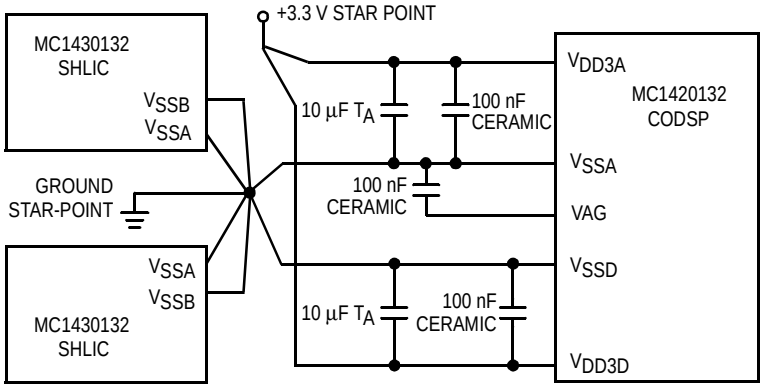
  In two-line systems, using the SHLIC regulator to supply only the CODSP (i.e., no other use is made of the regulator), one SHLIC may be used to provide V_{DD3D} power and the other V_{DD3A}, thus giving improved decoupling between analog and digital supplies. See Figure 3-2.
- The VAG line (analog signal reference) must always be properly decoupled using 100 nF, placed as close as possible to the CODSP device.

3.5.2 SHLIC Decoupling

- The SHLIC should use separate 100 nF decoupling capacitors between V_{DD5A} and V_{SSB}, and V_{DD5A} and V_{SSA}. When the on-board regulator of the SHLIC is not used, no capacitor is required at the V_{DD3} pin.



(a) Arrangement A



(b) Arrangement B

Figure 3-2. MC1420233 CODSP Recommended Power-Supply Decoupling Arrangements

SECTION 4
FUNCTIONAL CHARACTERISTICS OF THE SH-POTS SYSTEM

For reference, Figure 4-1 shows the typical voltages on tip and ring during various stages of operation. For detailed electrical parameters, refer to Section 5.

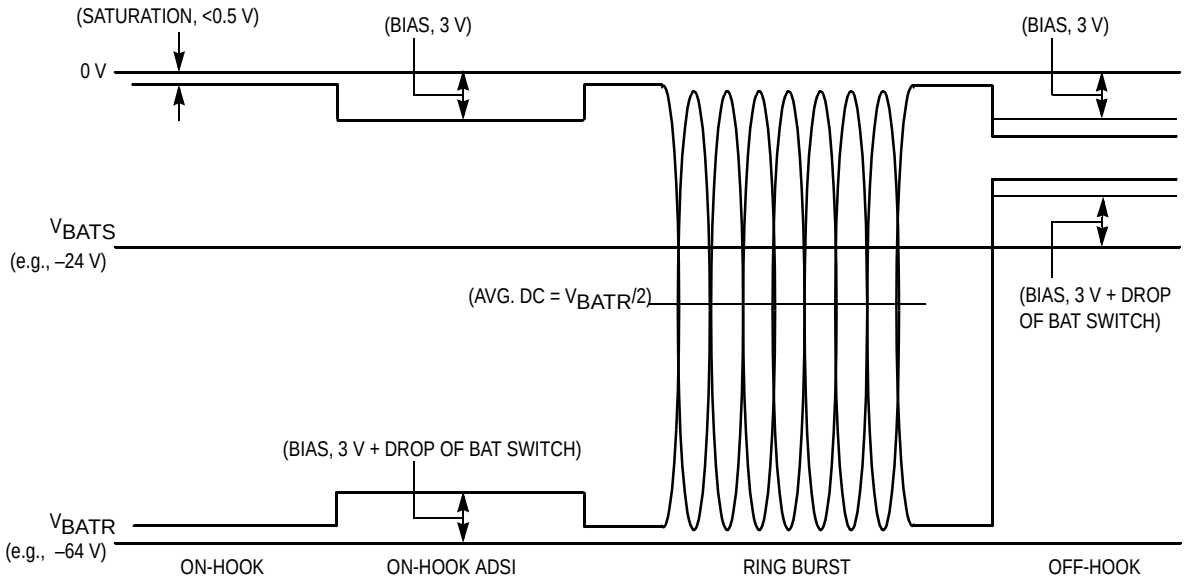


Figure 4-1. SH-POTS Line Voltages — Example

4.1 ON-HOOK CONDITIONS

When a line is not in use (on-hook), the designer may select either the speech battery or the ringing battery as the supply to the line drivers. In the on-hook mode, most of the internal circuits are put into a low-power operating mode to minimize supply currents. The A and B wire outputs are effectively connected to the supply voltage, thus applying this voltage (minus a small saturation voltage) to the line. The output is current-limited in this mode, thus protecting against short circuits and limiting any inrush current when a set goes off-hook. If the SHLIC detects a current in excess of a (programmable) limit, the off-hook

condition will be detected (an on-chip debouncer with selectable delay avoids accidental hookswitch detection), and the circuit will be put into active speech mode. The nominal off-hook detection currents and hysteresis are shown in Figure 4-2. When a line is in the on-hook condition, the system designer may select, under program control via the PCM/SPI bus, an “on-hook active mode,” whereby, on-hook signalling (ADSI, CLIP, etc.) can be performed in either direction (though battery reversal is not available in this mode).

The hookswitch detector has a programmable debounce timer. Times of 8, 16, 24, or 64 ms can be selected. (The timer is common for both channels.)

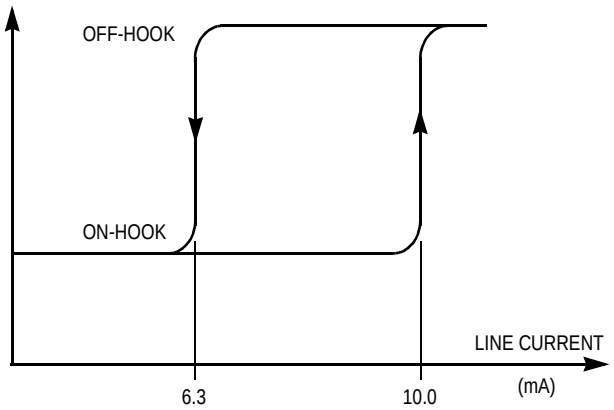


Figure 4-2. Nominal Hookswitch Detection Thresholds (Default Values)

Table 4-1. On-Hook Characteristics

Parameter	Condition	Min	Max	Unit	Note
V_{feedO}	Open-line feed voltage	V_{BATS-1}	V_{BATR-1}	V	1
I_{on}	Line current guaranteeing on-hook state	4.67	7.93	mA	2
I_{off}	Line current guaranteeing off-hook state	7.86	12.14	mA	2
I_{OHYST}	Hookswitch detect hysteresis	2	—	mA	2
I_{OC}	Peak over-current limit, on-hook mode	—	145	mA	3
V_{biasH} V_{biasL}	Bias voltage during ADSI mode on A (H) and B (L) wires, ref. BAT pin	2	4	V	

NOTES: 1. I_{line} = 0 mA, independent of battery reversal mode. This voltage is selected by the user. The output impedance when in the on-hook condition is set by the sense resistors R_{feed}. The hook-switch detector has a programmable debounce timer. Times of 8, 16, 24, or 64 ms can be selected (common for both channels).

2. These are the default values after reset. The on-hook and off-hook thresholds can be individually programmed in the range 0 to 63 mA nominal.

3. This is the intrinsic current limit of the output driver. This current can only be seen during on-hook to off-hook transients, or during ringing into a short-circuit load during the ring-trip delay period. The actual value measured will depend on the load resistance used.

4.2 RINGING INJECTION

4.2.1 Balanced Ringing

The SH-POTS chipset is capable of directly injecting a ringing signal of up to 50 Vrms (sine wave) without the need for additional external components. The technique of “balanced ringing” is used, which allows this large voltage swing to remain within the technology limits of the SHLIC device. (Balanced ringing requires a specific algorithm for ring-trip detection, which is also implemented by the chipset.) The SH-POTS chipset allows the user to program a dc offset during ringing as well as a reduced amplitude ringing signal, should the application require this. Ringing waveform, frequency, amplitude, and cadence, as well as ring-trip thresholds, are controlled by the CODSP device, and are all programmable. Ringing cadence can be automatic, with independently programmable ring and pause times, or ringing can be controlled directly via the PCM/SPI bus. In the automatic cadence mode, ringing bursts on both channels can be optionally interleaved, if simultaneously active, to avoid peaks in current from the ringing battery supply.

Table 4-2. Ringing Characteristics

Parameter	Condition	Min	Max	Unit	Note
F_R	Ringing frequency 16.66, 20, 25 Hz 50 Hz	 –1 –2	 1 2	Hz	
SF_{NR}	Single-frequency noise, 10 Hz to 4 kHz	—	–63	dBm	
V_R	Ringing voltage (max), V_{BATR} = –72 V	50	—	Vrms	1
D_R	Ringing distortion, sine mode 30 Hz to 132 kHz	—	5	%	
t_{RTD}	Ring-trip delay, load = 500 Ω + 4 μF	—	150	ms	
t_{RTDEB}	Ring-trip debounce time	0	30	ms	2
t_C	Ring-cadence times (active and silent)	1	255	n/n	4
I_{RTH}	Ring-trip current, high threshold	6.0	12.0	mA	3
I_{RTL}	Ring-trip current, low threshold	3.5	9.5	mA	3
H_{RT}	Ring-trip hysteresis	2	—	mA	3

NOTES: 1. Ringing voltage is user-programmable from 0 to 70 Vp(diff) between the A and B wires (NB, the ringing battery voltage must be large enough to encompass this voltage) in 256 steps. The default is the maximum value. Condition: Load = 0 mA.

2. User-selectable 0 or 30 ms. Default is 30 ms.

3. These are the default values after reset. The max and min ring-trip thresholds can be individually programmed in the range 0 to 63 mA nominal. The ring-trip detect mask time is used to bridge the zero-crossings of the ringing signal, and is programmable between 0 and 32 ms in 125 μs steps.

4. Units are periods of the selected ringing frequency. The default values are 1 s on, 3 s off, with a ringing frequency of 50 Hz.

4.2.2 Semi-Unbalanced Ringing

In order to support "semi-unbalanced ringing" (dc bias equal to V_{BATR} superimposed on the differential ringing signal), two of these outputs will be active high during the active ringing period on each channel (SPICK for channel 0 and SPICS for channel 1). This can be used to drive a relay via an external NPN transistor, as shown in Figure 4-3.

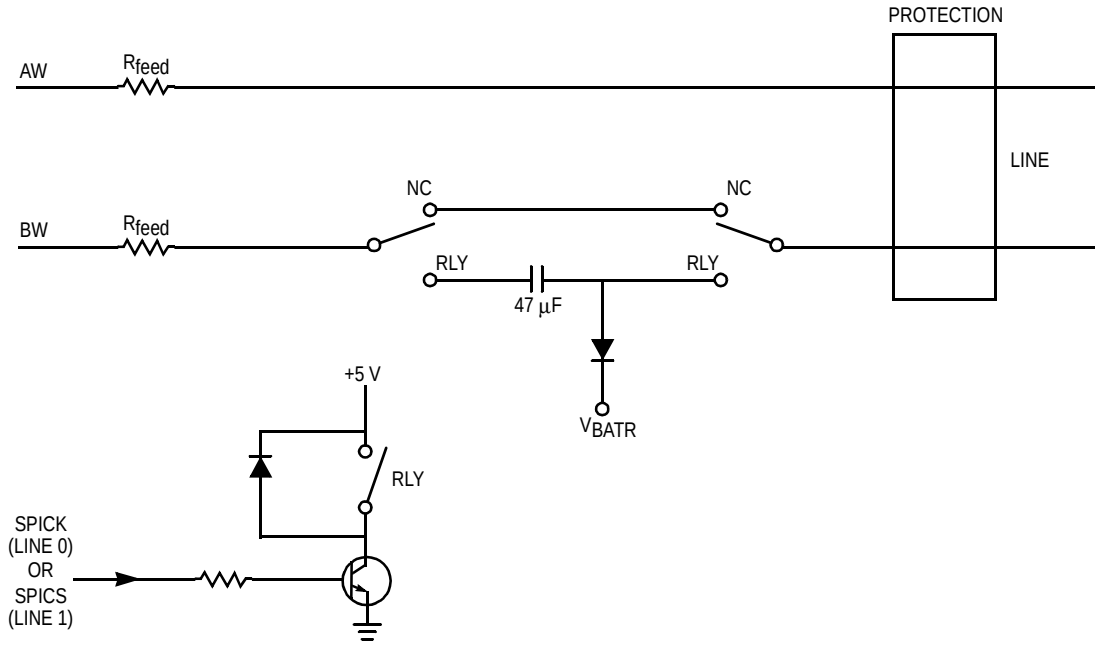


Figure 4-3. Application Suggestion for Semi-Unbalanced Ringing Injection

4.3 DC FEED CHARACTERISTICS

As shown in Figure 4-4, the SH-POTS chipset implements a constant-current feed. The limit current and the residual resistance (slope of the characteristic) are both programmable by the user. The dc characteristic falls into three regions. When the combination of line and subset result in a current less than the programmed limit current, the system behaves like a battery with a fixed feed resistance of 120 Ω, and a voltage equivalent to the speech supply voltage (V_{BATS}) minus the bias voltage on both lines (6 V nominal in total). Should line conditions permit a current that exceeds the programmed limit current, the system enters the constant-current feed mode described above. In order to protect the output stage in the transition region at higher line currents (in excess of 50 mA), a third region is defined, where the system synthesizes a fixed feed resistance of 200 Ω. The slope of the voltage/current characteristic in the constant-current mode can be user-programmed to select the effective feed-resistance.

NOTE

The SHLIC device includes over-temperature protection, that activates at 165°C in case of overheating of the device.

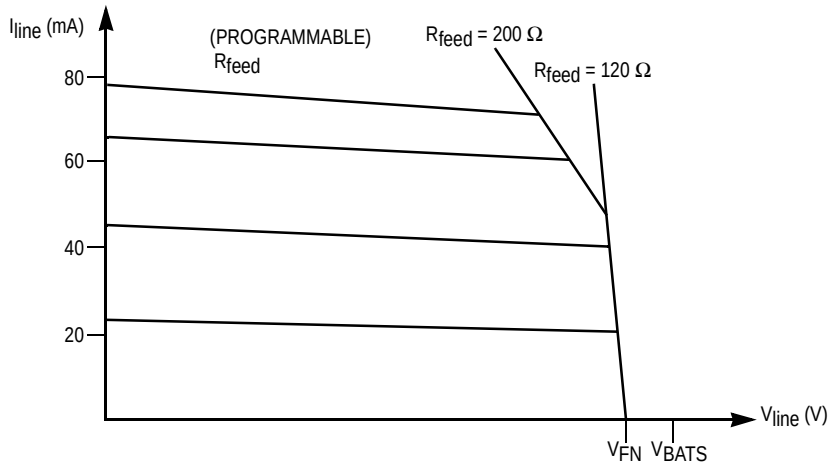


Figure 4-4. DC Feed Characteristics

Table 4-3. DC Feed Characteristics
[R_{feed} = 60 Ω Total (50 Ω +10 Ω Protection) x 2]

Parameter	Condition	Min	Max	Unit
V_{biasH}	Bias voltage, A wire (I_{line} = 0)	2.5	3.5	V
V_{biasL}	Bias voltage, B wire (I_{line} = 0)	2.5	3.5	V
TOL_{ICL}	Current limit tolerance	–15	15	%
$T_{RfeedCL}$	Tolerance on programmed R_{feed} when in current-limit	–15	15	%
I_{CL}	Current-limit, useful programmed range	20	70	mA

4.3.1 Battery Voltage and Reversal

The open-line voltage (i.e., the voltage seen on the line when on-hook) is user-selectable for each channel via an internal register. It can be either the ringing battery supply (most common use) or the speech battery supply. The speech battery supply is automatically selected when an off-hook condition is detected, independently of these control bits. The selected supply voltage is maintained when the on-hook signalling function (ADSI) is enabled.

The polarity of the line feed can be dynamically controlled by the user. In the “normal” condition, the A wire is the most positive. Thus, reversal makes the B wire the most positive. Battery reversal is fast (audible), is controlled by programming an internal register, and is independent for both channels. The selected polarity is used in all states (on-hook, off-hook, ringing, etc.) except for on-hook signalling, which is in normal battery mode.

4.4 AC TRANSMISSION CHARACTERISTICS (MS140132KT SYSTEM)

4.4.1 Transmit and Receive Filter Characteristics

The SH-POTS chipset implements transmit and receive filters according to ITU-T (G.712). These filters can be reprogrammed by the user for specific requirements. Please contact a Motorola sales office for more information. The implemented default filter characteristics are shown in Figures 4-5 and 4-6.

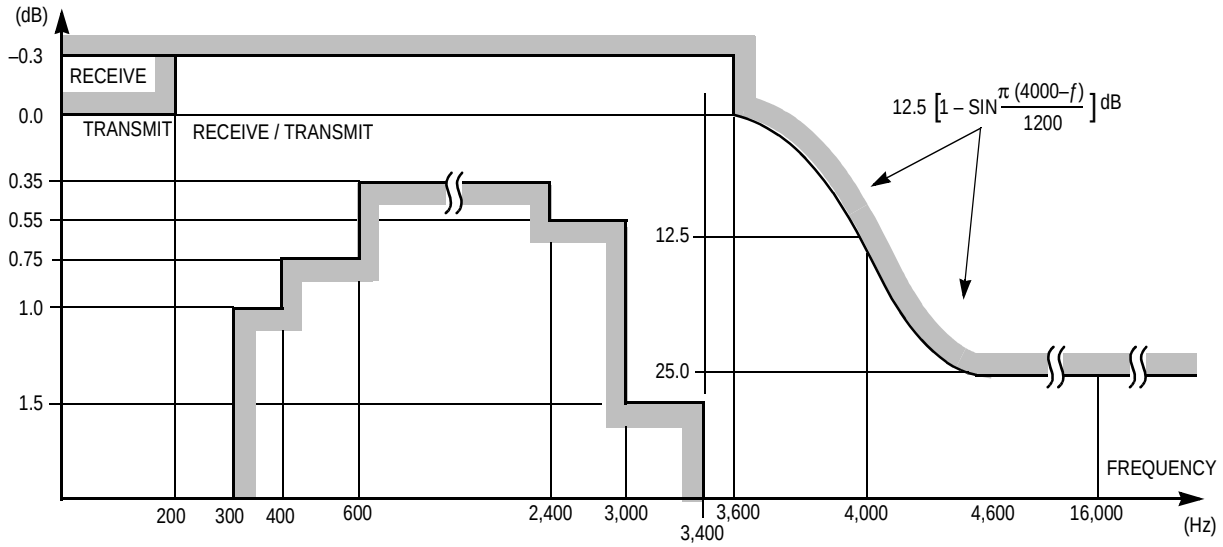


Figure 4-5. Transmit and Receive Frequency Response (Default)

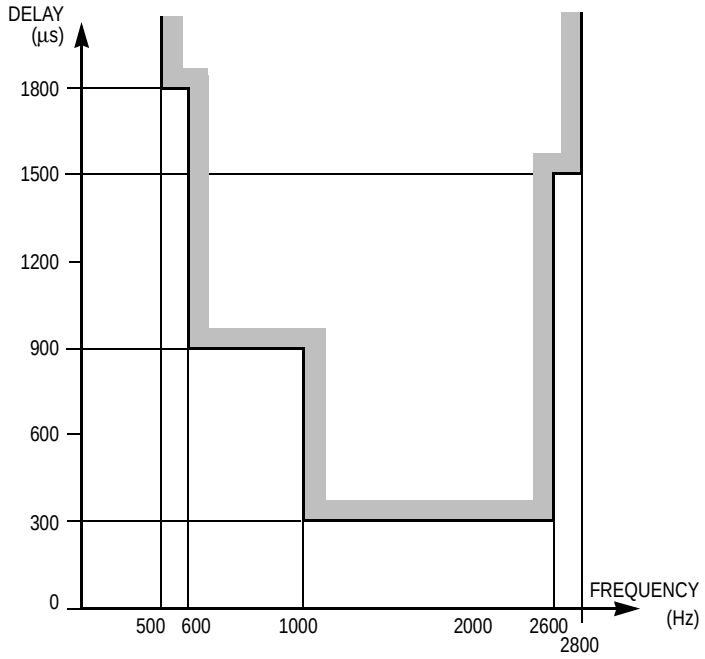


Figure 4-6. Relative Group Delay, Transmit and Receive Paths (Digital-to-Digital) Referred to 1 kHz

4.4.2 Transmit and Receive Gain

Transmit (from analog subset towards the switching system) and receive gains are user-programmable, independently for both lines. The default values are 0 dBr in the transmit direction, and –7 dBr in the receive direction.

4.4.3 Source Impedance (Z_{CO})

The central-office impedance, Z_{CO}, is synthesized using digital signal processing techniques. This renders it very stable, and moreover, programmable by the user by means of coefficients which are loaded via the PCM/SPI. Real or complex Z_{CO} impedances can be synthesized using the common three-element model (Rs, Rp, Cp; see Figure 4-7). The Z_{CO} setting is common for both lines. Both real and complex Z_{CO} impedances can be programmed to address the local requirements of specifications worldwide, and cover the following range.

Using the default coefficient values, the return loss when measured against 600 Ω (using 0 dBm input signal level) is better than 20 dB in the 300 to 3400 Hz band, and better than 10 dB at 10 kHz.

Real impedances: 600 Ω to 900 Ω.

Complex impedances: Rs from 160 Ω to 500 Ω
Rp from 300 Ω to 1000 Ω
Rp//Cp pole from 725 Hz to 5 kHz.

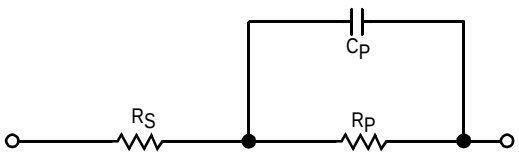


Figure 4-7. Three-Element Z_{CO} Model

4.4.4 Balance Impedance (Echo Canceller)

The balance impedance (model of the line plus set impedance used to separate the receive and transmit signals in the "hybrid") is independently programmable (though is the same for both channels). Default values offer echo return loss of better than 20 dB, though optimization to specific line and set characteristics may yield further improvement.

Table 4-4. Examples of Z_{CO} Coefficients

	Rs	Rp	Cp	Z_{CO}Sh Alfa3	Z_{CO}A2	RZ_{CO}	Z_{CO}-Gamma	Z_{CO}-Alfa3	Ftx	Ap	Nan	ACG
Belgium	600	0	0	0	0	3	0	0	237	0	0	103
Germany	220	820	115 nF	0	40	9	9	5	52	346	512	125
Europe	270	750	150 nF	0	19	7	15	4	122	388	–179	125
Z_{CO}850	850	0	0	0	0	0	0	0	282	0	0	123
Z_{CO}900	900	0	0	0	0	0	0	0	290	0	0	126

	h0	h1	h2	h3	a0	c5	b0	Dzd0	Dzd1
Belgium	4	–22	105	95	0	0	0	1	1
Germany	–31	48	1	156	0	0	0	0	0
Europe	3	–23	118	88	0	0	0	0	0
Z_{CO}850	4	–22	105	95	0	0	0	1	1
Z_{CO}900	4	–22	105	95	0	0	0	1	1

4.5 METERING

4.5.1 Metering Injection

Metering pulses of selectable frequency (12 kHz or 16 kHz) and programmable amplitude can be injected into either analog channel independently. The width of the injected pulse is determined by the user (on/off mode), or by an internal timer (burst mode) which can be set by the user from 2 ms to 510 ms in steps of 2 ms. The metering signal is always a multiple of half metering periods. See Figure 4-8.

Metering is initiated on a channel by an active low state on the corresponding $\overline{\text{MPI}}$ bit in the PCM/SPI C/I byte.

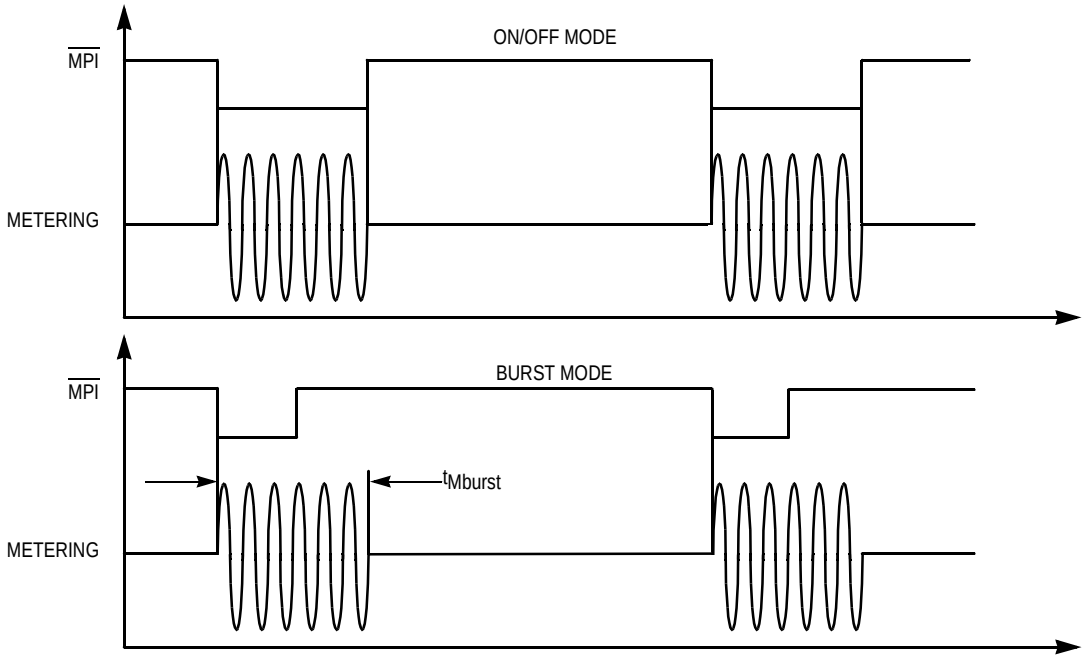


Figure 4-8. Metering Pulse Timing Diagrams

The metering level on the line is set by: $V_{LM} = (V_{GEN}\ Z_M)/(Z_M + Z_{COM})$ where:

V_{LM} = metering pulse level on the line

V_{GEN} = set level of the metering generator

Z_M = impedance of the metering load

Z_{COM} = CO impedance at the metering frequency.

The metering level V_{GEN} is selectable from 0 to a maximum level of 230 mVrms (500 m line with Z_{CO} = 900 Ω) in 15 linear steps. The internal tolerance on the metering signal level is ±10%.

4.5.2 Metering Characteristics

Table 4-5. Metering Characteristics (Determined by MC1420233 CODSP)
(Conditions: Refer to Section 5.2)

Parameter	Condition	Min	Max	Unit	Note
F_{ML}	Metering frequency, 12 kHz	11,940	12,060	Hz	1
F_{MH}	Metering frequency, 16 kHz	25,920	16,080	Hz	1
SFN1	Single-frequency noise, subharmonics for 12 kHz, 30 Hz to 12 kHz for 16 kHz, 30 Hz to 12 kHz	 — —	 –69 –69	dBm0	
SFN2	Single-frequency noise, mixed products 12 kHz, 12 kHz to 20 kHz 12 kHz, 20 kHz to 132 kHz 16 kHz	 — — —	 –51 –69 –69	dBm0	
N_{MC}	In-band noise due to metering signal	—	–60	dBmp	2
N_{MT}	Transient noise due to metering pulse	—	–35	dBm0	2
THD_M	Metering total harmonic distortion, 30 Hz to 132 kHz, out of CODSP	—	0.5	%	
D_M	Metering signal distortion at load	—	5	%	3
V_{LM}	Metering pulse amplitude, maximum level with Z_{CO} = 900 Ω, R_{line} = 130 Ω	207	253	mVrms	4
SYM_M	Metering symmetry, A and B wires	24	—	dB	5
SFN_{TX}	Single frequency noise, mixed products, 10 Hz to 4 kHz, Tx path	—	–63	dBm	

NOTES: 1. Tolerance = ±0.5%.
2. Measured in accordance to ITU-T Specification 071 (Blue Book).
3. On 200 Ω.
4. Tolerance = ±10%.
5. Tolerance = max 6%.

4.6 TONE GENERATION

The SH-POTS system allows the injection of user programmable tones, independently per channel, for signalling or user test purposes. Per channel, a tone comprising two programmable (sine wave) frequencies and programmable amplitudes can be generated (in this way, the most common call-progress and information tones, melody notes, or DTMF tones can be synthesized). The tone signal is added to the speech signal (the user must be aware of possible clipping which may occur if high signal levels are programmed), or the speech signal can also be muted during a tone burst. The tone burst duration is under user control only (the control bits for mute and tone insertion occupy the same register, which simplifies the generation of tone bursts).

The amplitude of each frequency within the tone can be independently set from 0 to the maximum level in 256 linear amplitude steps (8-bit value), with n = 63 corresponding to 0 dBm on the line. From this, the line signal level, V_{TL}, for a given gain factor n is given by:

$$V_{TL} = 20 \log(n/63) \text{ in dBm}$$

or

$$n = int(63 \times 10^{(Vtl/20)} + 0.5)$$

Table 4-6 lists values for n, for a range of tone signal levels.

The tone frequency is given by:

$$Fout = 250 \times N / 256 \text{ Hz},$$

where N is a 16-bit value (thus, N = 1024 yields a tone of 1 kHz) or

$$N = int(Fout \times 256/250 + 0.5)$$

The tone generated has continuous phase if the programmed frequency is changed during the course of a tone (this is not so if the generator is stopped and restarted). Tables 4-7 and 4-8 list the values of N required to generate commonly occurring frequencies, and the resulting error.

Table 4-6. Tone Signal Levels (Common Values) (See Note)

dBm	n	Actual	Error (dB)
3	89	3.00	0.00
1.5	75	1.51	0.01
0	63	0.00	0.00
–1.5	53	–1.50	0.00
–3	45	–2.92	0.08
–6	32	–5.88	0.12
–8	25	–8.03	–0.03
–10	20	–9.97	0.03
–15	11	–15.16	–0.16
–20	6	–20.42	–0.42
–30	2	–29.97	0.03
–36	1	–35.99	0.01

NOTE: It is possible to generate tones of very high amplitude. The user must ensure that the amplitude parameter is programmed before the tone is enabled.

Table 4-7. Tone Generator Division Values for Common Frequencies from ETS-300-001 and DTMF Tones

Common Signalling Frequencies			
Frequency (Hz)	**N**	**Actual Frequency**	**Error (%)**
300.00	307	299.805	–0.07
320.00	328	320.313	0.10
325.00	333	325.195	0.06
340.00	348	339.844	–0.05
350.00	358	349.609	–0.11
375.00	384	375.000	0.00
380.00	389	379.883	–0.03
382.50	392	382.813	0.08
400.00	410	400.391	0.10
410.00	420	410.156	0.04
420.00	430	419.922	–0.02
440.00	451	440.430	0.10
450.00	461	450.195	0.04
455.00	466	455.078	0.02
475.00	486	474.609	–0.08
490.00	502	490.234	0.05
500.00	512	500.000	0.00
525.00	538	525.391	0.07
550.00	563	549.805	–0.04
DTMF Tones			
Frequency (Hz)	**N**	**Actual Frequency**	**Error (%)**
697.00	714	697.266	0.04
770.00	788	769.531	–0.06
852.00	872	851.563	–0.05
941.00	964	941.406	0.04
1209.00	1238	1208.984	0.00
1336.00	1368	1335.938	0.00
1477.00	1512	1476.563	–0.03
1633.00	1672	1632.813	–0.01

Table 4-8. Required Frequency Setting Values (N) for a Melody Generator (Western Equal-Tempered Scale)

Octave	Note	Frequency (Hz)	N	Actual	Error (%)	
2	C	261.626	268	261.719	0.04	(Middle-C)
2	C#	277.183	284	277.344	0.06	
2	D	293.665	301	293.945	0.10	
2	Eb	311.127	319	311.523	0.13	
2	E	329.628	338	330.078	0.14	
2	F	349.228	358	349.609	0.11	
2	F#	369.994	379	370.117	0.03	
2	G	391.995	401	391.602	–0.10	
2	Ab	415.305	425	415.039	–0.06	
2	A	440.000	451	440.430	0.10	
2	Bb	466.164	477	465.820	–0.07	
2	B	493.883	506	494.141	0.05	
3	C	523.251	536	523.438	0.04	
3	C#	554.365	568	554.688	0.06	
3	D	587.330	601	586.914	–0.07	
3	Eb	622.254	637	622.070	–0.03	
3	E	659.255	675	659.180	–0.01	
3	F	698.456	715	698.242	–0.03	
3	F#	739.989	758	740.234	0.03	
3	G	783.991	803	784.180	0.02	
3	Ab	830.609	851	831.055	0.05	
3	A	880.000	901	879.883	–0.01	
3	Bb	932.328	955	932.617	0.03	
3	B	987.767	1011	987.305	–0.05	
4	C	1046.502	1072	1046.875	0.04	
4	C#	1108.731	1135	1108.398	–0.03	
4	D	1174.659	1203	1174.805	0.01	
4	Eb	1244.508	1274	1244.141	–0.03	
4	E	1318.510	1350	1318.359	–0.01	
4	F	1396.913	1430	1396.484	–0.03	
4	F#	1479.978	1515	1479.492	–0.03	
4	G	1567.982	1606	1568.359	0.02	
4	Ab	1661.219	1701	1661.133	–0.01	
4	A	1760.000	1802	1759.766	–0.01	
4	Bb	1864.655	1909	1864.258	–0.02	
4	B	1975.533	2023	1975.586	0.00	
5	C	2093.005	2143	2092.773	–0.01	
5	C#	2217.461	2271	2217.773	0.01	
5	D	2349.318	2406	2349.609	0.01	
5	Eb	2489.016	2549	2489.258	0.01	

Table 4-8. Required Frequency Setting Values (N) for a Melody Generator (Western Equal-Tempered Scale) (continued)

Octave	Note	Frequency (Hz)	N	Actual	Error (%)	
5	E	2637.020	2700	2636.719	–0.01	
5	F	2793.826	2861	2793.945	0.00	
5	F#	2959.955	3031	2959.961	0.00	
5	G	3135.963	3211	3135.742	–0.01	
5	Ab	3322.438	3402	3322.266	–0.01	
5	A	3520.000	3604	3519.531	–0.01	
5	Bb	3729.310	3819	3729.492	0.00	
5	B	3951.066	4046	3951.172	0.00	

4.7 CODSP CLOCK RECOVERY PLL

The CODSP device derives its internal clocks from the PCM/SPI input by means of a PLL. The PLL automatically detects the clock mode in use, and sets the multiplication factor accordingly. The PLL loop filter requires an external capacitor as shown in the application schematic.

SECTION 5
ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS

Operation of the device at or near these conditions is not guaranteed. Sustained exposure to these limits will adversely affect device reliability.

Table 5-1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Battery voltage BATR (ref. to V_{SSB}) of SHLIC	BATR	–75	0.5	V
Battery voltage BATS (ref. to V_{SSB}) of SHLIC	BATS	–35	0.5	V
Difference between the batteries BATR and BATS, BATR-BATS of SHLIC	DBAT	–40	0.5	V
V_{DD5A} (ref. to V_{SSA}) of SHLIC	V_{DD5A}	–0.5	7	V
V_{SSB} (ref. to V_{SSA}) of SHLIC	V_{SSB}	–0.5	0.5	V
Ambient temperature under bias of SHLIC	T_A	–40	85	°C
Maximum absolute power dissipation, T_A = 85°C		—	1.3	W
V_{DD3A},V_{DD3D} to CODSP	V_{DD3}	V_{SS} – 0.3	4	V
Voltage on any device pin (see Note) of CODSP	V_{in}	V_{SS} – 0.3	V_{DD3} + 0.3	V
Function temperature under bias of CODSP		–55	150	°C
Storage temperature	T_{stg}	–65	150	°C
Lead temperature (soldering 10 s)		—	300	°C

NOTE: Except special 5 V tolerant I/Os of CODSP as noted in Table 3-1.

5.2 OPERATING CONDITIONS

Operating ranges define the limits for functional operation and parametric characteristics of the device as described in this document, and for the reliability specifications. Correct functioning outside of these limits is not implied. Total cumulative exposure outside the normal power supply voltage range or ambient temperature under bias, must be less than 0.1% of the normal useful life as defined in Table 5-1.

Table 5-2. Operating Conditions

(All Voltages Referenced to $V_{SSA} = V_{SSB}$ or $V_{SS} = V_{SSA}$, as Appropriate)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
BATR	Ringing battery voltage	–72	–65	–18	V
BATS	Speech battery voltage	–35	–32	–18	V
D_{BAT}	Difference between the batteries BATR and BATS, BATR-BATS	–40	–35	0	V
V_{DD5A}	Supply voltage SHLIC (ref. to V_{SSA})	4.75	5	5.5	V
T_{range}	Operating temperature range	–40	—	85	°C (Note)
V_{DD3D} V_{DD3A}	V_{DD} of CODSP (3.3 V ±8%)	3.036	3.3	3.564	V

NOTE: See Section 5.4; maximum power dissipation is dependent on maximum ambient temperature.

5.3 THERMAL SHUTDOWN SHLIC

Thermal limiting circuitry on chip of the SHLIC will shut down the circuit at a junction temperature of about 165°C. The device should never be run at this temperature. Operation above 145°C junction temperature might degrade device reliability.

Thermal resistance = 55°C/w typ.

5.3.1 Transient Energy Capability

During testing, each device termination withstands being shorted to the supply voltages or ground as specified below. The shorting must be limited to 1 s.

Shorted to V_{SSA}, V_{DD5A} or V_{SSB}: VAG, PU, RNG, BR, TST, T_A, DCC, DCO, DCI, Tx to Rx

Shorted to V_{SSA}, V_{SSB} or BATS: AW, BW, SA to SB

5.4 DC CHARACTERISTICS (MC1430132 SHLIC, UNLESS OTHERWISE NOTED)

Unless otherwise stated, these characteristics apply for the operating conditions specified in Section 5.2. All parameters are explicitly or implicitly tested during production at the operating conditions unless they are marked with an asterisk (*), where they are guaranteed by design. Parameters marked with a double asterisk (**) are meant as user information only. Tests are performed using an equivalent of the application schematic.

Table 5-3. Power Supply Currents

Symbol	Parameter	Test Condition	Limits			Unit
			Min	Typ	Max	
I_{BATR}	BATR current (IL = 0)	Power RNG = 0	—	0.35	0.5	mA
		Up RNG = 1	—	3.5	5.0	mA
		Power RNG = 0	—	0.35	0.5	mA
		Down RNG = 1	—	2.5	3.5	mA
I_{BATS}	BATS current (IL = 0)	Power RNG = 0	—	3.5	5	mA
		Up RNG = 1	—	3.5	5	mA
		Power RNG = 0	—	1.5	2.5	mA
		Down RNG = 1	—	—	0.5	mA
I_{VDD}	V_{DD} current (I_{V3} = 0)	Power-up	—	3	5.5	mA
		Power-down	—	2.5	4	mA
P_{CC}	Power dissipation of CODSP (@ 3.45 V V_{DD3A} and V_{DD3D})	Power-down	—	—	30	mW
		Power-up 1 line active*	—	—	140	mW
		Power-up 2 lines active	—	—	180	mW

NOTES: 1. IL is the line current; i.e., these parameters are measured without line current.
2. I_{V3} is the load current in pin V3.
3. The maximum values in the table are valid for the full battery voltage ranges:
–18 V to –72 V for ringing battery BATR.
–18 V to –35 V for battery BATS. (BATR must always be the most negative one.)
4. In case of sleep mode activation. See Tables 6-5 and 6-7 for programming values.

Table 5-4. SHLIC Dissipation

Parameter	Symbol	Value	Unit
Maximum operating power dissipation, T_A = 70°C	Pmax_op	1.2	W

The specifications for power dissipation imply that in ring mode, the active ring phase must at least be four times shorter than the non-active ring phase. The maximum duration of the active ring phase must be below 2 s.

5.4.1 Power-On Reset

Table 5-5 shows the power reset threshold for V_{DD5A} of the SHLIC. As long as V_{DD5A} is below the reset threshold, SHLIC is held in power-down, and the output pins AW and BW are high impedance.

The CODSP uses a separate input pin, PWRS, for system reset at power-up.

Table 5-5. Power-On Reset Characteristics

Symbol	Parameter	Test Condition	Limits			Unit
			Min	Typ	Max	
V_{DDPWR}	Threshold voltage for power reset on V_{DD} of SHLIC		3.0	3.5	4.0	V
t_{PWRS}	Active low pulse width on PWRS of CODSP		10	—	—	ms
V_{PWRS}	Threshold voltage for reset on PWRS of CODSP		1.6	—	1.7	V

5.4.2 V_{DD3} Regulator

This series regulator of the SHLIC can be used to provide the supply voltage for the CODSP or other 3.3 V devices.

Table 5-6. V_{DD3} Regulator Characteristics

Symbol	Parameter	Test Condition	Limits			Unit
			Min	Typ	Max	
V_{DD3}	V_{DD3} output voltage	Load current I_{V3V} between 0 and 50 mA	3.05	3.3	3.55	V
I_{load}	Load current range		0	—	50	mA
PSRR	Signal rejection V_{DD} to V_{DD3}	Frequency range 0 to 10 kHz	20	—	—	dB
L_{REG}	Load regulation	Load current range from 5 to 50 mA	–1	—	1	Ω
C_{load} (**)	Maximum load capacitance	Load current range from 0 to 50 mA	—	100	—	nF
I_{CC}(*)	Current limitation shorted output	V_{DD3} shorted to V_{SSA}	70	—	200	mA

Table 5-7. Voltage Characteristics A Wire (AW), B Wire (BW)

Symbol	Parameter	Test Condition			Limits			Unit
		PU	BR	RNG	Min	Typ	Max	
V_{AWN}	Normal DC-bias on AW (ref. V_{SSB})	1	0	0	–3.5	–3.1	–2.7	V
V_{BWN}	Normal DC-bias on BW (ref. BAT)	1	0	0	2.5	3	3.5	V
V_{AWR}	Reverse polarity DC-bias on AW (ref. BAT)	1	1	0	2.5	3	3.5	V
V_{BWR}	Reverse polarity DC-bias on BW (ref. V_{SSB})	1	1	0	–3.5	–3.1	–2.7	V
V_{AW_H}	DC bias on AW in Act_H mode (TST = 1, ref. V_{SSB})	1	x	1	–4	–3	–2	V
V_{BW_H}	DC bias on BW in Act_H mode (TST = 1, ref. BAT)	1	x	1	2	3	4	V
V_{HWPD}	Voltage level high wire (IL < 5 mA)	0	x	0	–0.8	–0.5	—	V
V_{LWPD}	Voltage level low wire (IL < 5 mA), ref. BAT	0	x	0	—	0.5	0.8	V
V_{AWring} V_{BWring}	DC-level both wires in ringing mode (TST = 0)	1	0	1	BAT/2 –2%	BAT/2	BAT/2 2%	V

NOTE: These bias values are only valid if both DCC and Rx are biased at VAG voltage level.

Table 5-8. Impedance Characteristics A Wire (AW), B Wire (BW)

Symbol	Parameter	Test Condition	Limits			Unit
			Min	Typ	Max	
$Z_{A(B)WO}$ (*)	Output impedance at AW (BW) (power-up)	0 mA < IL < 70 mA 0 < f < 16 kHz	—	—	1.5	Ω
Z_{A-BWO} (*)	Tracking of the output impedance on AW and BW	0 mA < IL < 70 mA 0 < f < 16 kHz	—	—	0.3	Ω
Z_{HWOD}	Output impedance on high wire (power-down)	PU = 0	5	—	130	Ω
Z_{LWOD}	Output impedance on low wire (power-down)	PU = 0	5	—	130	Ω
Z_{OMD}	Matching output impedance low versus high wire (power-down)	PU = 0	–70	—	70	Ω
$I_{A(B)OC}$ $I_{A(B)HIMP}$	Output current in and out AW (BW) with OT (over-temperature) detected	A(B)W_V_{SSB} and A(B)W_BATS	–700	—	700	µA

Table 5-9. Rx, Tx Characteristics

Symbol	Parameter	Test Condition	Limits			Unit
			Min	Typ	Max	
Z_{Tx} (*)	Output impedance at Tx	f = 1 kHz	—	—	10	Ω
V_{OTx}	Offset voltage on Tx (PU=1) (ref. VAG)	SA shorted to AW and SB to BW, DCI to V_{DD3}, DCO to VAG	–20	0	20	mV
I_{OUTTx}	Tx output current capability		–1	—	0.05	mA
V_{Rx}(*)	Rx input voltage range (ref. VAG)		–1	—	1	V
Z_{Rx}	Rx input impedance	f = 1 kHz	20	—	—	kΩ

5.4.3 DCO DC Levels, Impedances

These limits are generally transparent to the user, but are given here for information.

Table 5-10. DCO Characteristics

Symbol	Parameter	Test Condition	Limits			Unit
			Min	Typ	Max	
Z_{DCO} (*)	Output impedance at DCO		—	—	10	Ω
V_{ODCO}	Offset voltage on DCO (ref. VAG)	SA shorted to AW and SB to BW	–20	0	20	mV
I_{OUTDCO} (*)	DCO output current capability		–1	—	0.05	mA
Z_{DCI}	Input impedance at DCI	f = 1kHz	210	—	—	kΩ

5.4.4 VAG Analog Ground Input

The analog ground is typically half the voltage of the V_{DD3} output voltage. It is the reference for all analog interfacing between SHLIC and the CODSP. VAG is provided by the CODSP.

Table 5-11. VAG Characteristics

Symbol	Parameter	Test Condition	Limits			Unit
			Min	Typ	Max	
V_{VAG} (**)	Voltage level at VAG pin CODSP		1.53	1.65	1.77	V
I_{VAG}	VAG input current SHLIC	VAG = 1.65 V	—	—	0.5	mA

5.4.5 DC Loop Filter

These limits are generally transparent to the user, but are given here for information.

Table 5-12. DC Loop Filter Characteristics

Symbol	Parameter	Test Condition	Limits			Unit
			Min	Typ	Max	
V_{DCLF1}	DCLF1 output voltage (ref. V_{SSB})	RNG = 0, PU = 1	–3.5	–3.1	–2.7	V
V_{DCLF2}	DCLF2 output voltage (ref. BAT)	RNG = 0, PU = 1	2.5	3.0	3.5	V
Z_{DCLF1S}	Output impedance at DCLF, $V_{DCLF} - V_{DCLF1} < 0.5$ V	RNG = 0, PU = 1	0.6	1	1.4	MΩ
Z_{DCLF2S}	Output impedance at DCLF, $V_{DCLF2} - V_{DCLF} < 0.5$ V	RNG = 0, PU = 1	0.6	1	1.4	MΩ

5.4.6 DCC Input Pin

These limits are generally transparent to the user, but are given here for information.

Table 5-13. DCC Input Characteristics

Symbol	Parameter	Test Condition	Limits			Unit
			Min	Typ	Max	
V_{DCC}	DCC input voltage range (ref. VAG)	RNG = 0, PU = 1	–1	—	1	V
I_{INDCC}	DCC input current, V_{DCC} = VAG + 1 V	RNG = 0, PU = 1	—	4	10	µA

NOTE: Forcing DCC positive (ref. VAG) will result in a smaller voltage between the A and B wire. If too large of a signal is applied at DCC, both wires are clamped at the same voltage (only a small residual voltage remains on the line).

5.4.7 Characteristics for the Digital I/O Pins

These include CODSP, plus TST, PU, BR, RNG of SHLIC.

Table 5-14. Digital I/O Characteristics

Symbol	Parameter	Test Condition	Limits			Unit
			Min	Typ	Max	
V_{IL}	Low-level input voltage		—	—	0.8	V
V_{IH}	High-level input voltage		2.0	—	—	V
I_{IL}	Low-level input current (except PU, see RPD below)	V_{DD} = 5.25 V	–1	—	1	µA
I_{IH}	High-level input current (except PU, see RPD below)	V_{DD} = 5.25 V	–1	—	1	µA
C_{INP} (*)	Input capacitance		—	—	7	pF
R_{PD}	Pull-down resistance at pin PU		18	30	40	kΩ
V_{OL}	Output level PU pin, driven low	Over-temperature OT activated, I_{PU} = 0.2 mA, tested at high temperature only	—	—	0.5	V
V_{IL}	Low-level input voltage, CODSP		—	—	0.2 x V_{DD3D}	V
V_{IH}	High-level input voltage, CODSP		0.8 x V_{DD3D}	—	—	V
V_{OL}	Low-level output voltage, CODSP		—	—	0.4	V
V_{OH}	High-level output voltage, CODSP		—	—	5.25	V
C_{in}	Input pin capacitance, CODSP (see Note)		—	—	4	pF
C_{out}	Load capacitance, CODSP		—	—	100	pF
I_{IH}	High-impedance leakage current	V_{OH} = 5.5 V off state	–10	—	10	µA

NOTE: Excluding package and measured at 0 V.

Table 5-15. Sense Bridge Inputs Characteristics

Symbol	Parameter	Test Condition	Limits			Unit
			Min	Typ	Max	
R_{AW-SB}	Bridge resistance from AW to SB	V_{DD}, VAG = 0 V, 25°C	205	257	309	kΩ
R_{SA-BW}	Bridge resistance from BW to SA	V_{DD}, VAG = 0 V, 25°C	205	257	309	kΩ

5.4.8 Test Switch

The internal test switch is between pins SB and SSB. Connecting an external load between SSB and SA allows test of the transmission characteristics in (simulated) off- and on-hook conditions. The typical on-resistance of the test switch is around 75 Ω, and has to be taken into account when defining the external load. The test switch is on when RNG = 0, PU = 1, TST = 1, BR = 0.

Table 5-16. Test Switch Characteristics

Symbol	Parameter	Test Condition	Limits			Unit
			Min	Typ	Max	
I_{SWoff}	Switch leakage current	$\|V_{SSB} - VSB\| < 72$ V	—	—	5	µA
V_{SWon}	Voltage drop over test switch	I_{SW} = 80 mA	4	—	9	V
		I_{SW} = 20 mA (V_{SSB} – VSB > 0 V)	1	—	3	V

NOTE: The test switch is normally off when V_{DD} is below the reset level. If the battery voltages are sufficient, the switch remains on, if it was on before V_{DD} went below the reset level.

5.4.9 Battery Switch

This switch is activated during ringing or when the higher on-hook voltage is selected (RNG = 1). When active, BATR is connected to the internal battery supply line V_{BAT}. In other cases (RNG = 0), the switch is open; V_{BAT} is now connected to BATS via an internal diode.

Table 5-17. Ringing Battery Switch Characteristics

Symbol	Parameter	Test Condition	Limits			Unit
			Min	Typ	Max	
I_{BSWoff} (*)	Leakage current battery switch (RNG = 0)	BATR = –72 V, BATS = –32 V	—	—	5	µA
$I_{REVBATS}$ (*)	Reverse current BATS diode (RNG = 1)	BATR = –72 V, BATS = –32 V	—	—	5	µA
V_{DRBATS}	Forward drop BATS diode	Load current < 80 mA	—	0.85	1.2	V
I_{BSon}	Current capability battery switch		0	—	80	mA
V_{BSWon}	Voltage drop over battery switch (RNG = 1)	Load current < 80 mA	—	1	2	V

5.5 AC CHARACTERISTICS (SHLIC)

Unless otherwise stated, the characteristic limits apply over the operating conditions specified in Section 5.2 and each combination of the drive bits.

All parameters are specified in the presence of a longitudinal current of max 5 mA and a dc current of between 0 mA and the current limit. The behavior of the chip in the presence of longitudinal voltages is not tested in production.

The different gains in the signal paths are shown in Figure 5-1. The values of the gains are given in Table 5-18.

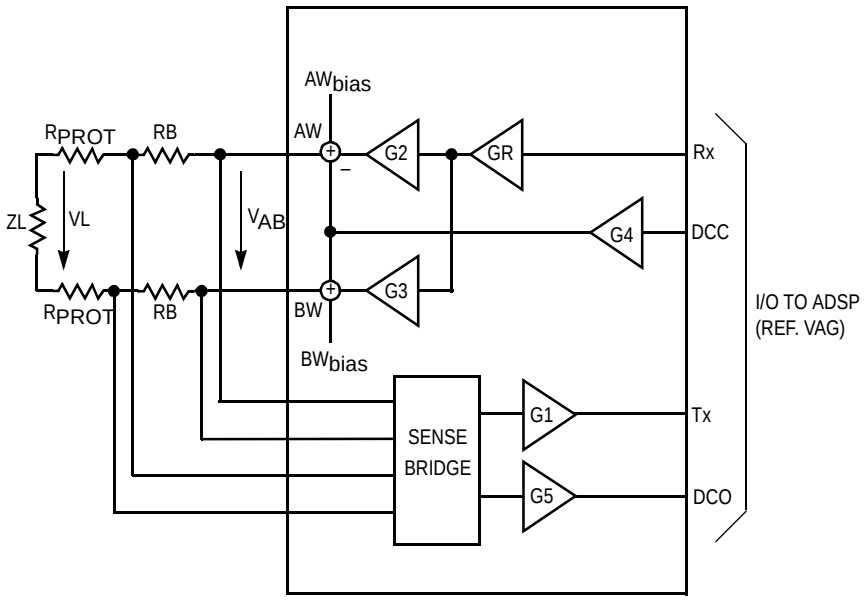


Figure 5-1. Block Diagram Showing Gains in Various Signal Paths in SHLIC

Table 5-18. Typical Gains

Gain	Factor
G1	1.66
G1′	0.079
G2	2
G3	–2
G4	15
G5	–1/8
GR	1
GR′	35/2

The gains in Table 5-18 are not tested. They are mentioned for information only. The pin-to-pin gains in Table 5-20 (G_{RX}, G_{TX}, etc.) are tested and guaranteed. In case of ringing, the receive gain is changed from GR to GR′, the transmit gain factor G1 is changed to G1′.

The default test condition of the input bits is: PU = 1, RNG = 0, BR = 0/1. DCC is shorted to VAG.

NOTE 0 dBm: 1 mW in 600 ohms.

5.5.1 Receive Path

The following equation is valid for an open loop configuration. This does not incorporate the Z_{CO} synthesis, which is defined by the feedback from Tx to Rx. This function is performed in the CODSP.

$$GRX = \frac{VAB}{VRX} = GR(G3 - G2)$$

5.5.2 Transmit Path

The following equation is valid under open loop conditions.

$$GRX = \frac{Vx}{VL} = \frac{2RB}{ZL} \quad G1$$

5.5.3 Overpower and Short Circuit Protection

In power-down, the DC-loop current limitation is not active. The line current is limited directly through the line drivers.

The AW and BW outputs are fully protected against short circuits to a voltage between V_{SSA}/V_{SSB} and BATR (see Figure 5-2).

The current flowing from (or into) AW and/or BW is limited to a value I_{LW}/I_{HW} as long as the junction temperature $T_J < 165°C$ (electronic current limitation). The values for I_{LW}/I_{HW} for different conditions are given in the table below. If T_J rises above 165°C (±15%) the output drivers' outputs are made high impedance. Current can only flow in or out of the internal protection diodes, in case V_{SA} and/or V_{SB} exceeds the range between V_{SS} and BATR. The currents should, however, be limited externally (internal clamping diodes protection) (see Section 2.2).

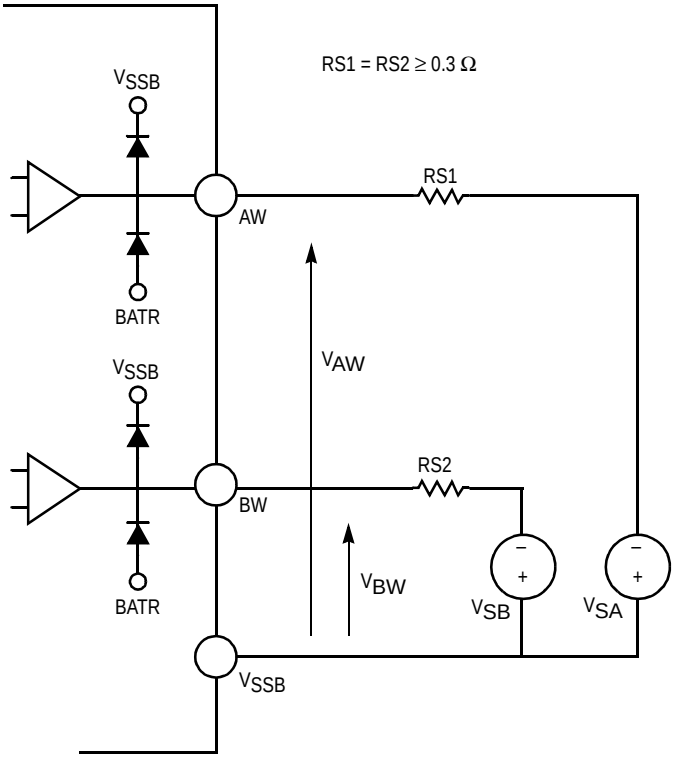


Figure 5-2. Short Circuit Protection

Table 5-19. Short Circuit Protection Characteristics

Symbol	Parameter	Test Condition	Limits			Unit
			Min	Typ	Max	
I_{LW}	Short circuit peak current, power-up, sink current	PU = 1	–145	–120	–95	mA
	Short circuit peak current, power-down, sink current	PU = 0	–65	–45	–20	mA
I_{HW}	Short circuit peak current, power-up, source current	PU = 1	95	120	145	mA
	Short circuit peak current, power-down, source current	PU = 0	20	45	65	mA

5.6 OFF-HOOK CHARACTERISTICS (MS140132KT SYSTEM)

Table 5-20. Off-Hook Characteristics (MS140132KT System)
(Conditions: Refer to Section 5.2)

Parameter	Condition	Min	Max	Unit	Note
G_{TX}	Relative gain, transmit direction Gain programming step Step accuracy Gain tolerance (ref. programmed value)	–6 — — –0.5	1 0.25 0.1 0.5	dB	1
G_{RX}	Relative gain, receive direction Gain programming step Step accuracy Gain tolerance (ref. programmed value)	–12 — — –0.5	1 0.25 0.05 0.5	dB	1
d_{GLT}	Long-term gain stability	–0.5	0.5	dB	2
G_{TTX}	Gain tracking, Tx path 3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0	 –0.3 –0.6 –1.6	 0.3 0.6 1.6	dB	3
G_{TRX}	Gain tracking, Rx path 3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0	 –0.3 –0.6 –1.6	 0.3 0.6 1.6	dB	3
IMD_{TX}	Intermodulation distortion, Tx path	—	–45	dBm0	4
IMD_{RX}	Intermodulation distortion, Rx path	—	–50	dBm0	4
S_{DTX}	Signal to total distortion ratio, Tx (gain = 0 dB) 0 to –10 dBm0 –20 dBm0 –30 dBm0 –40 dBm0 –45 dBm0	 35 34.7 32.9 24.9 19.9	 — — — — —	dB	5
S_{DRX}	Signal to total distortion ratio, Rx (gain = –7 dB) 0 to –10 dBm0 –20 dBm0 –30 dBm0 –40 dBm0 –45 dBm0	 35 33.8 28.8 19.5 14.5	 — — — — —	dB	5
SFN_{RX}	Single frequency noise 300 to 3400 Hz, all out-of-band frequencies 700 to 1100 Hz in-band 300 to 3400 Hz	 — —	 –40 –49	dB	
	Longitudinal balance	1%	40	dB	
	Resistor matching	0.1%	46	dB	

NOTES: 1. User programmable.
2. Covers variations within the permitted ranges of supply voltage and temperature during any one year.
3. Referred to the gain at 1020 Hz applied to the input at a level –10 dBm0.
4. Intermodulation distortion measured for all intermodulation products of any non-harmonically related frequencies in the range 300 to 3400 Hz for levels between –4 and –21 dBm0.
5. Intermodulation distortion measured for all intermodulation products of a frequency in the range 300 to 3400 Hz at –9 dBm0 and 50 Hz at –23 dBm0.

5.7 OFF-HOOK DETECTION

Each channel has one I/O pin used for signalling purposes, $\overline{\text{DET*}}$. With this, one signalling bit from the SH-POTS chipset can be routed to this output: off-hook detection ($\overline{\text{LS*}}$), alarm ($\overline{\text{AL*}}$), or ring phase ($\overline{\text{RPH*}}$). Register 5 [4-2] defines which bit. $\overline{\text{DET*}}$ is the default functionality. This value can be changed as follows.

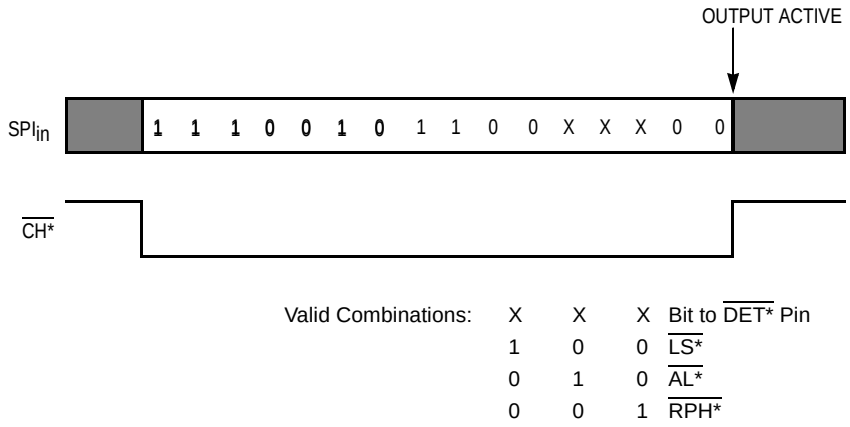


Figure 5-3. Write Signalling Register

See the MS140131KT/D data sheet for a functional explanation of the signalling bits. The other bits should not be changed.

$\overline{\text{DET0}}$ (default) is the on/off hook and ring trip detection open drain output for line 0. When off-hook, $\overline{\text{DET0}}$ goes low. When on-hook, $\overline{\text{DET0}}$ is high impedance.

$\overline{\text{DET1}}$ (default) is the corresponding on/off hook and ring trip detection output for line 1.

5.8 PROGRAMMING THE PCM CLOCK FREQUENCY

The PCMCLK clock is used for generation of the internal 512 kHz clock required for the PCM/SPI interface. Register 7 has to be programmed to the expected value.

SECTION 6
DETAILED PROGRAMMING DESCRIPTION

6.1 SPI INTERFACE

The data on pin SPI_{in} is shifted in on the rising edge of SPICLK. The data on SPI_{out} occurs at the falling edge of SPICLK. The first bit is shifted out on the falling edge of SPICLK after $\overline{CH*}$ became active (= low level) or at the falling edge of $\overline{CH*}$ after SPICLK became active (= low level). The user should ensure that the data on SPI_{out} is stable at moment of use: the master device will normally read in the data of SPI_{out} on the rising edge of the clock (equal to SPICLK on the SH CODSP). Both select signals $\overline{CH0}$ and $\overline{CH1}$ can not be simultaneously activated.

Note that $\overline{CH*}$ may remain low 8 or 16 bits during shift out of data via SPI_{out} depending on the type of read request.

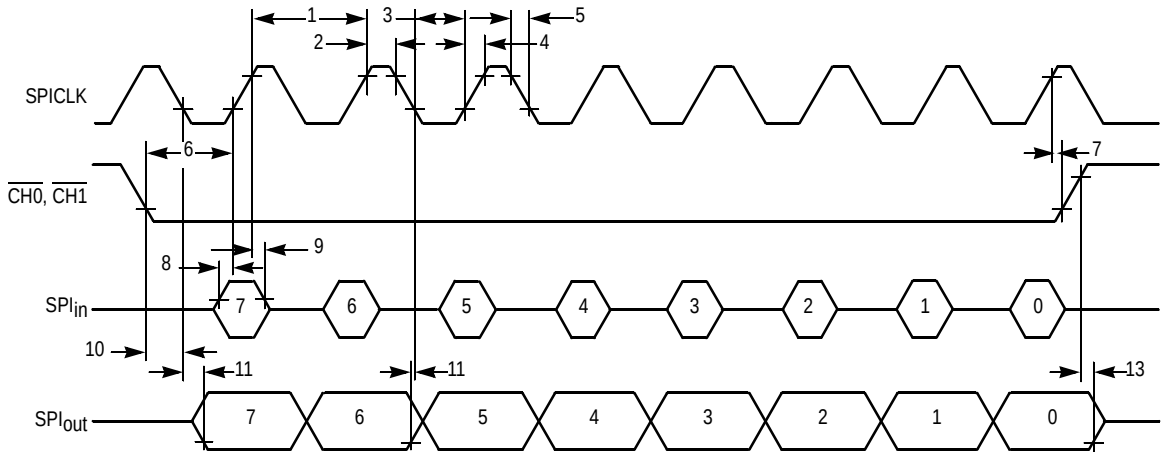


Figure 6-1. SPI Bus Timing Parameters

Table 6-1. SPI Bus Timing Characteristics

No.	Symbol	Parameter	Min	Typ	Max	Units
1	$1/t_{SPICLK}$	SPICLK Frequency	0	2.048	8.192	MHz
2	t_{SPICLK_H}	SPICLK High Time	50	$t_{SPICLK}/2$	—	ns
3	t_{SPICLK_L}	SPICLK Low Time	50	$t_{SPICLK}/2$	—	ns
4	t_{SPICLK_R}	SPICLK Rise Time	—	—	15	ns
5	t_{SPICLK_F}	SPICLK Fall Time	—	—	15	ns
6	t_{CH_SU}	$\overline{CH*}$ Setup Time Before SPICLK Rising Edge	50	—	—	ns
7	t_{CS_H}	$\overline{CH*}$ Hold Time After SPICLK Rising Edge	50	—	—	ns
8	t_{SPIIN_SU}	SPI_{in} Data Setup Time Before SPICLK Rising Edge	50	—	—	ns
9	t_{SPIIN_H}	SPI_{in} Data Hold Time After SPICLK Rising Edge	50	—	—	ns
10	t_{SPIOUT_V}	SPI_{out} Data Valid After $\overline{CH*}$ Falling Edge (see Notes 1, 2, 4)	0	—	50	ns
11	t_{SPIOUT_V}	SPI_{out} Data Valid After SPICLK Falling Edge (see Notes 1 ,2, 4)	0	—	50	ns
13	t_{SPIOUT}	SPI_{out} High-Z After $\overline{CH*}$ Rising Edge (see Notes 2, 3)	0	—	50	ns

NOTES: 1. Values guaranteed with a maximum capacitive load of 50 pF.
2. On condition the other pin (= SPICLK or $\overline{CH*}$) is already low.
3. When $\overline{CH*}$ transits to high at the end: bit 0 stays valid until $\overline{CH*}$ becomes high or next negative transition on SPICLK occurs.
4. SPI_{out} valid means the moment V_{OL} level is reached for a low level or the moment the driver becomes high impedance (High-Z) for a high level.

6.2 PCM INTERFACE

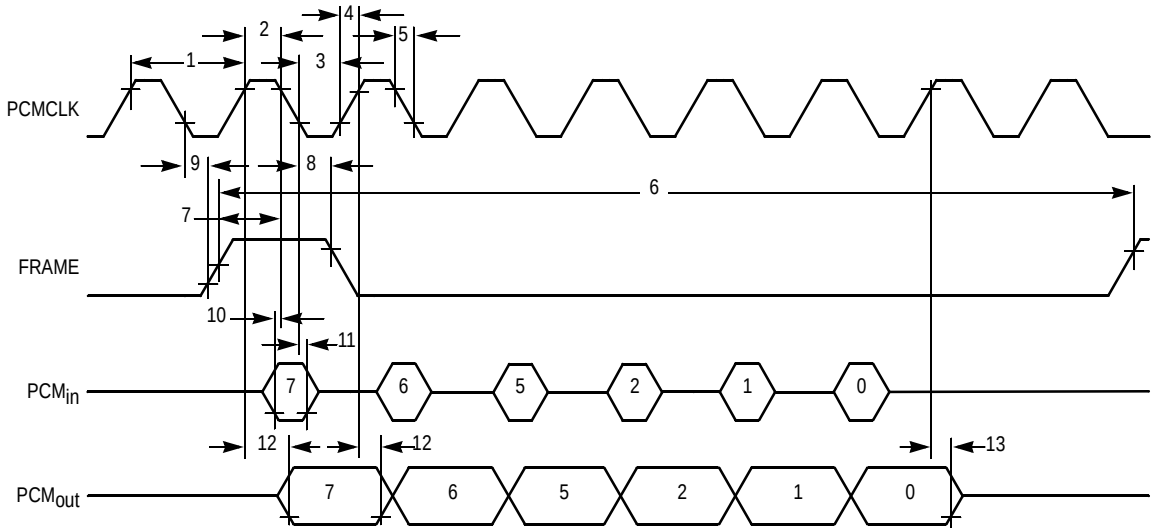


Figure 6-2. PCM Bus Timing Parameters

Table 6-2. PCM Bus Timing Characteristics

No.	Symbol	Parameter	Min	Typ	Max	Unit
1	$1/t_{PCLK}$	PCMCLK Frequency (Note 1)	512	2048	8192	kHz
		PCMCLK Accuracy	–100	—	100	ppm
2	t_{WCLKH}	Width of PCMCLK High	50	—	—	ns
3	t_{WCLKL}	Width of PCMCLK Low	50	—	—	ns
4	t_R	PCMCLK Rise Time	—	—	15	ns
5	t_F	PCMCLK Fall Time	—	—	15	ns
6		FRAME Period		125	—	ns
7	t_{SFSCKL}	Setup Time From FRAME High to PCMCLK Low	50	—	—	ns
8	t_{HCKFSL}	Hold Time of PCMCLK Low to FRAME Low	50	—	—	ns
9	t_{HCKFSH}	Hold Time From PCMCLK Low to FRAME High	50	—	—	ns
10	t_{SINCK}	Setup Time From PCM_{in} to PCMCLK Low	50	—	—	ns
11	t_{HCKIN}	Hold Time From PCMCLK Low to PCM_{in} Invalid	50	—	—	ns
12	t_{DCKDXV}	Delay Time From PCMCLK to PCM_{out} Valid (Notes 2, 3)	0	—	50	ns
13	t_{DCFDXD}	Delay Time From PCMCLK to PCM_{out} Disabled (High-Z)	0	—	50	ns

NOTES: 1. PCMCLK must be an integer multiple of 512 kHz.
2. PCM_{out} timing is defined with capacitive load = 50 pF.
3. PCM_{out} valid means the moment V_{OL} level is reached for a low level or the moment the driver becomes high impedance (High-Z) for a high level.

6.3 FUNCTIONAL DESCRIPTION OF THE PROGRAMMING INTERFACE: SPI

The SPI block operates on a totally independent clock, SPICLK. This clock can vary from dc up to 8192 kHz. If the pin $\overline{CH0}$ or $\overline{CH1}$ is pulled low (= activation), the clock is gated through the interface block and the other $\overline{CH*}$ pin is deactivated. With this, the registers of the PCM2GCI interface block can be programmed.

The data is shifted in via the SPI_{in} pin at the rising edge of SPICLK. The data is always transmitted as bytes (or multiples). The first byte received via the SPI_{in} pin is always the command byte. The first 2 bits define the type of command.

B7	B6	Function
0	0	Software Reset
0	1	Write Control Word
1	0	Access CODEC Memory
1	1	Access Interface Block Registers + Idle Command

These two bits are interpreted on-line and represent a specific action. The table below describes the valid commands, a short functional description and action description from the SPI interface block:

Valid Command	Function
00000000	Software Reset
01XXXXXX	Write Control Word
10000000	ID Request
10001BBB	Write Request
10011BBB	Read Request
110YYYYY	Interface Block Registers: Read Request
111YYYYY	Interface Block Registers: Write Request
11111111	Idle Command: Can Be Used When SPI_{out} Data is Expected

SPI_{out} is a three-state serial data (8-bits, MSB first) output. The output is activated at the moment data is available after a GCI monitor command (ID or read request) or after an interface-block-read request. The data is shifted out of SPI_{out} on the SPICLK falling edge when $\overline{CH*}$ is low. At that moment, data on SPI_{in} is not accepted by the interface. When both $\overline{CH*}$ are high, SPI_{out} is in high impedance state. Before data can be shifted out on SPIOUT, $\overline{CH*}$ is set high for a small time. The same $\overline{CH*}$ signal as used for the command must also be used for the data that will be shifted out of SPI_{out}.

At power-up, the chipset is programmed to power down, and the output SPI_{out} is in the high-impedance state (refer also to the memory map).

In case multiple bytes are required for execution of a command (e.g., writing data in the CODSP memory), these can be send in separate cycles, or within the same activation of $\overline{CH0}$ or $\overline{CH1}$.

Only the command 01* is dependent on which $\overline{CH0}$ or $\overline{CH1}$ is activated.

None of the bytes received via the SPI_{in} are echoed via the SPI_{out}; only the requested read-data is returned.

$\overline{\text{BUSY}}$ Function: This signal (when low) indicates that the SPI interface is busy with transmitting program data to the required location inside the CODSP. The time $\overline{\text{BUSY}}$ is low depends on the type of command. For example, the control word takes maximum 12 FRAME periods. When $\overline{\text{BUSY}}$ is low due to a write of the control word via one channel ($\overline{\text{CH0}}$ or $\overline{\text{CH1}}$), a control word via the other channel ($\overline{\text{CH1}}$ or $\overline{\text{CH0}}$) can be written. The commands are executed in the same order as they are programmed. When $\overline{\text{BUSY}}$ is low, due to execution of a previous command, the user must wait until $\overline{\text{BUSY}}$ is high again before issuing any new command.

6.4 PROGRAMMABILITY OF THE SH-POTS CHIPSET

The following sections describe how the SH-POTS chipset can be programmed.

6.4.1 Software Reset of the Chipset

The software reset unconditionally forces the chipset into the reset state. It can be activated by writing 1 byte via either of the two $\overline{\text{CH*}}$ signals.

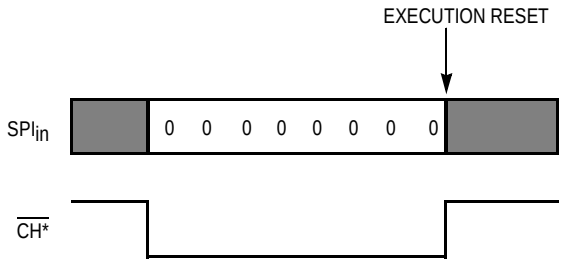
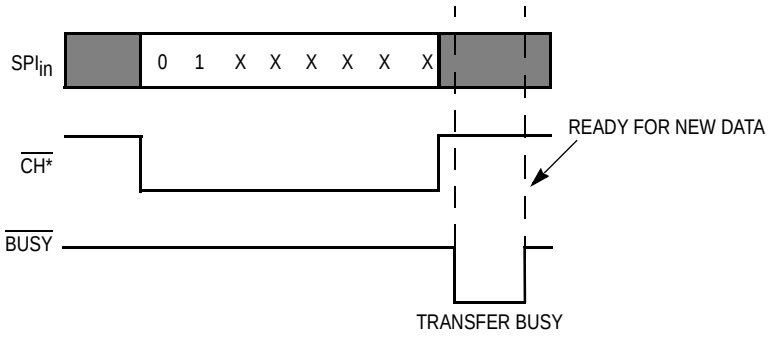


Figure 6-3. Software Reset

6.4.2 Control Word

The control word provides an easy and fast access to the operating states of the chipset. Both lines have thier own dedicated control word. The difference is usually chosen by the use of the corresponding $\overline{\text{CH0}}$ signal for line 0 and $\overline{\text{CH1}}$ for line 1. It is also possible to address both lines by any $\overline{\text{CH*}}$ signal activation. The control word is a 1-byte command.



NOTE: Activating $\overline{CH0}$ or $\overline{CH1}$ program the corresponding channel.

Figure 6-4. Write Control Word

The bits have following functions.

Bit	Activation of	When
7	Always 0 for Control Word	
6	Always 1 for Control Word	
5	TBD (see Note)	1
4	TBD (see Note)	1
3	Polarity Reversal	1
2	Power-Up (ADSI Mode)	1
1	Ringing Mode	1
0	Metering	1

NOTE: Bits should always be written 0, foreseen for future extension.

6.4.3 Access to the CODSP Memory

The first byte of these commands all begin with B7-6 = 10. (They are exactly the same commands as the MS140131KT SH-POTS chipset with GCI interface.).

The $\overline{BUSY}$ signal becomes low after acceptance of the commands (when all required bytes are received) and remain low during execution of the command. When the result is available at the SPI_{out} pin, the $\overline{BUSY}$ signal becomes high again.

6.5 ID REQUEST

There is one required byte. The command returns 2 bytes that are the software revision of the CODSP (see explanation in the MS140131KT SH-POTS datasheet). The command itself is not echoed.

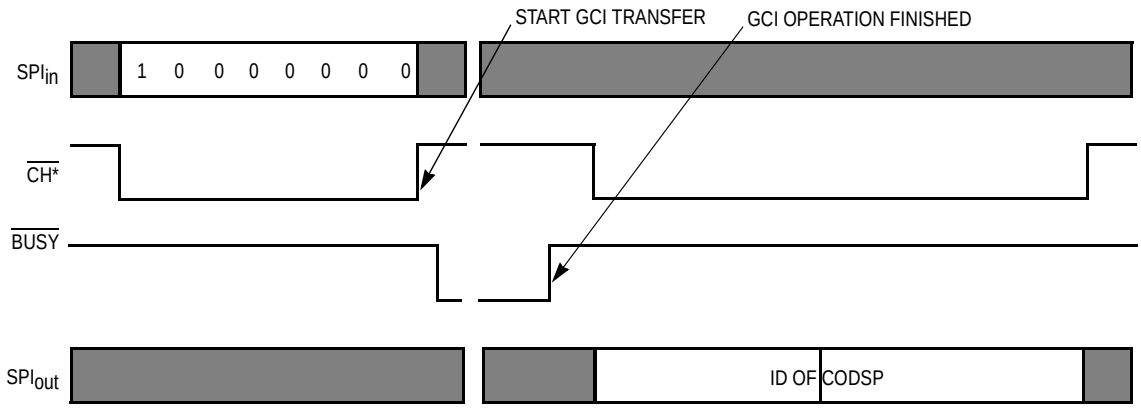


Figure 6-5. ID Request

6.6 READ REQUEST

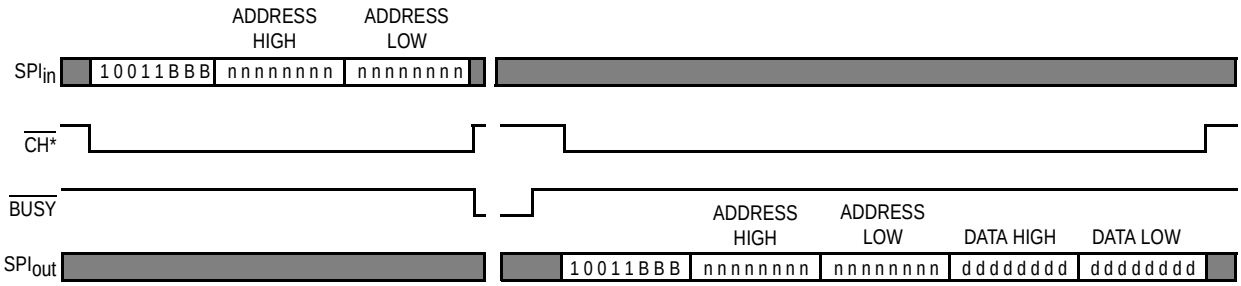


Figure 6-6. Read Request

This is a 3-byte command, which returns 2 bytes; the codec-memory contents at the specified address. The read request is exactly the same as in the SH-POTS GCI interface description. See explanation in the MS140131KT SH-POTS datasheet. The command itself is not returned.

6.7 WRITE REQUEST

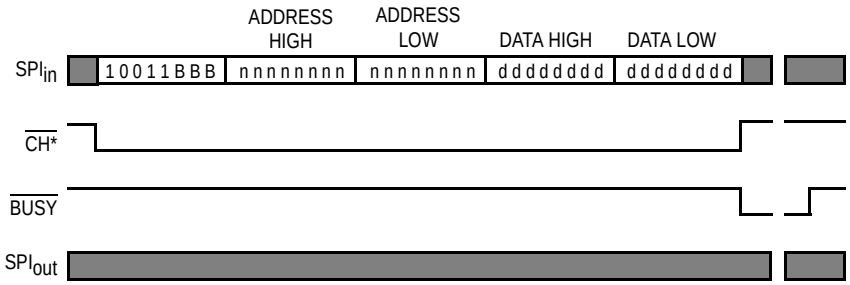


Figure 6-7. Write Request

This is a 5-byte command (see explanation in the MS140131KT SH-POTS datasheet).

6.8 PROGRAMMING OTHER FEATURES VIA THE SPI INTERFACE

The SPI interface has a memory map in which the setup for the PCM interface can be changed, as well as the clock frequency and the signaling pin. See Section 6.12 for a description of the memory map.

6.8.1 Write SPI Interface Memory

Each address can be written to via the SPI interface independently. The command to be used is 111YYYYY + byte to be loaded in the register. The address is defined by YYYYY. It is possible to write more than 1 byte with the same command. For this, the relevant $\overline{\text{CH*}}$ signal has to be pulled low for a multiple of 8 clocks. Each time, the byte with the address = previous +1 is written. For valid addresses, see memory map.

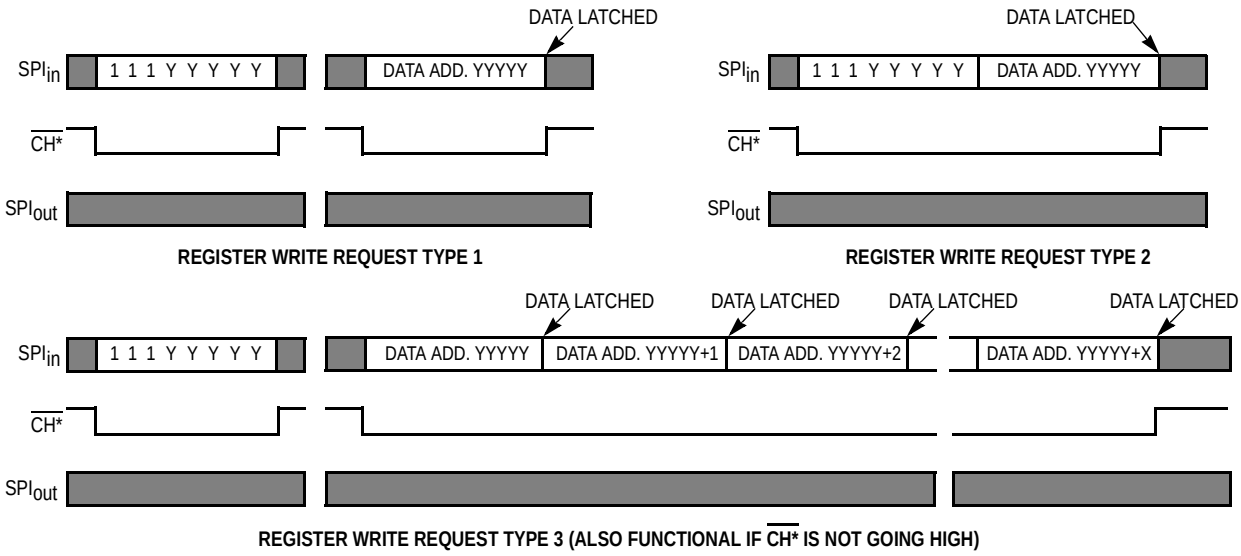


Figure 6-8. Register Write Request Types

6.8.2 Read SPI Interface Memory

Read operation will return the data of the corresponding register. The data is sampled during the bytes following the request, on condition that the idle command is written during the access of the SPI interface.

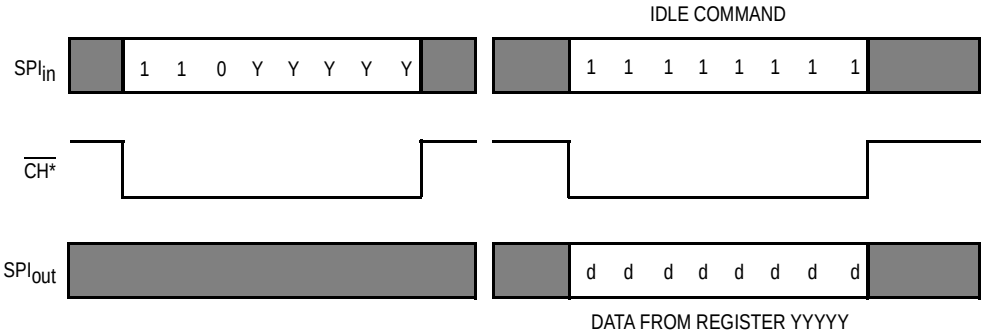


Figure 6-9. Register Read Request

6.9 IDLE COMMAND

This command is used to read the data from the SPI_{out} pin and has no programming effect in the PCM2GCIM interface block. FF is returned via SPI_{out} if no data is available.

6.10 REGISTERS IN THE SPI INTERFACE BLOCK

There are 11 addressable registers: from 0x05 to 0x0F (hex), and 0x11(hex). These registers are used to control the functions of other interface blocks: PCM interface, GCI interface, and clock generator. These registers are controlled by the SPI interface.

Addresses	Control of:
5	Which Signaling Signal is Directed to $\overline{\text{DET}}$*
6	Direct C/I bits programming
7	PCMCLK Frequency
8 – D	PCM Interface
E – F	Control Word Registers
11	Direct C/I Bits Monitoring

Table 6-3 lists the memory map and function.

Table 6-3. Memory Map: SPI

Address (Hex)	Function Write Registers	Default	Content When Read
5	$\overline{\text{DET}}$* pins control register. See Section 5.7.	90	Idem
6	Normal SH-POTS GCI Downstream C/I bits (B7-2): see SH-POTS, excluding the AE bits.	FF (non-active)	Idem
7	PCMCLK clock frequency: the user must program the applied clock frequency at PCMCLK pin as a multiple of 512 kHz. Program B7-4 = B3-0: — 1 x 512 to 15 x 512 write 0001 to 1111 — 16 x 512 write 0000	44 (2048 kHz)	Idem
8	PCM_{in} delay versus FRAME rising edge for line 0 per byte (B6-0: channel 0 – 127), default is 0 bytes. B7 is always = 0.	00	Idem
9	PCM_{out} delay versus FRAME rising edge for line 0 per byte (B6-0: channel 0 – 127), default is 0 bytes. Activation of the channel = B7, default = 0 = deactivated.	00	Idem
A	PCM delay versus FRAME rising edge for line 0 per bit, default is B7-5 = 0; B4 = 1/2 clock period only for PCM_{out}, other bits are for expansion and should be programmed 0.	00 (no shift)	Idem
B	PCM_{in} delay versus FRAME rising edge for line 1 per byte (B6-0: channel 0 – 127), default is 1 byte. B7 is always = 0.	01	Idem
C	PCM_{out} delay versus FRAME rising edge for line 1 per byte (B6-0: channel 0 – 127), default is 1 byte. Activation of the channel = B7, default = 0 = deactivated.	01	Idem

Table 6-3. Memory Map: SPI (continued)

Address (Hex)	Function Write Registers	Default	Content When Read
D	PCM delay versus FRAME rising edge for line 1 per bit, default is B7-5 = 0; B4 = 1/2 clock period only for PCM_{out}, other bits are for expansion and should be programmed 0.	00 (no shift)	Idem
E	Control word Channel 0. See Section 6.4.2.	40	Idem
F	Control word Channel 1. See Section 6.4.2.	40	Idem
11	NA. Remark: Writing to this register may put the system into an undefined mode.	FF	Normal GCI upstream C/I bits (B7-2): see the MS140131KT datasheet. Some bits can be sent to outputs $\overline{DET}$*. Bits 1-0 are always High.

Registers 0 to 4 and higher then 11 are for internal use only. Writing to these registers may put the system into an undefined mode.

6.11 PROGRAMMING THE PCM INTERFACE

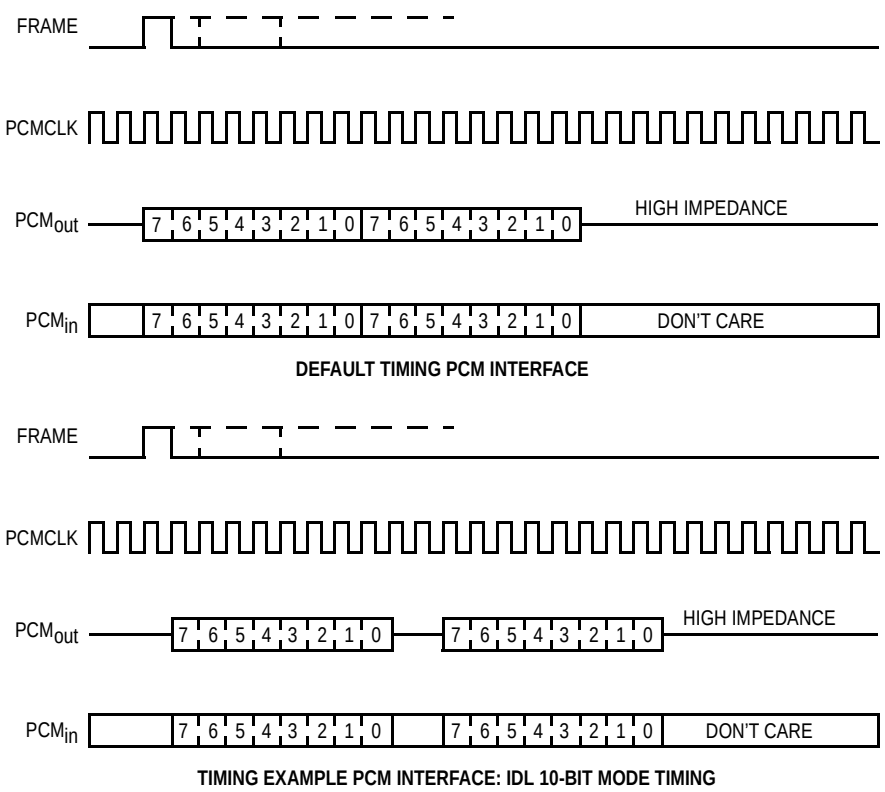
The PCM interface consists of inputs PCMCLK, FRAME, PCM_{in}, and output PCM_{out}. PCMCLK controls the internal operation of the PCM interface and shifts/latches the PCM data from PCM_{in} in the interface on its falling edge, and sends the PCM data onto PCM_{out}* on its rising edge. The data is read/written in the B-channels of the GCI interface via the control block.

FRAME is an 8-kHz frame-sync pulse. Its rising edge determines the beginning of the PCM data transfer out of PCM_{out} and into PCM_{in}. A register in the interface block defines the shift between this FRAME signal and the corresponding PCM channel. Default values are as defined in the interface block register map.

The FRAME pulse is one or more PCMCLK periods long, with timing relationships as specified in Figure 6-10. The PCM_{out} open drain output buffer is enabled with reference to the rising edge of FRAME or the rising edge of PCMCLK, depending on whichever comes later, and the first bit clocked out is the PCM sign bit. The following 7 rising edges of PCMCLK shift out the remaining 7 bits, MSB first. Default compression of PCM data is A-law as defined in the CODSP core. The PCM_{out} output is disabled by the falling edge of PCMCLK following the eighth rising edge. A rising edge of the FRAME will cause PCM data at PCM_{in} to be latched after the last of the next 8 falling edges of PCMCLK.

See register 8-D for a description of how the activation and time delay can be programmed.

Figure 6-10 is an example of the default timing and programming a different setup.



NOTE: Default values +
Program Reg. A = 20 and D = 60 for timing shift
Program Reg. 9 = 80 for activation line 0
Program Reg. C = 81 for activation line 1.

Figure 6-10. Timing Example of PCM Interface

6.12 MEMORY MAP OF THE CODSP

Global memory map and MemID definitions:

- All addresses can be read and written, though writing to locations or individual bits which are not described here may result in unpredictable behavior.
- The default parameter and coefficient values that are used at startup and after reset are listed in the following tables.
- The memory block to be accessed is given as part of the READ or WRITE command (see above) as the “B” bits in the command byte.
- The control registers of the SH-POTS system, accessed via the SPI, are organized in a number of memory blocks. Within each block, a number of addresses are used directly to control the operation of specific functions of the SH-POTS system.

Table 6-4. Memory Map for CODSP

MemID	Memory	Start Address	Memory Contents
2	Data RAM	0x 02 0000	C-code read/write data C-code stack region C-code IRQ stack region
4	Coprocessor Coef RAM	0x 04 0000	Filter coefficients
5	Shared RAM	0x 05 0000	Data packet buffers Label vectors, FIFO control

6.13 DATA RAM — MEMID = 2

Table 6-5. Data RAM: Memory Map

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00 (0x0000)										Bbs0		Bsa0	Bs0	Br0	Tst0	Sh0
01 (0x0001)										Bbs1		Bsa1	Bs1	Br1	Tst1	Sh1
02 (0x0002)																
03 (0x0003)	Tx Gain 0															
04 (0x0004)	Tx Gain 1															
05 (0x0005)	Rx Gain 0															
06 (0x0006)	Rx Gain 1															
07 (0x0007)															Dzd1	Dzd0
08 (0x0008)															Td1	Td0
09 (0x0009)	CurLim_Rlarge								CurLim_Threshold							
10 (0x000A)											RW		RIL	RM	RF	
11 (0x000B)	Ringing_DC_Offset								Ringing_Amplitude							
12 (0x000C)	Ringing_Off_Period								Ringing_On_Period							
13 (0x000D)													LBO			
14 (0x000E)	RTDAC_ThresholdLow								RTDAC_ThresholdHigh							
15 (0x000F)	RTDAC_Debouncetime								RTDAC_GapTime							
16 (0x0010)														AlarmReg		
17 (0x0011)	IDC0								IDC1							
18 (0x0012)	IAC0															
19 (0x0013)	IAC1															
20 (0x0014)													TG1	TG0	MS1	MS0
21 (0x0015)									TestTone_Ampl1_L0							
22 (0x0016)									TestTone_Ampl1_L1							
23 (0x0017)									TestTone_Ampl2_L0							
24 (0x0018)									TestTone_Ampl2_L1							

Table 6-5. Data RAM: Memory Map (continued)

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
25 (0x0019)	TestTone_Freq1_L0															
26 (0x001A)	TestTone_Freq1_L1															
27 (0x001B)	TestTone_Freq2_L0															
28 (0x001C)	TestTone_Freq2_L1															
29 (0x001D)									ACG							
30 (0x001E)			Sleep2		Pd1	Pd0					Rzd1	Rzd0		Sleep1		
31 (0x001F)	DialP_SatTxLevel															
32 (0x0020)	DialP_DebTime															

NOTE: Bit positions and memory locations not documented must not be changed.

6.14 LBO REGISTER

This register controls various loopback modes, as well as the routing of the GCI B channels to or from the physical line analog channels. The bits are codes as shown in Table 6-6.

Table 6-6. LBO Register Description

Mode	D2	D1	D0	GCI Side	Analog Side
Normal	0	0	0	Tx(0) -> B1Up Tx(1) -> B2Up	B1Down -> Rx(0) B2Down -> Rx(1)
Simplex loop B2	0	0	1	Tx(0) -> B1Up B2Down -> B2Up	B1Down -> Rx(0) Tx(1) -> Rx(1)
Simplex loop B1	0	1	0	B1Down -> B1Up Tx(1) -> B2Up	Tx(0) -> Rx(0) B2Down -> Rx(1)
Simplex loop B1 and B2	0	1	1	B1Down -> B1Up B2Down -> B2Up	Tx(0) -> Rx(0) Tx(1) -> Rx(1)
Duplex loopback	1	0	0	B2Down -> B1Up B1Down -> B2Up	Tx(0) -> Rx(1) Tx(1) -> Rx(0)
Reserved	1	0	1		
Reserved	1	1	0		
Swap mode	1	1	1	Tx(0) -> B2Up Tx(1) -> B1Up	B1Down -> Rx(1) B2Down -> Rx(0)

NOTE: BnDown: GCI B channel 1 or 2, downstream direction.
BnUp: GCI B channel 1 or 2, upstream direction.
Tx(m): Analog “transmit” signal (upstream direction), line 1 or 2.
Rx(m): Analog “receive” signal (downstream direction), line 1 or 2.

6.15 ALARM BITS

- After initialization (e.g., due to a hardware reset), the CODSP itself will make the upstream Alarm bit active, and set the AlarmReg with an InitRequest value (i.e., “1xx”). The Alarm bit will remain active until the InitRequest is cleared by the PCM/SPI supervisor (indicating that the supervisor has done the necessary reinitialization of system parameters).
- In order to check the contents of the AlarmReg, execute the following PCM/SPI command:

```
ReadRequest ( MemId=2, Add=0x0010 );
```

This results in a four-nibble value; e.g., “0xabgd,” read by the supervisor.

- In order to clear the InitRequest alarm, in principle, one must only clear one bit. Therefore, the supervisor should execute the following commands:

```
NewValue = "0xabgd" AND "0xFFFB";
WriteRequest ( MemId=2, Add=0x0010, NewValue );
```

- Note that the other bits in the alarm register are updated by the DSP at a 8 kHz rate, and that they are only used by the PCM/SPI supervisor; therefore, the other bits might also be overwritten for one cycle, clearing all bits (inclusive the InitRequest bit) in one command:

```
WriteRequest ( MemId=2, Add=0x0010, 0x0000 );
```

6.16 MEANING AND DEFAULT VALUES OF THE PARAMETERS

Table 6-7. Data RAM: Description and Default Values

Name (Note 1)	Address	Position	Description	Mapping	Default
Sh0, Sh1	00, 01	0	SHLIC test mode control bit	0: normal mode 1: test mode	0 (normal)
Tst0, Tst1	00, 01	1	SHLIC test switch control bit	0: open switch 1: closed switch	0 (open)
Br0, Br1	00, 01	2	SHLIC battery reversal control bit	0: non-reversed 1: reversed	0 (non rev.)
Bs0, Bs1	00, 01	3	SHLIC battery selection control bit for NonAct_X variant	0: BATS selection L 1: BATR selection H	0 (NonAct_L)
Bsa0, Bsa1	00, 01	4	SHLIC battery selection control bit for ActAdsi_X variant	0: BATS selection L 1: BATR selection H	0 (ActAdsi_L)
Bbs0, Bbs1	00, 01	6:5	SHLIC battery selection control bit for ActRng_Sph_X variant	0 = “00”:BATS L 1 = “01”:BATR H 2 = “10”:BATS + bias LA 3 = “11”:BATR + bias HA	0 (ActRng_Sph_L)

Table 6-7. Data RAM: Description and Default Values (continued)

Name (Note 1)	Address	Position	Description	Mapping	Default
Tx_Gain_0 Tx_Gain_1	03 04	15:0	Gain factor in Tx direction for Line0 and Line1	$20 \log \frac{\text{Tx-Gain\_*}}{320}$	320 (0 dB)
Rx_Gain_0 Rx_Gain_1	05 06	15:0	Gain factor in Rx direction for Line0 and Line1	$-7 + 20 \log \frac{\text{Rx-Gain\_*}}{384}$	384 (– 7dB)
Dzd1, Dzd0	07	1:0	Disable digital Z_{CO} path	0: enable 1: disable	1 (disabled)
Td1, Td0	08	1:0	Disable Tx path at pdm level	0: enable 1: disable	0 (enabled)
CurLim_Threshold	09	7:0	Current limitation threshold parameter	val = 0 ... 127 unit = 0.63 mA (eq = 0 ... 80 mA)	51 (32 mA)
CurLim_RLarge	09	15:8	Current limitation RLarge resistance parameter (internal resistance)	val = 0 ... 210 unit = 47 (eq = 0 ... 10 kΩ)	64 (3 kΩ)
RF	10	1:0	Ringing frequency	0 = “00”: 16 Hz 1 = “01”: 20 Hz 2 = “10”: 25 Hz 3 = “11”: 50 Hz	3 (50 Hz)
RM	10	2	Ringing mode	0: on/off mode 1: burst mode	0 (on/off)
RIL	10	3	Enable interleaved ringing	0: non-interleaved 1: interleaved	1 (interleaved)
RW	10	5	Ringing waveform	0: sine wave 1: trapezoidal wave	0 (sine)
Ringing_Amplitude	11	7:0	Amplitude of ringing signal	val = 0 ... 255 unit = 194 mV rms	255 (max ampl)
Ringing_DC_Offset	11	15:8	DC offset of ringing signal (Between A and B wire)	val = 0 ... 255 unit = 250 mV	0 (no offset)
Ringing_On_Period	12	7:0	Length of active ringing phase to be used in burst mode	val = 0 ... 255 unit = 32 ms	32 (1 s)
Ringing_Off_Period	12	15:8	Length of silent ringing phase to be used in burst mode	val = 0 ... 255 unit = 32 ms	96 (3 s)
LBO	13	3:0	GCI loopback register (encoding see below)	val = 0 ... 15	0 (no loop)
RTDAC_ThresholdHigh	14	7:0	Threshold level high during ringing	val = 0 ... 255 unit = 1.6 mA	27 (43.2 mA)
RTDAC_ThresholdLow	14	15:8	Threshold level low during ringing	val = 0 ... 255 unit = 1.6 mA	7 (11.2 mA)
RTDAC_GapTime	15	7:0	Gaptime during RTDAC peak detection	val = 0 ... 255 unit = 125 µs	10 (1.25 ms)

Table 6-7. Data RAM: Description and Default Values (continued)

Name (Note 1)	Address	Position	Description	Mapping	Default
RTDAC_Debouncetime	15	15:8	Deb. time during RTDAC	val = 0 ... 255 unit = 125 µs	240 (30 ms)
AlarmReg	16	2:0	Alarm status register (encoding)	val = 0 ... 7	4 (InitReq'st)
IDC1	17	7:0	DC line current of Line1, sampled at 2 kHz	val = 0 ... 127 unit = 0.63 mA	0
IDC0	17	15:8	DC line current of Line0, sampled at 2 kHz	val = 0 ... 127 unit = 0.63 mA	0
IAC0	18	15:0	AC line current of Line0, sampled at 8 kHz	unit = 215/1.6 V @ Tx	0
IAC1	19	15:0	AC line current of Line1, sampled at 8 kHz	unit = 215/1.6 V @ Tx	0
TG1, TG0	20	3, 2	Tone generator control bit for Line1 and Line0	0 : do not add tone 1 : add tone	0 (no tone)
MS1, MS0	20	1, 0	Mute speech control bit for Line1 and Line0	0 : pass speech 1 : mute speech	0 (no mute)
TestTone_Ampl1_L0 TestTone_Ampl1_L1	21 22	7:0	Amplitude of first sine for Line0 and Line1	val = 0 ... 255	63 (0 dBm)
TestTone_Ampl2_L0 TestTone_Ampl2_L1	23 24	7:0	Amplitude of second sine for Line0 and Line1	val = 0 ... 255	63 (0 dBm)
TestTone_Freq1_L0 TestTone_Freq1_L1	25 26	15:0	Frequency of first sine for Line0 and Line1	unit = 250 Hz/256	1024/256 (1 kHz)
TestTone_Freq2_L0 TestTone_Freq2_L1	27 28	15:0	Frequency of second sine for Line0 and Line1	unit = 250 Hz/256	512/256 (500 Hz)
ACG	29	7:0	Rx amplitude correction for Z_{CO} synthesis	val = 0 ... 255/128	103/128 (600 Ω)
Pd1, Pd0	30	11:10	Power denial mode Line1	1 = enable 0 = disable	0 (disable)
Sleep2 (Note 2)	30	13:12	Low power activation	00 = inactive 11 = active	00 active
Sleep1 (Note 2)	30	2:0	Sleep factor to be used when one line inactive	val = 0 ... 7 eq = 0 ... 70% sleepy	0 (0% sleep)
Rzd1, Rzd0	30	4:3	Disable analog Z_{CO} path	0: enable 1: disable	0 (enabled)
DialP_SatTxLevel	31	15:0	Tx saturation level to be used for dial pulse detection	unit = 48.83 µV @ Tx	8192 (400 mV)
DialP_DebTime	32	15:0	Debounce time to be used for dial pulse detection	unit = 125 µs	40 (5 ms)

NOTES: 1. Parameter names with 0 or 1 at the end refer to the analog Line0 or Line1.

2. In low power applications: recommended program value is sleep 1 = 5 combined with sleep 2 = 3 will save power consumption when only one line off-hook.

6.17 COPROCESSOR COEFFICIENT RAM — MEMID = 4

Access is similar to that of the data RAM parameters. Note, however, that the PCM/SPI commands work with 2-byte values whereas the memory contains only 3-nibble values. Because all values are <12, 0>, the most significant nibble of the 2-byte PCM/SPI value will be a sign-extension of the 12-bit value. In the case of a ReadRequest; the most significant nibble of a WriteRequest will be neglected.

Table 6-8. Coprocessor Coefficient RAM: Memory Map

Address	11	10	9	8	7	6	5	4	3	2	1	0
00 (0x0000)	Rx32KFilter coefficient : r0											
01 (0x0001)	r1											
02 (0x0002)	r4											
03 (0x0003)	s1											
04 (0x0004)	s2											
05 (0x0005)	r2											
06 (0x0006)	r3											
07 (0x0007)	r5											
08 (0x0008)	s3											
09 (0x0009)	s4											
10 (0x000A)	m0											
11 (0x000B)	m1											
12 (0x000C)	u0											
13 (0x000D)	u1											
14 (0x000E)	Hyb16KFilter coefficient : h0											
15 (0x000F)	h1											
16 (0x0010)	h2											
17 (0x0011)	h3											
18 (0x0012)	a0											
19 (0x0013)	c5											
20 (0x0014)	b0											
21 (0x0015)	Tx32KFilter coefficient : t0											
22 (0x0016)	t1											
23 (0x0017)	t8											
24 (0x0018)	q1											
25 (0x0019)	q2											
26 (0x001A)	t2											
27 (0x001B)	t3											
28 (0x001C)	t9											

Table 6-8. Coprocessor Coefficient RAM: Memory Map (continued)

Address	11	10	9	8	7	6	5	4	3	2	1	0
29 (0x001D)	q3											
30 (0x001E)	q4											
31 (0x001F)	t4											
32 (0x0020)	t5											
33 (0x0021)	t10											
34 (0x0022)	q5											
35 (0x0023)	t6											
36 (0x0024)	t7											
37 (0x0025)	t11											
38 (0x0026)	q6											
39 (0x0027)	q7											
40 (0x0028)	c2											
41 (0x0029)	c3											
42 (0x002A)	ZcoTxFilter coefficient : Ftx											
43 (0x002B)	Ap											
44 (0x002C)	NAn											
45 (0x002D)	Constants : HLF											
46 (0x002E)	ONE_EIGHT											

6.18 MEANING AND DEFAULT VALUES OF THE PARAMETERS

Table 6-9. Coprocessor Coefficient RAM: Description and Default Values

Name	Address	Position	Description	Mapping	Default
r0	00	11:0	Rx filter coefficient	unit = intval / 512	int96
r1	01	11:0	Rx filter coefficient	unit = intval / 512	int78
r4	02	11:0	Rx filter coefficient	unit = intval / 512	int96
s1	03	11:0	Rx filter coefficient	unit = intval / 512	int642
s2	04	11:0	Rx filter coefficient	unit = intval / 512	int263
r2	05	11:0	Rx filter coefficient	unit = intval / 512	int256
r3	06	11:0	Rx filter coefficient	unit = intval / 512	int303
r5	07	11:0	Rx filter coefficient	unit = intval / 512	int256
s3	08	11:0	Rx filter coefficient	unit = intval / 512	int746
s4	09	11:0	Rx filter coefficient	unit = intval / 512	int450

Table 6-9. Coprocessor Coefficient RAM: Description and Default Values (continued)

Name	Address	Position	Description	Mapping	Default
m0	10	11:0	Rx filter coefficient	unit = intval / 512	int512
m1	11	11:0	Rx filter coefficient	unit = intval / 512	int512
u0	12	11:0	Rx filter coefficient	unit = intval / 512	int0
u1	13	11:0	Rx filter coefficient	unit = intval / 512	int0
h0	14	11:0	Echo cancelling coefficient	unit = intval / 512	int109
h1	15	11:0	Echo cancelling coefficient	unit = intval / 512	int2
h2	16	11:0	Echo cancelling coefficient	unit = intval / 512	int8
h3	17	11:0	Echo cancelling coefficient	unit = intval / 512	int32
a0	18	11:0	Echo cancelling coefficient	unit = intval / 512	int127
c5	19	11:0	Echo cancelling coefficient	unit = intval / 512	int512
b0	20	11:0	Echo cancelling coefficient	unit = intval / 512	int157
t0	21	11:0	Tx filter coefficient	unit = intval / 512	int48
t1	22	11:0	Tx filter coefficient	unit = intval / 512	int37
t8	23	11:0	Tx filter coefficient	unit = intval / 512	int48
q1	24	11:0	Tx filter coefficient	unit = intval / 512	int728
q2	25	11:0	Tx filter coefficient	unit = intval / 512	int439
t2	26	11:0	Tx filter coefficient	unit = intval / 512	int390
t3	27	11:0	Tx filter coefficient	unit = intval / 512	int492
t9	28	11:0	Tx filter coefficient	unit = intval / 512	int390
q3	29	11:0	Tx filter coefficient	unit = intval / 512	int573
q4	30	11:0	Tx filter coefficient	unit = intval / 512	int227
t4	31	11:0	Tx filter coefficient	unit = intval / 512	int64
t5	32	11:0	Tx filter coefficient	unit = intval / 512	int128
t10	33	11:0	Tx filter coefficient	unit = intval / 512	int64
q5	34	11:0	Tx filter coefficient	unit = intval / 512	int442
t6	35	11:0	Tx filter coefficient	unit = intval / 512	int384
t7	36	11:0	Tx filter coefficient	unit = intval / 512	int768
t11	37	11:0	Tx filter coefficient	unit = intval / 512	int384
q6	38	11:0	Tx filter coefficient	unit = intval / 512	int962
q7	39	11:0	Tx filter coefficient	unit = intval / 512	int458
c2	40	11:0	Tx filter coefficient	unit = intval / 512	int512
c3	41	11:0	Tx filter coefficient	unit = intval / 512	int512
Ftx	42	11:0	Z_{CO}Tx filter coefficient	unit = intval / 512	int237

Table 6-9. Coprocessor Coefficient RAM: Description and Default Values (continued)

Name	Address	Position	Description	Mapping	Default
Ap	43	11:0	Z_{CO}Tx filter coefficient	unit = intval / 512	int0
NAn	44	11:0	Z_{CO}Tx filter coefficient	unit = intval / 512	int0
HLF	45	11:0	Constant definition	unit = intval / 512	int256
ONE_EIGHT	46	11:0	Constant definition	unit = intval / 512	int64

6.19 SHARED MEMORY — MEMID = 5

Table 6-10. Shared Memory: Memory Map

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
85 (0x0055)		VLM				HT		Deb				MF	MM			
86 (0x0056)	SpiDo	SpiDi	SpiSk	SpiCs	SpiSe	RBD					SR*	SR*			SR*	SR*
87 (0x0057)			HSD_ThresholdHigh							HSD_ThresholdLow						
88 (0x0058)			RTD_ThresholdHigh							RTD_ThresholdLow						
89 (0x0059)	MeteringDutyCycle															
90 (0x005A)	ZcoShAlfa3		ZcoA2							Rxd*		Alo*		Sleep*		
91 (0x005B)					RZco				ZcoGamma				ZcoAlfa3			
94 (0x005E)															TL	

NOTE: Bit positions and memory locations not described here must not be changed.

6.20 MEANING AND DEFAULT VALUES OF THE PARAMETERS

Table 6-11. Shared Memory: Description and Default Values

Name	Address	Position	Description	Mapping	Default
VLM	85	14:11	Metering amplitude (unit value = depending on Z_{CO})	val = 0 ... 15	3
HT	85	10:9	HSD debounce time	0 = “00”: 8 ms 1 = “01” : 24 ms 2 = “10” : 16 ms 3 = “11”: 64 ms	2 (16 ms)
DEB	85	8	RTD debounce time	0 : 0 ms 1 : 30 ms	1 (30 ms)
MF	85	4	Metering frequency	0 : 12 kHz 1 : 16 kHz	1 (16 kHz)
MM	85	3	Metering mode	0 : burst mode 1 : on/off mode	1 (on/off)
SPIDO	86	15	SPI D_{out} port		0
SPIDI	86	14	SPI D_{in} port		0
SPISK	86	13	SPI SK port		0
SPICS	86	12	SPI CS port		0
SPISE	86	11	SPI port selection		0
RBD	86	10	Disable automatic ring activation of SPICK and SPICK	1 = disabled 0 = enabled	0 (enabled)
SR (Note 1)	86	5:4 1:0	Software resets of SID1, SID0, CP, GCI	1 = reset block 0 = no reset	0
Soft Resets (Note 2)	86	5:0	Reset ability of HW blocks (SID0, SID1, MRT, LS, CP, GCI)	0: no reset 1: reset block	0 (no reset)
HSD_ThresholdHigh	87	13:7	HSD high threshold	val = 0 ... 127 unit = 0.63 mA = 0 ... 80 mA	16 (10 mA)
HSD_ThresholdLow	87	6:0	HSD low threshold	val = 0 ... 127 unit = 0.63 mA = 0 ... 80 mA	10 (6.3 mA)
RTD_ThresholdHigh	88	13:7	RTD high threshold	val = 0 ... 127 unit = 0.63 mA = 0 ... 80 mA	16 (10 mA)
RTD_ThresholdLow	88	6:0	RTD low threshold	val = 0 ... 127 unit = 0.63 mA = 0 ... 80 mA	10 (6.3 mA)
MeteringDutyCycle	89	15:8	Length of the metering burst to be used in “burst” metering mode	val = 0 ... 255 unit = 2 ms = 0 ... 510 ms	150 (300 ms)

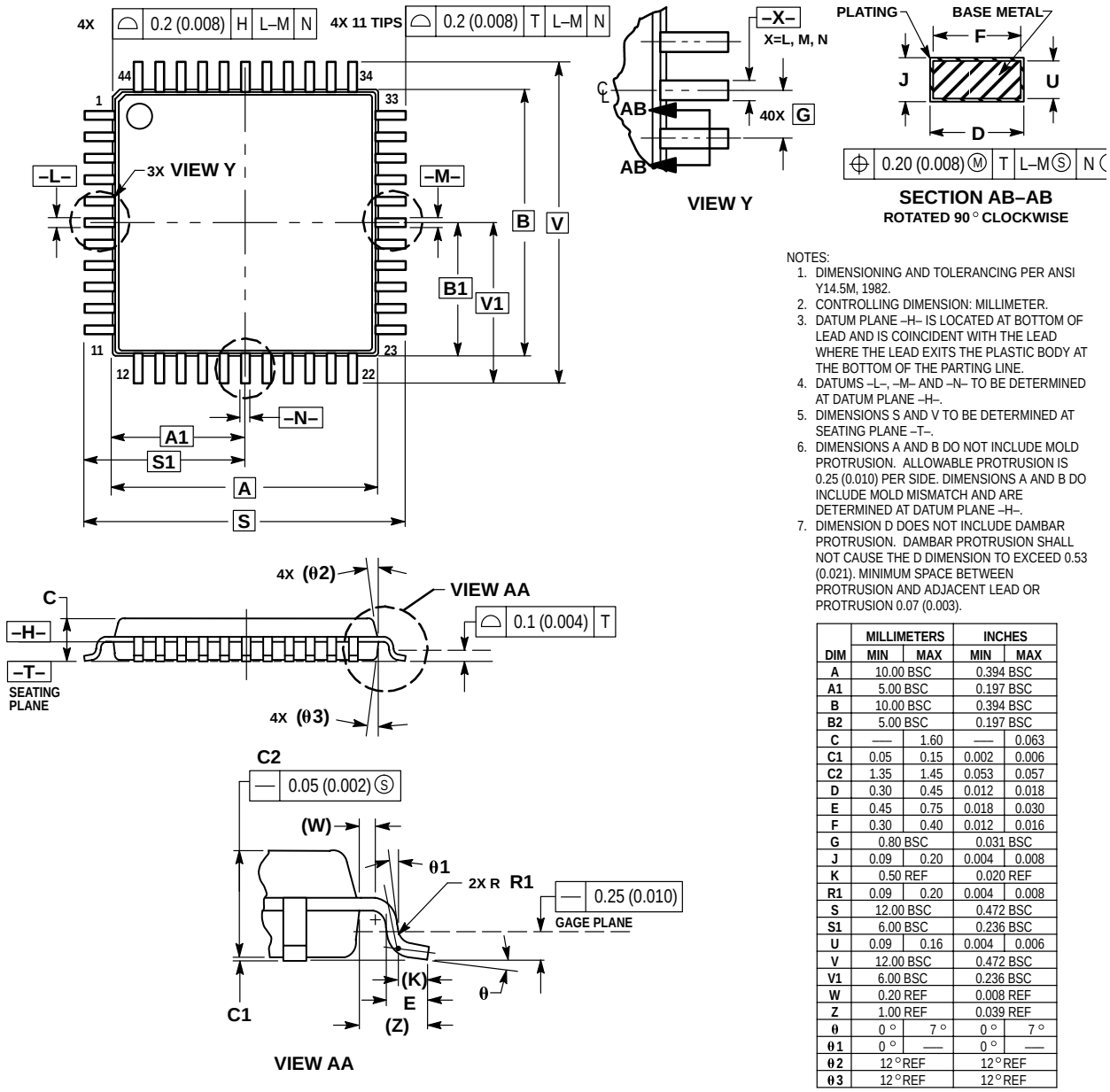
Table 6-11. Shared Memory: Description and Default Values (continued)

Name	Address	Position	Description	Mapping	Default
ZcoShAlfa3	90	15:1	Central office impedance parameter	(Note 1)	0 (600 Ω)
ZcoA2	90	13:7	Central office impedance parameter	(Note 1)	0 (600 Ω)
RxD (Note 1)	90	6	RxDisable at input of analog part	0: enabled Rx path 1: disable Rx path	0 (enabled)
ALO (Note 2)	90	4	Analog loopback at pdm	0: disabled loop 1: enable loop	0 (disabled)
Sleep (Note 2)	90	2:0	Sleep factor actually used by the processor	val = 0 ... 7 = 0 ... 70% sleepy	0 (0% sleep)
RZco	91	11:8	Central office impedance parameter	(Note 1)	3 (600 Ω)
ZcoGamma	91	7:4	Central office impedance parameter	(Note 1)	0 (600 Ω)
ZcoAlfa3	91	3:0	Central office impedance parameter	(Note 1)	0 (600 Ω)
TL	94	1:0	Transcode law selection	0 = “00”: A Law 1 = “01”: μ Law 2 = “10”: Linear	0 (A-Law)

NOTES: 1. Examples of other Z_{CO} parameters are listed in Table 4-4. Otherwise, contact a Motorola sales office.
2. Do not change these values.

SECTION 7
MECHANICAL SPECIFICATIONS
7.1 MC1420233 PACKAGE DIMENSIONS

FU SUFFIX
TQFP PACKAGE
CASE 824D-02

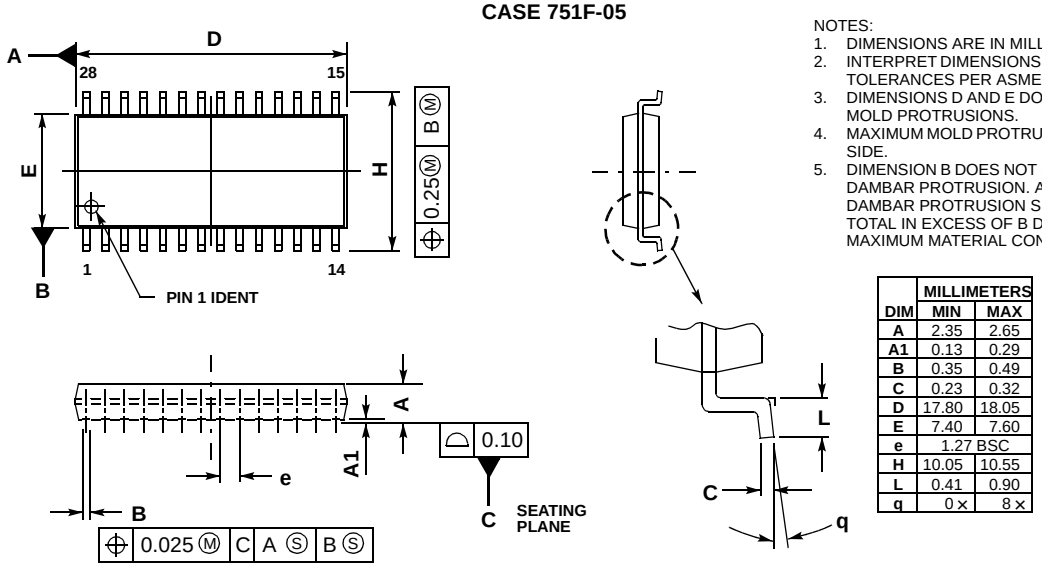


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.53 (0.021). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B2	5.00 BSC		0.197 BSC	
C	—	1.60	—	0.063
C1	0.05	0.15	0.002	0.006
C2	1.35	1.45	0.053	0.057
D	0.30	0.45	0.012	0.018
E	0.45	0.75	0.018	0.030
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
J	0.09	0.20	0.004	0.008
K	0.50 REF		0.020 REF	
R1	0.09	0.20	0.004	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	12° REF		12° REF	
θ3	12° REF		12° REF	

7.2 MC1430132 PACKAGE DIMENSIONS

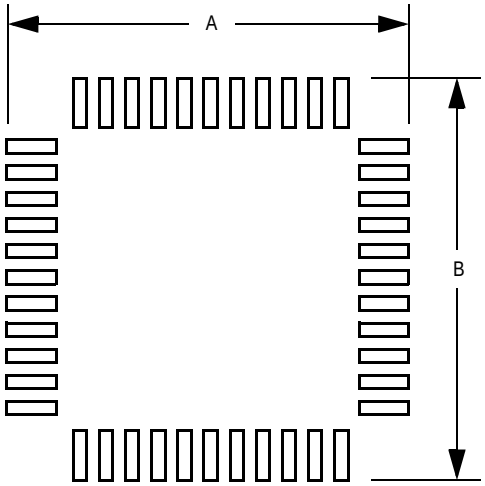
DW SUFFIX
SOIC PACKAGE
CASE 751F-05



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
4. MAXIMUM MOLD PROTRUSION 0.015 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
q	0 ×	8 ×

7.3 RECOMMENDED PAD LAYOUT FOR 44-LEAD TQFP MC1420233



Solder Pad Size: W = 0.55 mm x L = 2.0 mm

Solder Pad Pitch: 0.8 mm (center to center)

Toe to Toe Dimension: A = 14.2 mm x B = 14.2 mm

Figure 7-1. Recommended Pad Layout for 44-Lead TQFP MC1420233

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