8-BIT ADDRESSABLE LATCHES

GENERAL DESCRIPTION

The MMC 4099 and MMC 4599 are 8 bit addressable latches. Data is entered in serial form when the appropiate latch is addressed (via address pins A0, A1, A2), and write disable is in the low state.
Chip enable must be high for writing into MMC 4599. For the MMC 4599 the data pin is a bidirectional data port and for the MMC 4099 the input is a unidirectional write only port.
The Write/Read line controls this port in the MMC 4599.
The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, Write/Read or Chip Enable.
A Master Reset capability is available on both parts.

FEATURES

- Serial Data Input
- Parallel Output
- Low Input Capacitance 5.0 pF typical
- Master Reset
- Noise Immunity 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low Power TTL Loads, One Low Power Schottky TTL Load or Two HTL Loads over the Rated Temperature Range

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_I	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature: G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

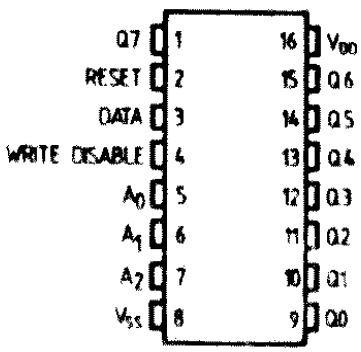
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

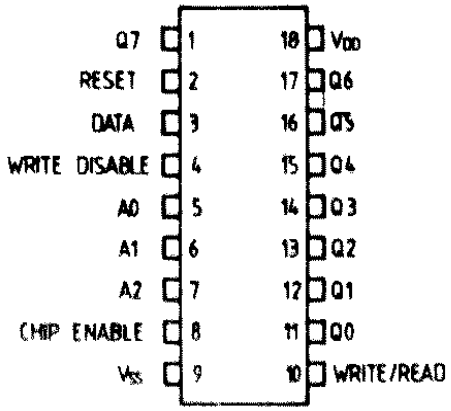
V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_I	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature: G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAMS

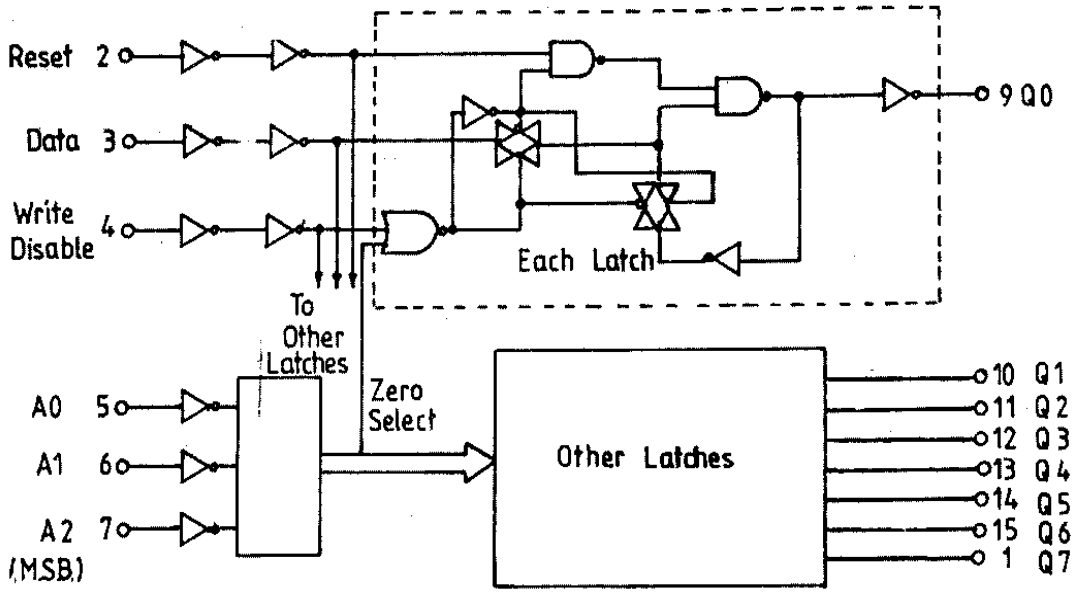
MMC 4099



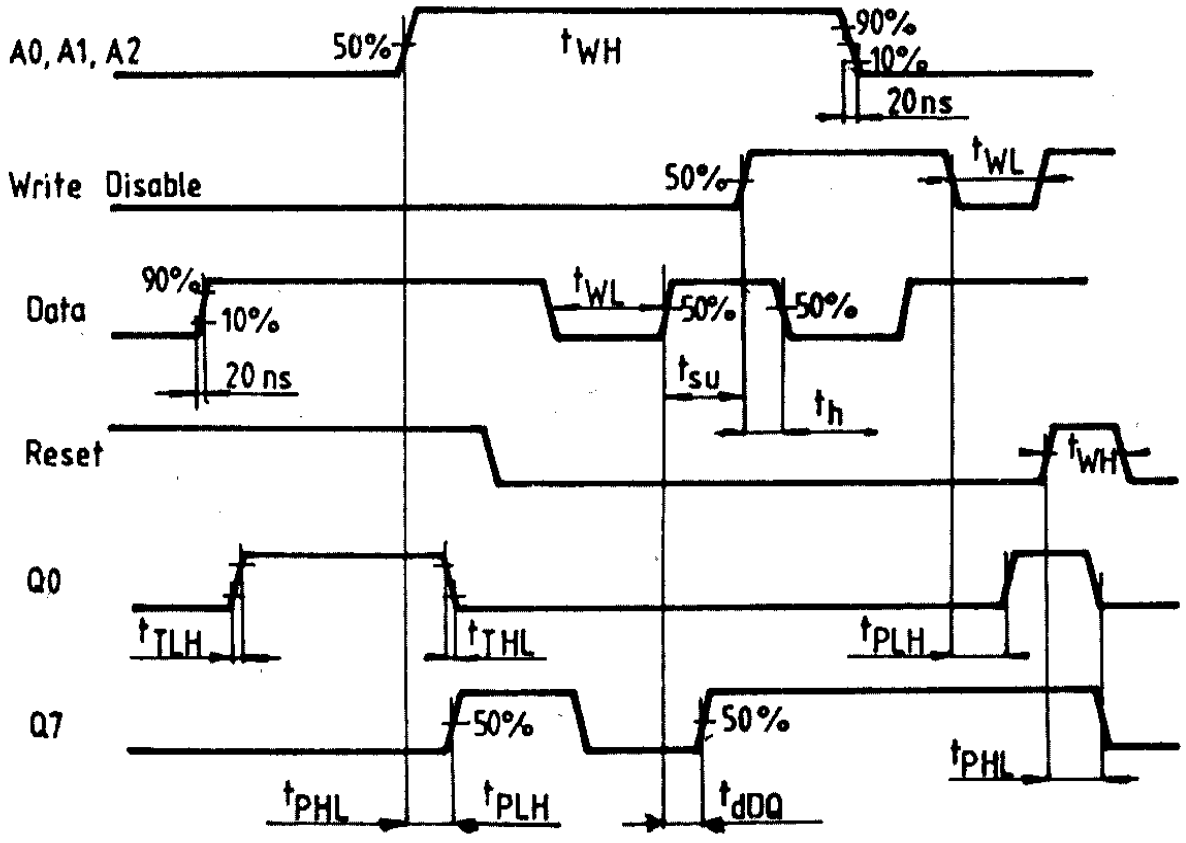
MMC 4599



FUNCTIONAL DIAGRAM - MMC 4099



TIMING DIAGRAM - MMC 4099

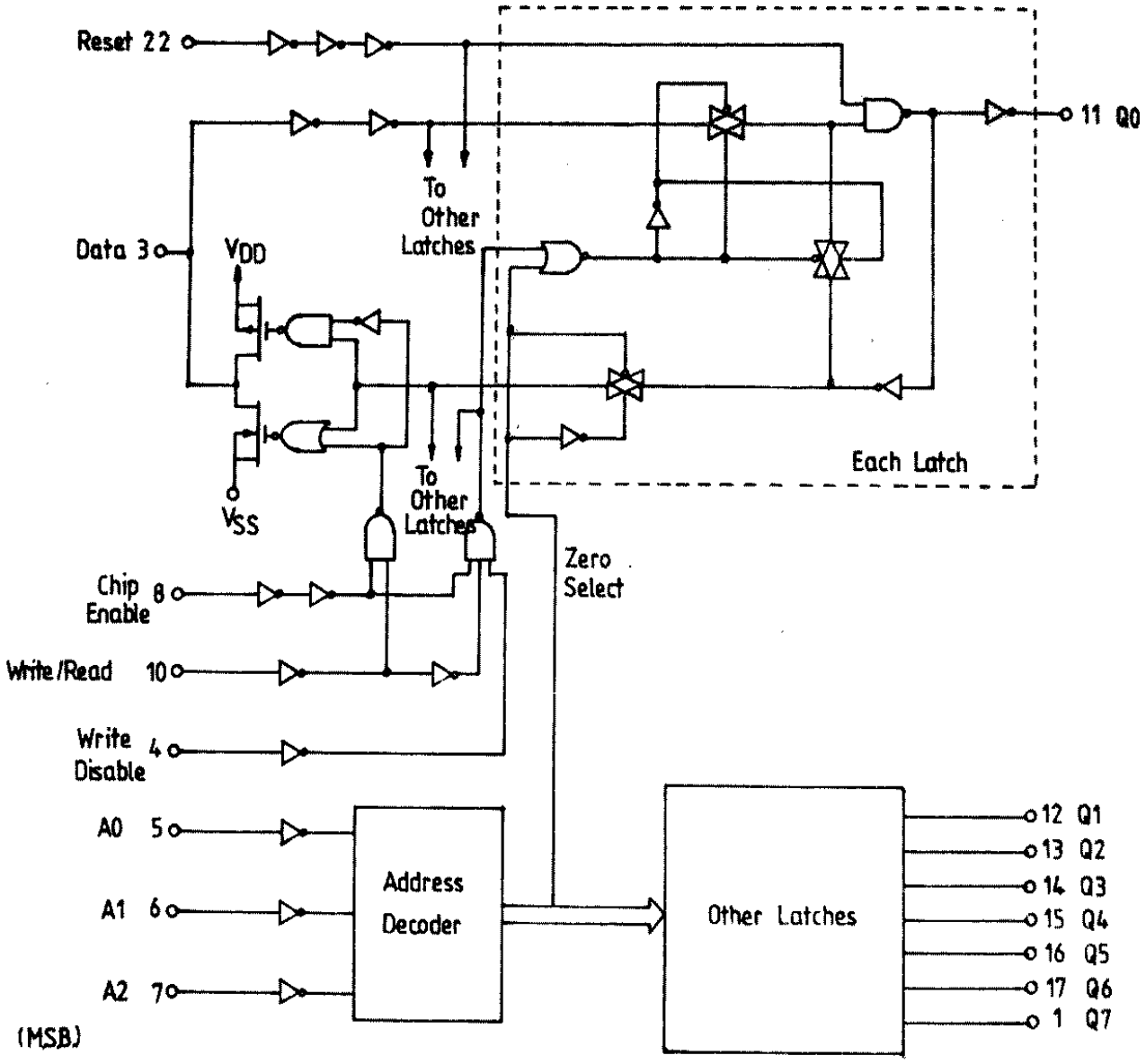


TRUTH TABLE - MMC 4099

Write Disable	Reset	Addressed Latch	Unaddressed Latch
0	0	Data	Q_n ✲
0	1	Data	Reset
1	0	Q_n ✲	Q_n ✲
1	1	Reset	Reset

✲ Q_n is previous state of latch

FUNCTIONAL DIAGRAM - MMC 4599

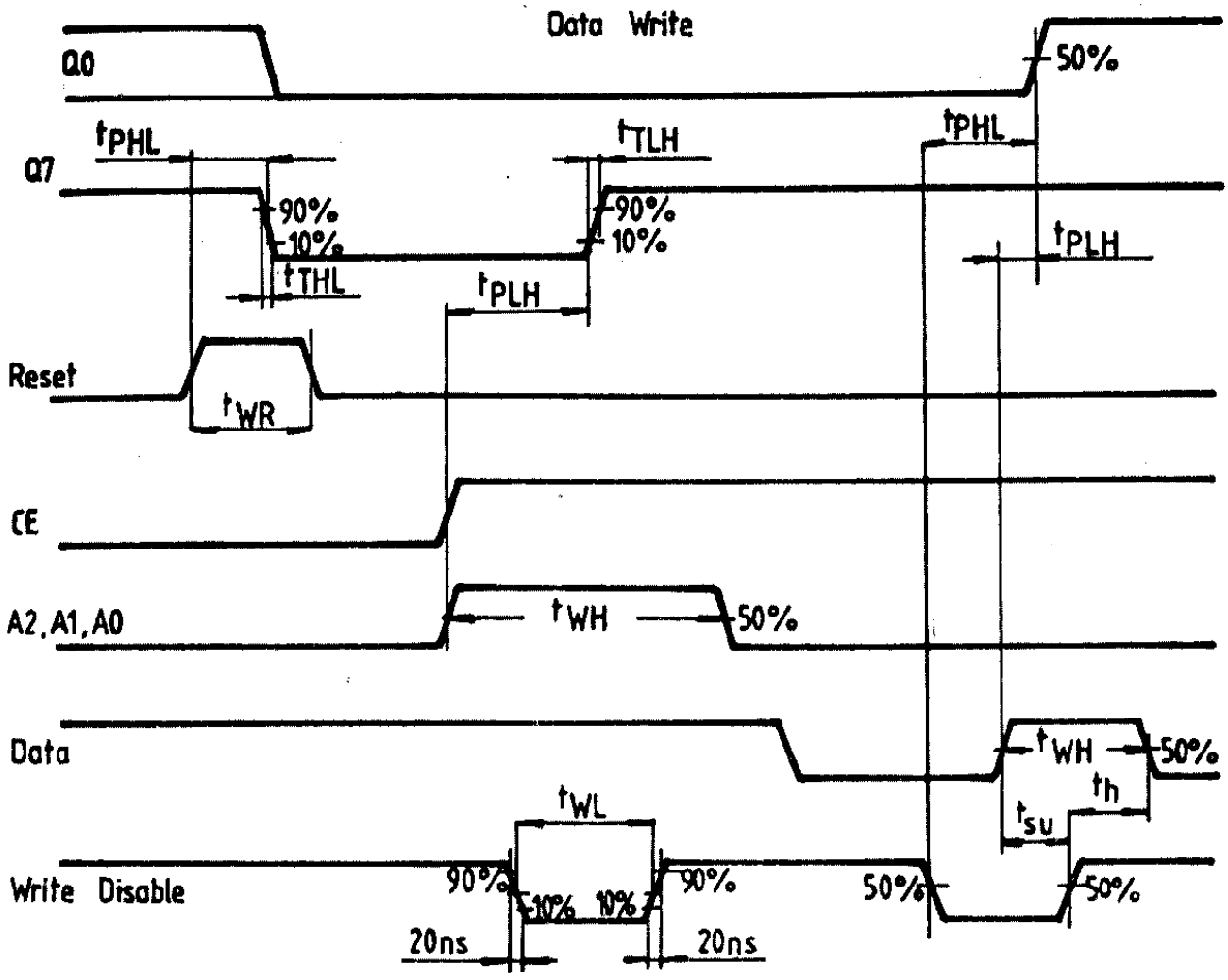


TRUTH TABLE - MMC 4599

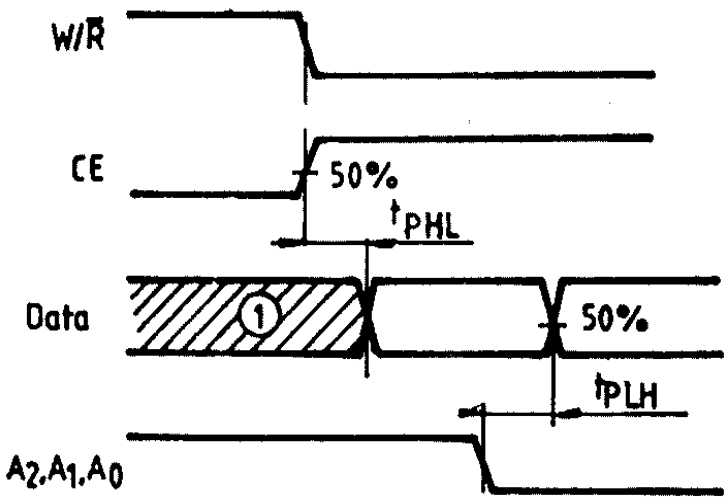
Chip Enable	Write/ Read	Write Disable	Reset	Addressed Latch	Unaddressed Latch	Data Pin
0	X	X	0	*	*	Z
1	1	0	0	Data	*	Input
1	1	1	0	*	*	Z
1	0	X	0	*	*	Q_n
X	X	X	1	0	0	Z/0

X = Don't care
* = No change in state of latch
Z = High impedance
Q_n = State of addressed latch

TIMING DIAGRAM - MMC4599



Data Read



NOTE: 1. Invalid Data Output
2. Reset in LOW State

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS				VALUES							UNIT
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L —Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
		0/10			10		10		0.04	10		300	
		0/15			15		20		0.04	20		600	
		0/20			20		100		0.08	100		3000	
	E, F types	0/ 5			5		20		0.04	20		150	
		0/10			10		40		0.04	40		300	
		0/15			15		80		0.04	80		600	
V_{OH} —Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
		0/10		< 1	10	9.95		9.95			9.95		
		0/15		< 1	15	14.95		14.95			14.95		
V_{OL} —Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
		10/0		< 1	10		0.05			0.05		0.05	
		15/0		< 1	15		0.05			0.05		0.05	
V_{IH} —Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
			1/9	< 1	10	7		7			7		
			1.5/13.5	< 1	15	11		11			11		
V_{IL} —Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
			9/1	< 1	10		3			3		3	
			13.5/1.5	< 1	15		4			4		4	
I_{OH} —Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
		0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
		0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
		0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
	E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
		0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
		0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
		0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL} —Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
		0/10	0.5		10	1.6		1.3	2.6		0.9		
		0/15	1.5		15	4.2		3.4	6.8		2.4		
	E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
		0/10	0.5		10	1.3		1.1	2.6		0.9		
		0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH} I_{IL} —Input leakage current	G, H types	0/18	Any input		18		±0.1		±10 [5]	±0.1		±1	μA
	E, F types	0/15			15		±0.3		±10 [5]	±0.3		±1	
I_{OH} 3-state output	G, H types	0/18	0/18		18		±0.4		±10 [4]	±0.4		±12	μA
	E, F types	0/15	0/15		15		±1.0		±10 [4]	±1.0		±7.5	

STATIC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS				VALUES							UNIT
	V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T_{HIGH}		
					min.	max.	min.	typ	max.	min.	max.	
C_{in} Input Capacitance (Data pin)								15.0	22.5			pF
C_I * Input capacitance		Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C; C_l = 50 pF; R_L = 200 K; all inputs rise and fall times = 20 ns)

	CHARACTERISTICS	V_{DD} Vdc	Min.	Typ.	Max.	Unit
	Output Rise and Fall Time					
t_{TLH}	t_{TLH}, t_{THL} = (1.35ns/pF) C_L +32ns	5.0		100	200	
		10		50	100	ns
	t_{TLH}, t_{THL} = (0.6ns/pF) C_L+20ns	15		40	80	
t_{THL}	t_{TLH}, t_{THL} = (1.4ns/pF) C_L +20ns					
	Propagation Delay Time					
t_{PHL}	Data to Output	5.0		200	400	
t_{PLH}		10		75	150	ns
		15		50	100	
	Write Disable to Output	5.0		200	400	
		10		80	160	ns
		15		80	120	
	Reset to Output	5.0		175	360	
		10		80	160	ns
		15		65	130	
	Address, CE to Output	5.0		225	450	
		10		100	200	ns
		15		75	150	
t_{PHL}	Propagation Delay Time MMC 4599 only	5.0		200	400	
t_{PLH}	Chip Enable, Write/Read to Data	10		80	160	ns
		15		65	130	
	Address to Data	5.0		200	400	
		10		90	180	ns
		15		75	150	

	CHARACTERISTICS	V_{DD} Vdc	Min.	Typ.	Max.	Unit
t_{WH} t_{WL}	Minimum Pulse Widths Data	5.0	200	100		ns
		10	100	50		
		15	80	40		
	Address	5.0	400	200		ns
		10	200	100		
		15	125	65		
	Reset	5.0	150	75		ns
		10	75	40		
		15	50	25		
	Write Disable	5.0	320	160		ns
		10	160	80		
		15	120	60		
t_{su}	Set Up Time Data	5.0	100	50		ns
		10	50	25		
		15	35	20		
t_h	Hold Time Data	5.0	150	75		ns
		10	75	40		
		15	50	25		