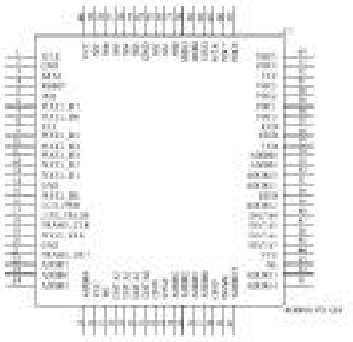
Amulet Technologies

GUI Engines for Embedded Systems

Easy GUI™ Browser Chip

AGB64LV01-QC

- **Dedicated GUI Chip —** Manages the GUI, interacts with the user, and controls the LCD— Frees up your Micro!
- **HTML-Based GUI Creation—** create and edit quickly using drag-and-drop HTML tools
- **Compiler Included—** Converts from HTML, JPEG, and GIF into small, quickly-executable Amulet µHTML™ pages
- **Processor Independent—** Easily interfaces to most microcontrollers (8/16/32-bit and DSPs)
- **Replaces Traditional GUI Library—** No library porting, complex GUI programming, or RTOS required
- **RS232 Interface—** Up-to 115.2 Kbps



Requires:

- 3.3V Power Supply
- Serial Flash (Atmel, 1 Megabit minimum)
- Static RAM (64K-byte minimum)
- Clock/Crystal (up to 20 MHz)

Amulet's Easy GUI Browser Chip is a special purpose microcontroller that is optimized to execute Amulet's GUI kernel and component based GUI firmware. The chip is a combination LCD controller chip and a user interface chip. This chip eliminates the need for complex code to draw each pixel on an LCD. The chip renders GUI pages containing graphic images, Amulet Widgets, and other UI objects directly to the LCD. This lets your embedded micro do its job more efficiently. Thus, the main application can run on a smaller processor with less RAM and ROM, and code development and maintenance time is significantly reduced.

The AGB64LV01-QC is an 80-pin FQFP ASIC with the following built in peripherals:

- LCD Controller
- Microprocessor
- UART
- Timer
- SPI Master

The Easy GUI Browser chip has 13 dedicated output lines for LCD control of various size sub-VGA displays. The chip is able to drive different size displays because the bias voltage, which determines the LCD driving voltage, is supplied from an external source.

- Supply voltage: 3.3V ±10%
- Applicable LCD duty: up to 1/256 (adjustable in single increments)

Pin No.	Name	Pin No.	Name
1	ICLK	2	GND
3	XTAL	4	/RESET
5	/IRQ2	6	PIXEL_D7
7	PIXEL_D6	8	VCC
9	PIXEL_D5	10	PIXEL_D4
11	PIXEL_D3	12	PIXEL_D2
13	PIXEL_D1	14	GND
15	PIXEL_D0	16	LCD_PWR
17	LINE_PULSE	18	FRAME_CLK
19	PIXEL_CLK	20	GND
21	FRAME_OUT	22	ADDR7
23	ADDR6	24	ADDR5
25	ADDR4	26	VCC
27	/WE	28	DATA3
29	DATA2	30	DATA1
31	DATA0	32	GND
33	SYNC	34	ADDR3
35	ADDR2	36	ADDR1
37	ADDR0	38	GND
39	ADDR16	40	ADDR15
41	ADDR14	42	ADDR13
43	/OE	44	VCC
45	DATA7	46	DATA6
47	DATA5	48	DATA4
49	ADDR12	50	GND
51	ADDR11	52	ADDR10
53	ADDR9	54	ADDR8
55	TXD	56	GND
57	RXD	58	/POC0
59	POC1	60	POC2
61	POC3	62	VCC
63	/POC4	64	/IRQ1
65	POC6	66	POC7
67	SCLK	68	GND
69	MOSI	70	MISO
71	/SS0	72	/SS1
73	/SS2	74	GND
75	/SS3	76	/SS4
77	/SS5	78	/SS6
79	/SS7	80	VCC

Pin Description

I = Input O = Output I/O = Input and Output P = Power Supply

Pin Name	Type	Pin Number	Description
DATA7-DATA0	I/O	45-48, 11-13, 31	System Data Bus
ADDR16-ADDR0	O	40-42, 49, 51-54, 22-25, 34-37, 39	System Address Bus
WE	O	27	Memory Write Enable (1=read 0=write)
OE	O	43	Memory Output Enable (0=read 1=write)
SYNC	O	33	N/C
RESET	I	4	System Reset (active low)
ICLK	I	1	System Clock See Diagram for connections
XTAL	O	3	System Clock
IRQ2	I	5	Interrupt Request (active low)
RXD	I	57	UART Receive Data
TXD	O	55	UART Transmit Data
MISO	I	70	SPI Data In
MOSI	O	69	SPI Data Out
SS0	O	71	SPI Flash Select
SS1-SS6	O	72-73, 75-78	Extra Slave Selects
SS7	O	79	System Ram Test Status
POC0	I	58	System Power-Up Mode
POC3	I	61	Flash Programming Rate*
POC6	I	65	System Ram Test
POC4	I	63	Touch Panel Calibration
POC1-POC2	I	59-60	Crystal Selection*
IRQ1	I	64	Touch Panel Interrupt
POC7	I	66	N/C
SCLK	O	67	SPI Clock
PIXEL_D7-PIXEL_D0	O	6-7, 9-13, 15	LCD Pixel Data. This output bus transfers data to be displayed on the LCD. Users can specify the bus width to be either 1, 2, 4, or 8.
PIXEL_CLK	O	19	Pixel Data Shift Clock (CL2). User can specify whether to clock data in on the rising or falling edge of PIXEL_CLK.
LINE_PULSE	O	17	Pixel Data Latch Signal (CL1). This output goes active for one clock period after all the serial data for the current line has been shifted to the LCD. Polarity of this signal can be specified.
FRAME_OUT	O	21	Frame Signal (FLM). LCD first frame synchronization.
FRAME_CLK	O	18	LCD Drive Signal (M). LCD crystal polarization clock.
LCD_PWR	O	16	Display Control Signal. LCD power (“H”=On, “L”=Off).
VCC	P	8, 26, 44, 62, 80	Power Supply Pin
GND	P	2, 14, 20, 32, 38, 50, 56, 68, 74	Grounding Pin

***Frequency Setup Table.**

115200 Baud Rate				**19200 Baud Rate**			
Freq.	**POC Line**			**Freq.**	**POC Line**		
	1	**2**	**3**		**1**	**2**	**3**
10Mhz	1	1	1	10Mhz	0	1	1
12Mhz	0	1	1	12Mhz	0	1	0
16Mhz	1	0	1	16Mhz	1	0	0
20Mhz	0	0	1	20Mhz	0	0	0

DC Characteristics

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage	VCC	-0.3 to +6.5	V
Input Voltage 3.3V	Vin	3.0 to 3.6	V
Operating Temp.	Topr	-20 to +75	°C
Storage Temp.	Tstg	-60 to +150	°C
Soldering Lead Temp. soldering 10 Sec.	Tsol	210	°C

DC Characteristics for 3.3V

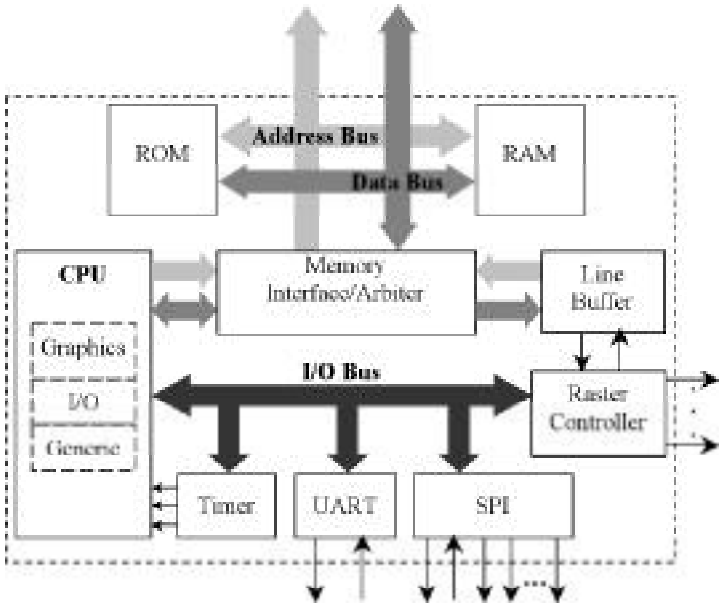
Item	Symbol	Min	Typ	Max	Unit
TTL INPUT					
Input “High” Voltage	Vih	2			V
Input “Low” Voltage	Vil			0.8	V
Input Leakage current	IL	-10		10	µA
CMOS INPUT					
Input “High” Voltage	Vih	.7 x VCC			V
Input “Low” Voltage	Vil			0.3VCC	V
Input Leakage current	IL	-10		10	µA
TTL OUTPUT					
Output “High” Voltage	Voh	2.45			V
Output “Low” Voltage	Vol			0.45	V
CMOS OUTPUT					
Output “High” Voltage	Voh	.7 x VCC			V
Output “Low” Voltage	Vol			0.3VCC	V
Operating Frequency	F_CLK	10	16	20	MHz
Pull-up Resistor (Reset, RxD, POC7, IRQ, MISO, ICLK)		70K	108K	202K	Ohms

Current

VCC = + 3.3V +/-10%, GND = 0, TEMP= -20 TO +75C

Item	Symbol	Condition	Min	Typ	Max	Unit
Operating Current	Icc	10MHz		10		mA
Operating Current	Icc	10MHz Reset		7		mA
Operating Current	Icc	16MHz		16		mA
Operating Current	Icc	16MHz Reset		10		mA

Detailed Description



Although there is only a single Von-Neuman CPU, the CPU features task specific opcodes, registers and memory segments for three very different types of tasks: graphics rendering, I/O processing and general purpose computing. This architecture enables the GUI kernel firmware to implement a highly efficient task scheduler. In addition, graphics and I/O tasks are implemented with a minimum of CPU cycles and code space.

The Line Buffer is a parallel loaded shift register with a maximum capacity of 256 bytes. It is responsible for periodically burst fetching a block of pixel data for each raster line from the frame buffer. To minimize the burst period, the Line Buffer was implemented as a dual ported synchronous SRAM block capable of reading a single byte in a single CPU clock cycle.

To minimize external pin and component count, only a single external memory bus is implemented. Because both the CPU and Line Buffer require access to external memory, a memory interface unit is employed to resolve arbitration and to direct flow of data and address signals.

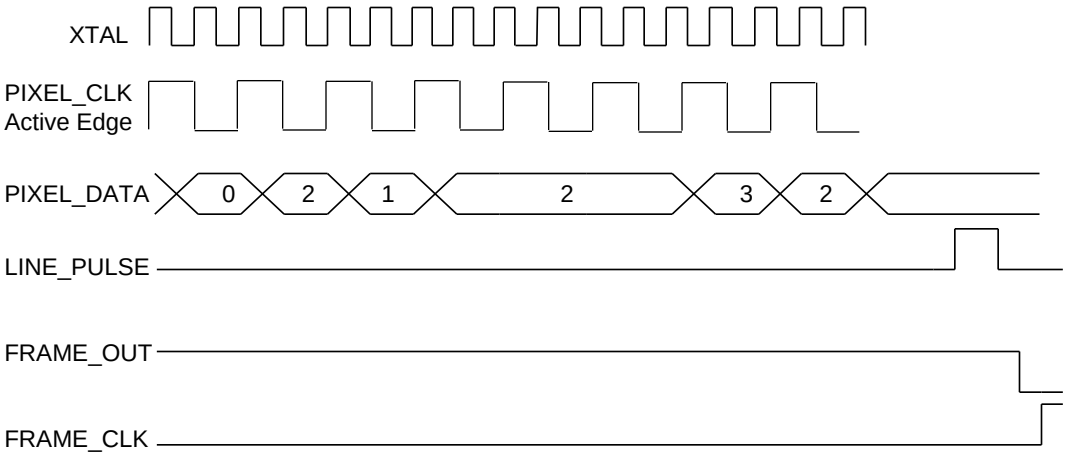
The CPU also features a separate I/O bus linking the following on-chip peripherals to the CPU's I/O task: an LCD Raster Controller, Three Timers, a UART, and an SPI master with 8 slave selects.

The LCD Raster Controller is a unique peripheral. It is responsible for converting the Line Buffer data to signals conforming to standard LCD interfaces. These include horizontal and vertical synchs as well as a serially shifted data stream of pixel data and a shift clock.

LCD Interface Timing Diagrams

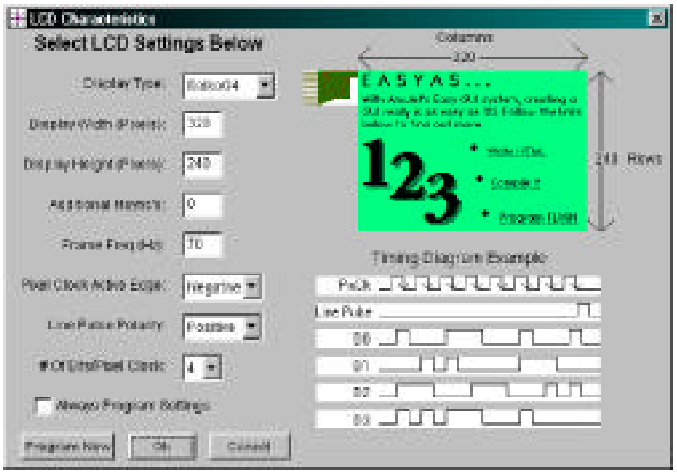
The following timing diagrams assume:

DATA WIDTH = 8-bits Max. (Adjustable in Software)
LINE_PULSE = Positive or Negative - Edge Line Pulse (Adjustable in Software)
PIXEL_CLK = Positive or Negative - Edge Pixel Clock (Adjustable in Software)
MAXBYTE = 4 bytes of data per line and with the following data in the line buffer: 20, 21, 22, 23 …



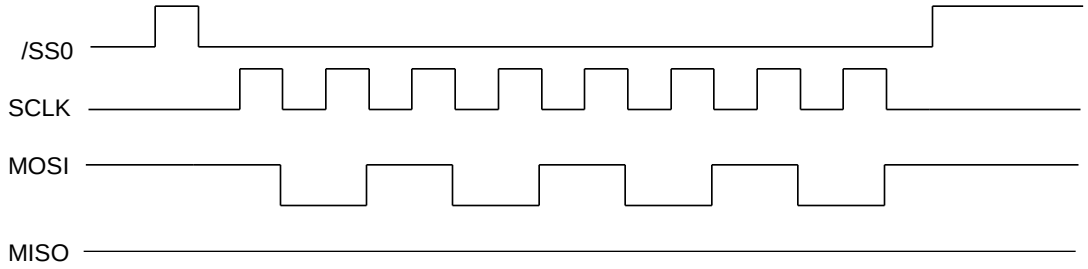
Interface Information, by Manufacturer/Model

Signal	Seiko G4 /G8	Optrex DMF50081	Denistron PM0149	NanYa LMBGAX032X	Hantronix DM3224-1	Pixtech FE524M1
PIXEL_CLK	CL2	CP	CL2(SCP)	CP2	CP	DCLK
PIXEL_D0	D3	D3	D0	D3	D3	D4
PIXEL_D1	D2	D2	D1	D2	D2	D3
PIXEL_D2	D1	D1	D2	D1	D1	D2
PIXEL_D3	D0	D0	D3	D0	D0	D1
LINE_PULSE	CL1	LP	CL1(LP)	CP1	LOAD	HSYNC
FRAME_OUT	FLM	FLM	FLM	S	FRAME	YSYNC
FRAME_CLK	M	M	M			
LCD_PWR	DISP OFF	DISP OFF	BLE		DISPOFF	DON



LCD characteristic settings within the compiler let you specify different displays either by manufacturer or by size (up to 1/4 VGA resolution), frame frequency, and pixel clock.

SPI Interface Timing Diagram



SPI Interface

- Serial Interface Architecture
- Minimum 1M-Bit (264 bytes/page * 512 pages)
- One 264-byte SRAM data buffer
- TTL I/O

Description

Amulet's Easy GUI Browser Chip supports an Atmel flash memory device (Part # AT45DB011B-SC) for data storage of µHTML pages. The flash memory device must be organized with a minimum of 512 pages of 264 bytes each, plus one SRAM data buffer of 264 bytes. The flash is enabled through a chip select pin (/CS) and accessed via a three-wire serial interface consisting of a serial input (SI), serial output (SO), and a serial clock (SCK).

Device Operation

The flash device is controlled by instructions from the Amulet Easy GUI Browser Chip. The list of instructions which Amulet uses to interface to the flash are as follows:

Main Memory Page Read (52H)

Main Memory Page to Buffer Transfer (53H),

Buffer Write (84H)

Buffer to Main Memory Page Program (83H)

Status Register (57H).

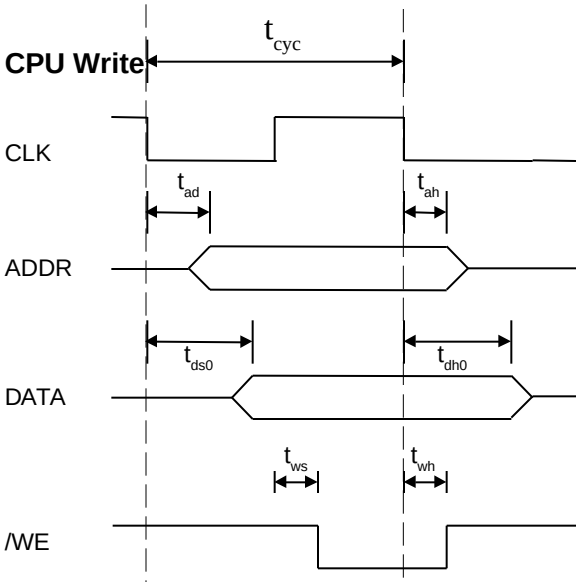
If you decide to use a flash device other than the recommended Atmel part, the device must support the five instructions above. Please check the Atmel datasheet for more information on the Atmel flash device.

There are two subsystems that access memory: The CPU and the Display Line Buffer. The timing for each subsystem is detailed below.

CPU Memory Access Timing

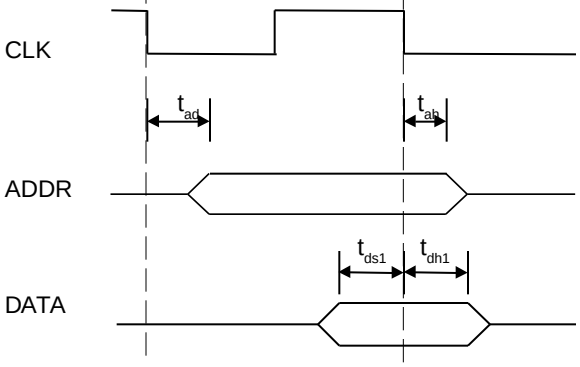
The CPU performs both Read and Write accesses to memory. In either case, all timing parameters for CPU accesses are relative to the falling edge of CLK. All input signals are sampled at the falling edge of CLK and all output signals transition after some delay relative to the falling edge of CLK. Input Hold times are the amount of time after the falling edge of CLK that a signal must remain stable. Output Hold times are the minimum delay that the signal will remain stable after the falling edge of CLK.

CPU Write



Label	Description	Value	Units
t_{ad}	Address Delay	10	nS
t_{ah}	Address Hold	5	nS
t_{ds0}	Write Data Delay	10	nS
t_{dh0}	Write Data Hold	5	nS
t_{ws}	Write Enable Delay	8	nS
t_{wh}	Write Enable Hold	3	nS

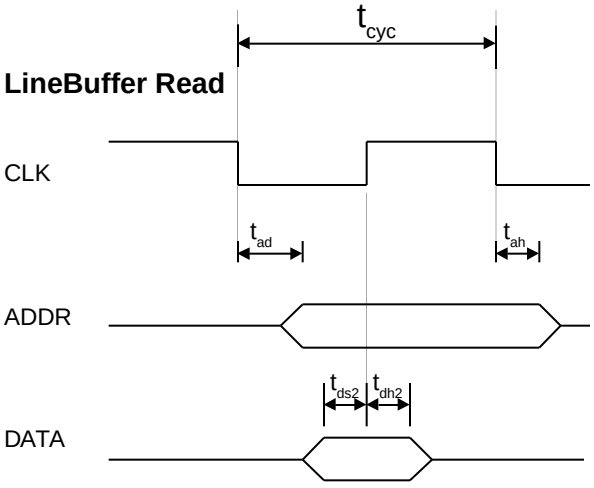
CPU Read



Label	Description	Value	Units
t_{ad}	Address Delay	10	nS
t_{ah}	Address Hold	5	nS
t_{ds1}	Read Data Setup	5	nS
t_{dh1}	Read Data Hold	0	nS

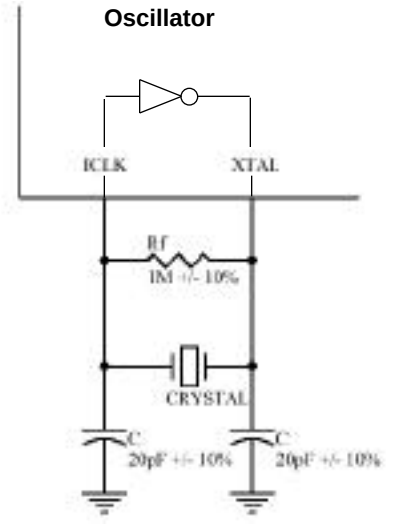
Line Buffer Memory Access Timing

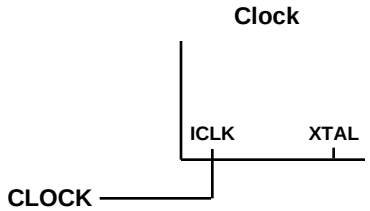
The Line buffer only performs Read accesses to memory. Timing parameters for Line buffer reads are relative to both edges of CLK. All input signals are sampled at the rising edge of CLK and all output signals transition after some delay relative to the falling edge of CLK. Input Hold times are the amount of time after the rising of CLK that a signal must remain stable. Output Hold times are the minimum delay that the signal will remain stable after the falling edge of CLK.



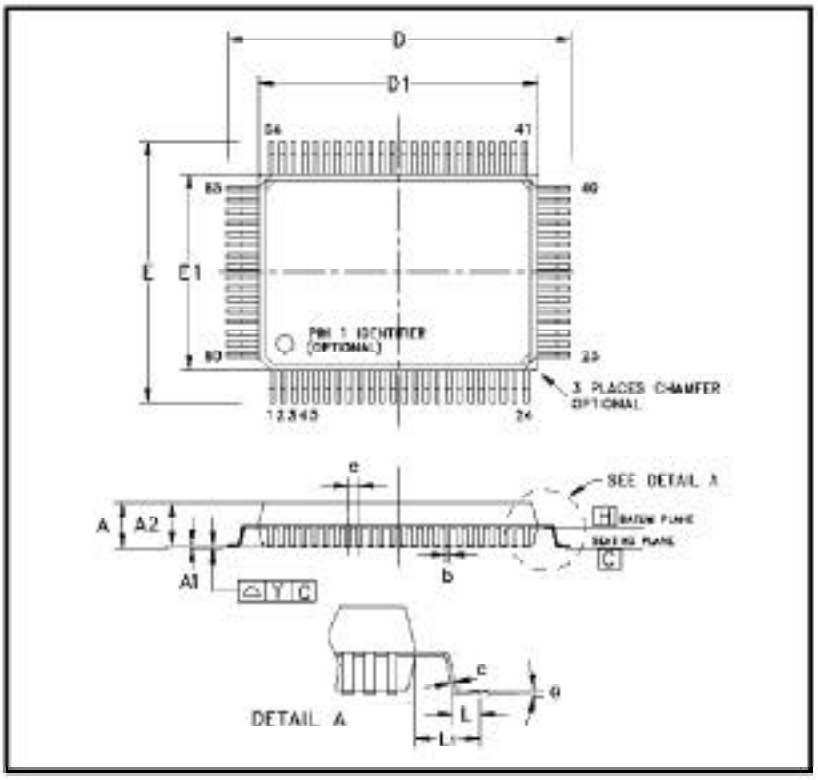
Label	Description	Value	Units
t_{ad}	Address Delay	10	nS
t_{ah}	Address Hold	5	nS
t_{ds2}	Read Data Setup	5	nS
t_{dh2}	Read Data Hold	5	nS

Clock Options



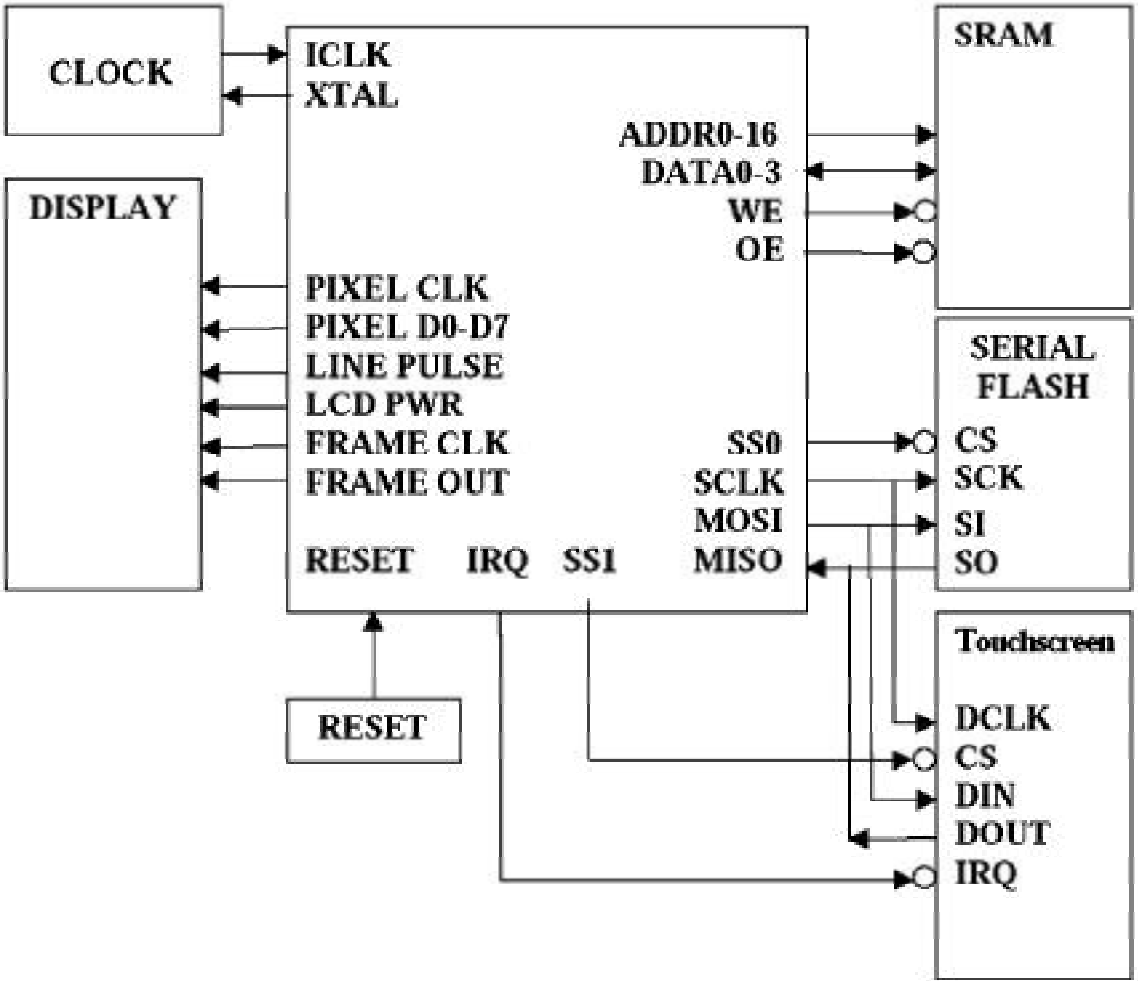


Chip Mechanicals 80 PQFP (14x20x2.7mm), 3.2mm FP



Symbol	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A			3.40			0.134
A1	0.25			0.010		
A2	2.55	2.70	2.87	0.100	0.106	0.113
b	0.30		0.45	0.012		0.018
c	0.13		0.23	0.005		0.009
D	22.95	23.20	23.45	0.904	0.913	0.923
E	16.95	17.20	17.45	0.667	0.677	0.687
e		0.80	BSC		0.031	
D1	19.90	20.00	20.10	0.783	0.787	0.791
E1	13.90	14.00	14.10	0.547	0.551	0.555
L	0.73	0.88	1.03	0.029	0.035	0.041
L1		1.60	REF		0.063	
Y		0.10			0.004	
θ	0°		7°	0°		7°

Sample Application



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www.AmuletTechnologies.com

Amulet Technologies, LLC
275 Saratoga Avenue, Suite 230
Santa Clara, CA 95050
(408) 244-0363