

## AUTOMOTIVE GLOW PLUG DRIVER

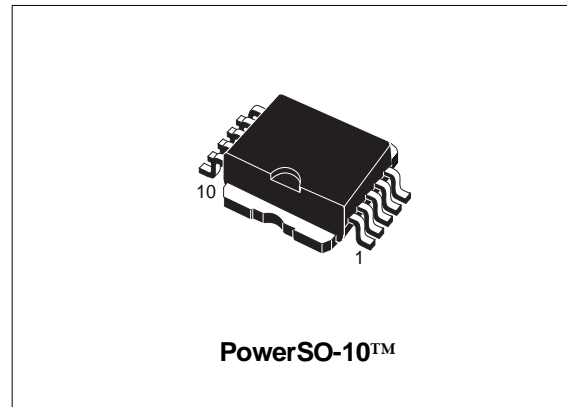
PRELIMINARY DATA

TYPE	$R_{DS(on)}$	$I_{OUT}$	$V_{CC}$
VN710SP	18m $\Omega$	35 A	16 V

- CMOS COMPATIBLE INPUT
- ON STATE OPEN LOAD DETECTION
- OFF STATE OPENLOAD DETECTION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- PROTECTION AGAINST LOSS OF GROUND
- VERY LOW STAND-BY CURRENT WHEN ENABLE PIN IS LOW
- REVERSE BATTERY PROTECTION (\*)

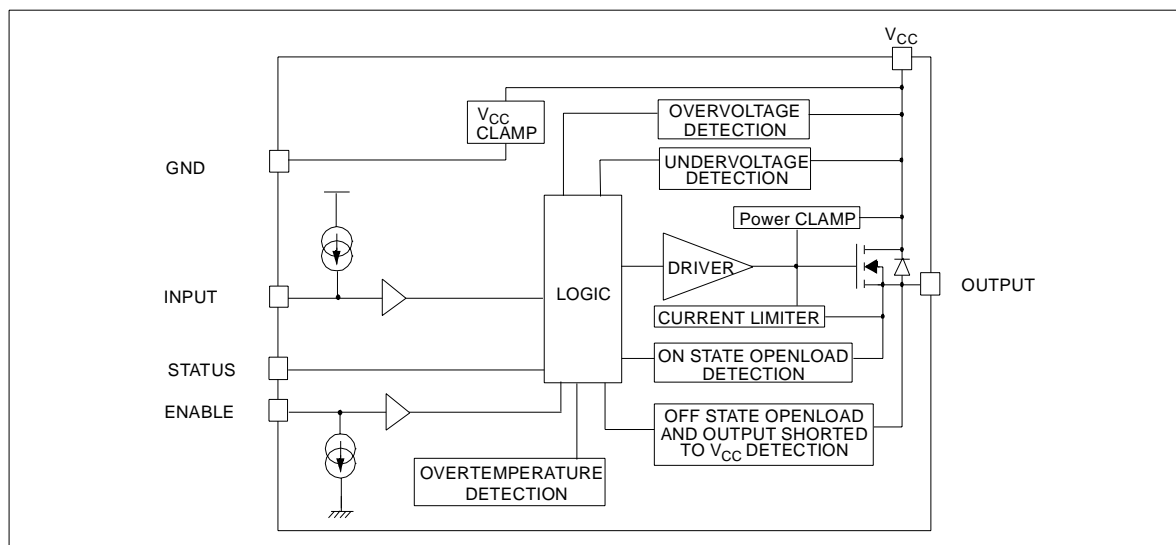
### DESCRIPTION

The VN710SP is a monolithic device made using STMicroelectronics VIPower M0-3 technology, intended for driving any kind of load with one side connected to ground. Active  $V_{CC}$  pin voltage clamp protects the device against low energy spikes (see ISO7637 transients compatibility table). Active current limitation combined with thermal shutdown protect the device against



overload. After a thermal shutdown event, device stays latched off and diagnostic stays at a low level until next falling edge of input signal. The device detects open load condition both in on state and off state. Output shorted to  $V_{CC}$  is detected in the off state. Device automatically turns off in case of ground pin disconnection. Enable pin allows to switch the device to idle state with very low quiescent current from  $V_{CC}$ . When enable is low, device turns off regardless of input pin state.

### BLOCK DIAGRAM



(\*) See application schematic at page 7

# VN710SP

## THERMAL DATA

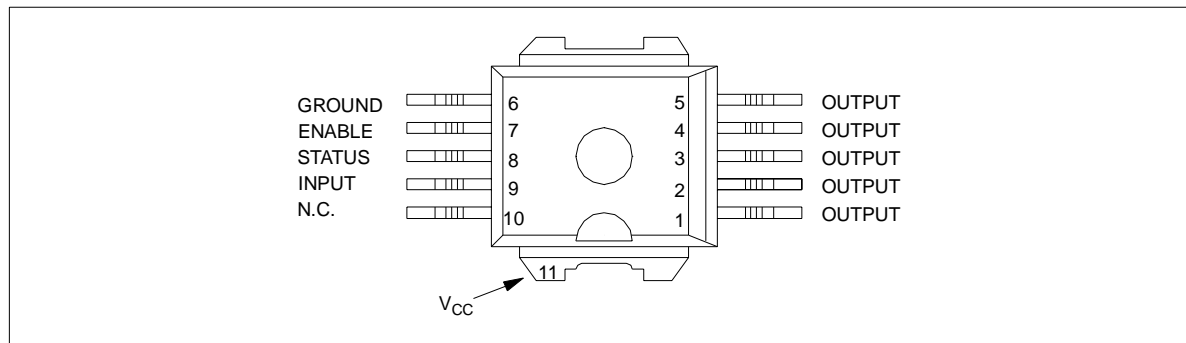
Symbol	Parameter	Value	Unit
$R_{\text{tj-case}}$	Thermal resistance junction-case	1.4	$^{\circ}\text{C/W}$
$R_{\text{tj-amb}} (*)$	Thermal resistance junction-ambient	52	$^{\circ}\text{C/W}$

(\*) When mounted on a standard single-sided FR-4 board with  $50\text{mm}^2$  of Cu (at least  $35\mu\text{m}$  thick).

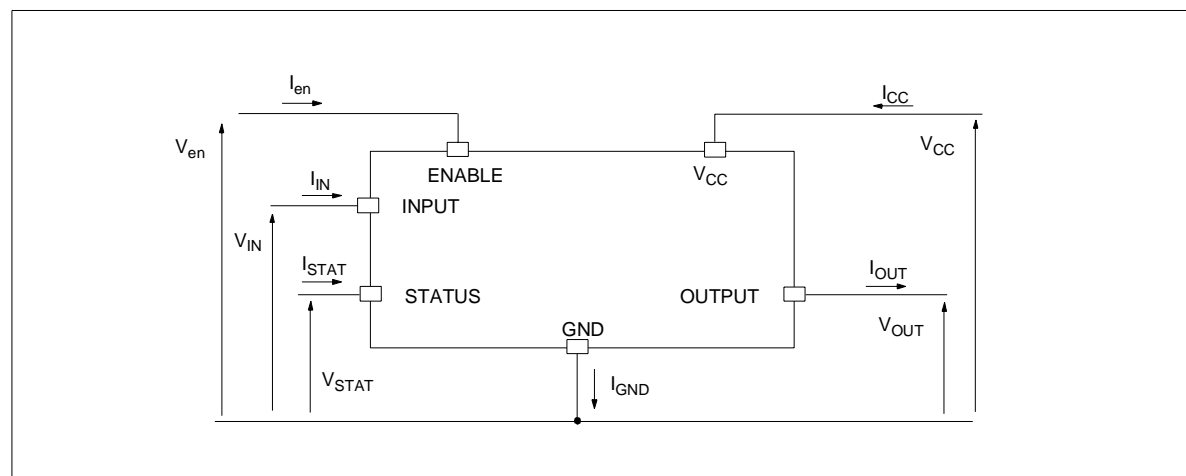
## ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
$V_{\text{CC}}$	DC supply voltage	41	V
$-V_{\text{CC}}$	Reverse DC supply voltage	-0.3	V
$-I_{\text{GND}}$	Reverse DC ground pin current	-200	mA
$I_{\text{OUT}}$	DC output current	Internally limited	A
$-I_{\text{OUT}}$	Reverse DC output current	-35	A
$I_{\text{IN}}$	DC input current	+/-10	mA
$I_{\text{en}}$	DC enable current	+/-10	mA
$I_{\text{STAT}}$	DC status current	+/-10	mA
$V_{\text{ESD}}$	Electrostatic discharge ( $R=1.5\text{k}\Omega$ ; $C=100\text{pF}$ )	2000	V
$P_{\text{tot}}$	Power dissipation at $T_{\text{c}}=25^{\circ}\text{C}$	89	W
$T_{\text{j}}$	Junction operating temperature	Internally limited	$^{\circ}\text{C}$
$T_{\text{c}}$	Case operating temperature	-40 to 150	$^{\circ}\text{C}$
$T_{\text{stg}}$	Storage temperature	-55 to 150	$^{\circ}\text{C}$

## CONNECTION DIAGRAM (TOP VIEW)



## CURRENT AND VOLTAGE CONVENTIONS



**ELECTRICAL CHARACTERISTICS** ( $7V < V_{CC} < 16V$ ;  $-40^{\circ}C < T_j < 150^{\circ}C$ ; unless otherwise specified)**POWER**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{CC}$	Operating supply voltage		5.5	13	16	V
$V_{USD}$	Undervoltage shutdown		3	4	5.5	V
$V_{OV}$	Overvoltage shutdown		16	18	20	V
$R_{ON}$	On state resistance	$I_{OUT}=15A$ ; $T_j=25^{\circ}C$			20	m $\Omega$
		$I_{OUT}=15A$			40	m $\Omega$
$I_S$	Supply current	Off state; $V_{CC}=13V$ ; $V_{en}=V_{OUT}=0V$ ; $V_{IN}=5V$		10	25	$\mu A$
		Off state; $V_{CC}=13V$ ; $V_{en}=V_{OUT}=0V$ ; $V_{IN}=5V$ ; $T_j=25^{\circ}C$		10	20	$\mu A$
		On state; $V_{CC}=13V$ ; $V_{IN}=0V$ ; $I_{OUT}=0A$ ; $V_{en}>V_{enh}$		2.5	4	mA
$I_{LGND}$	Output current at Turn-off	$V_{CC}=V_{GND}=16V$ $V_{IN}=V_{en}=n.c.$ ; $V_{OUT}=0V$			2	mA
$I_{L(off1)}$	Off state output current	$V_{OUT}=0V$ ; $V_{IN}>V_{IH}$	0		50	$\mu A$
$I_{L(off2)}$	Off state output current	$V_{OUT}=3.5V$ ; $V_{IN}>V_{IH}$ ; $V_{en}>V_{enh}$	-75		0	$\mu A$

**SWITCHING** ( $V_{CC}=13V$ )

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	$R_L=0.85\Omega$ , from $V_{IN}$ falling edge to $V_{OUT}=1.3V$		40		$\mu s$
$t_{d(off)}$	Turn-off delay time	$R_L=0.85\Omega$ , from $V_{IN}$ rising edge to $V_{OUT}=11.7V$		80		$\mu s$
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L=0.85\Omega$ , from $V_{OUT}=1.3V$ to $V_{OUT}=10.4V$		0.1		V/ $\mu s$
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L=0.85\Omega$ , from $V_{OUT}=11.7V$ to $V_{OUT}=1.3V$		0.1		V/ $\mu s$

**INPUT PIN** (active low)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{IL}$	Input low level				1.25	V
$I_{IL}$	Low level input current	$V_{IN}=1.25V$ ; $V_{en}>V_{enh}$	-35			$\mu A$
$V_{IH}$	Input high level		3.25			V
$I_{IH}$	High level input current	$V_{IN}=3.25V$ ; $V_{en}>V_{enh}$			-4	$\mu A$
		$V_{IN}=3.25V$ ; $V_{en}=0V$	-300		-4	$\mu A$
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
$V_{ICL}$	Input clamp voltage	$I_{IN}=1mA$	6	6.8	8	V
		$I_{IN}=-1mA$		-0.7		V

**ENABLE PIN** (active high)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{enl}$	Enable low level				1.25	V
$I_{enl}$	Low level enable current	$V_{en}=1.25V$	4			$\mu A$
$V_{enh}$	Enable high level		3.25			V
$I_{enh}$	High level enable current	$V_{en}=3.25V$			35	$\mu A$
$V_{ehyst}$	Enable hysteresis voltage		0.5			V
$V_{encl}$	Enable clamp voltage	$I_{en}=1mA$	6	6.8	8	V
		$I_{en}=-1mA$		-0.7		V

**ELECTRICAL CHARACTERISTICS** (continued)  
 STATUS PIN (Open Drain)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{STAT}$	Status low output voltage	$I_{STAT}=1.6mA$			0.5	V
$I_{LSTAT}$	Status leakage current	Normal operation; $V_{STAT}=5V$			10	$\mu A$
$C_{STAT}$	Status pin input capacitance	Normal operation; $V_{STAT}=5V$			100	pF
$V_{SCL}$	Status clamp voltage	$I_{STAT}=1mA$	6	6.8	8	V
		$I_{STAT}=-1mA$		-0.7		V

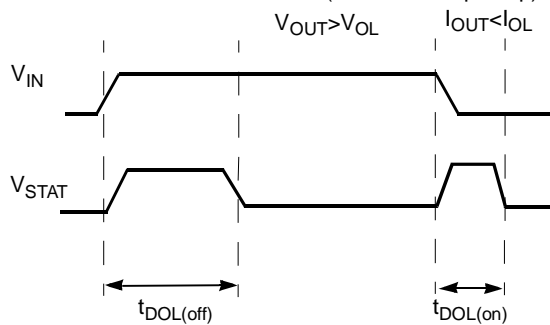
**PROTECTIONS**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$T_{TSD}$	Shut-down temperature		170	190		$^{\circ}C$
$T_R$	Reset temperature		135			$^{\circ}C$
$T_{hyst}$	Thermal hysteresis		7	15		$^{\circ}C$
$t_{SDL}$	Overload detection delay	$T_j > T_{TSD}$			20	$\mu s$
$I_{lim}$	Current limitation		35	55	80	A
$V_{demag}$	Turn-off output clamp voltage	$I_{OUT}=2A$ ; $V_{IN}=5V$ ; $L=6mH$	$V_{CC}-41$	$V_{CC}-48$	$V_{CC}-55$	V

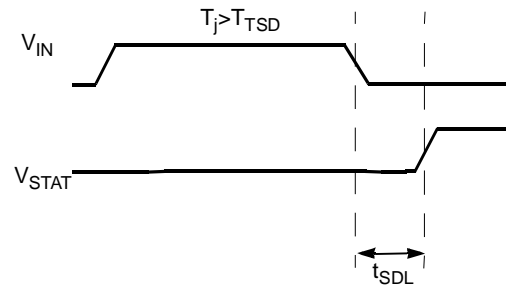
**OPENLOAD DETECTION**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$I_{OL}$	Openload on state detection threshold	$V_{IN}=0V$	0.1	1	2	A
$V_{OL}$	Openload off state voltage detection threshold	$V_{IN}=5V$	1.5	2.5	3.5	V
$t_{DOL(off)}$	Openload detection delay at turn-off				500	$\mu s$
$t_{DOL(on)}$	Openload detection delay at turn-on	$I_{OUT}=0V$			200	$\mu s$

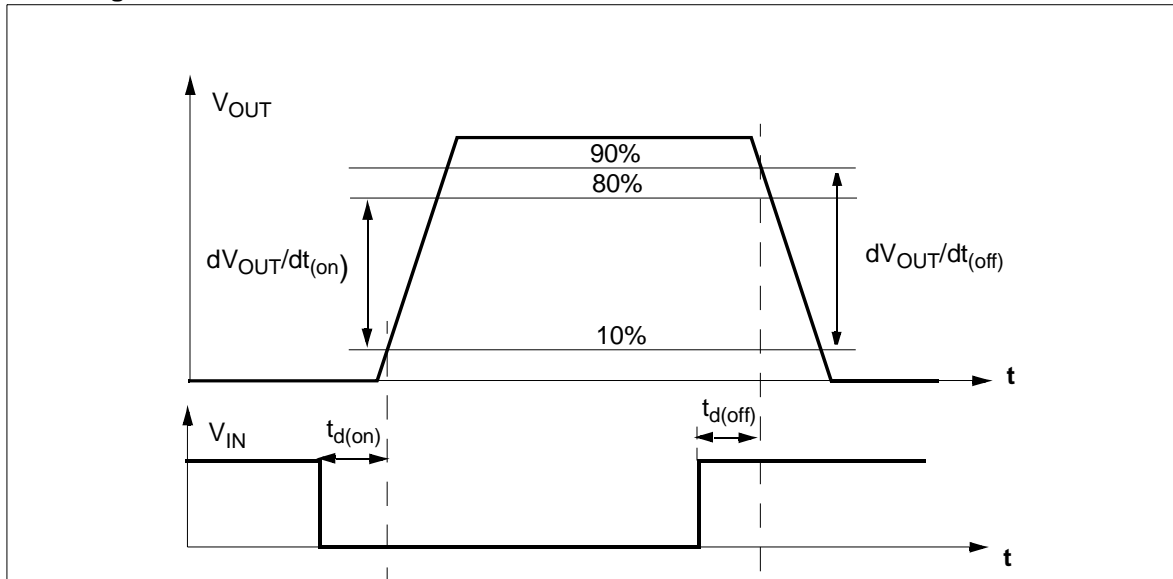
OPENLOAD STATUS TIMING (with external pull-up)



OVERTEMP STATUS TIMING



## Switching Time Waveforms



## TRUTH TABLE

CONDITIONS	ENABLE	INPUT	OUTPUT	STATUS
Normal operation	H	H	L	H
	H	L	H	H
Current limitation	H	H	L	H
	H	L	X	H
Overtemperature	H	L	L (*)	L (*)
	H	H	L	L
Undervoltage	H	H	L	X
	H	L	L	X
Overvoltage	H	H	L	H
	H	L	L	H
Output voltage > $V_{OL}$	H	H	H	L
	H	L	H	H
Output current < $I_{OL}$	H	H	L	H
	H	L	H	L
Any	L	X	L	H

(\*) Latched on first overtemperature event; latch cleared on next input falling edge.

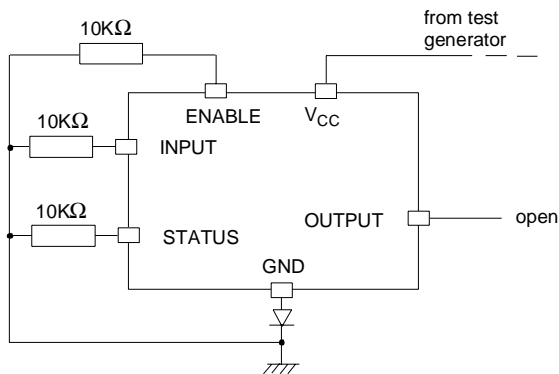
**ELECTRICAL TRANSIENTS REQUIREMENTS ON V<sub>CC</sub> PIN**

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25V	-50V	-75V	-100V	2ms, 10Ω
2	+25V	+50V	+75V	+100V	0.2ms, 10Ω
3a	-25V	-50V	-100V	-150V	0.1ms, 50Ω
3b	+25V	+50V	+75V	+100V	0.1ms, 50Ω
4	-4V	-5V	-6V	-7V	100ms, 0.01Ω
5	+26.5V	+46.5V	+66.5V	+86.5V	400ms, 2Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULT			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

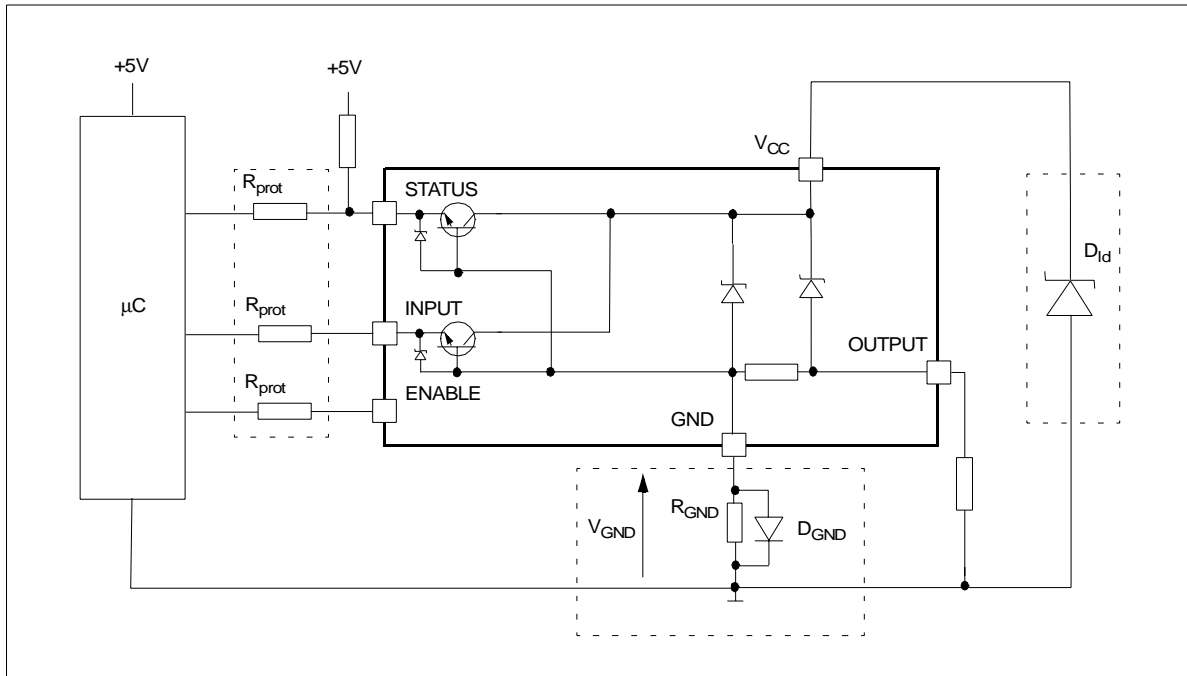
CLASS	CONTENTS
<b>C</b>	All functions of the device are performed as designed after exposure to disturbance.
<b>E</b>	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

**SUGGESTED SCHEME FOR ISO TEST PULSE**



Warning: Input, Enable, Status Pulled to V<sub>CC</sub> voltage during negative transient.

## APPLICATION SCHEMATIC



## GND PROTECTION NETWORK AGAINST REVERSE BATTERY

**Solution 1:** Resistor in the ground line ( $R_{GND}$  only). This can be used with any type of load.

The following is an indication on how to dimension the  $R_{GND}$  resistor.

- 1)  $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$ .
- 2)  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the of the device's datasheet.

Power Dissipation in  $R_{GND}$  (when  $V_{CC} < 0$ : during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the  $R_{GND}$  will produce a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift will vary depending on many devices are ON in the case of several high side drivers sharing the same  $R_{GND}$ .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggest to utilize Solution 2 (see below).

**Solution 2:** A diode ( $D_{GND}$ ) in the ground line.

A resistor ( $R_{GND} = 1\text{k}\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ( $\approx 600\text{mV}$ ) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

## LOAD DUMP PROTECTION

$D_{Id}$  is necessary (Transil or MOV) if the load dump peak voltage exceeds  $V_{CC}$  max DC rating. The same applies if the device will be subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO T/R 7637/1 table.

 $\mu\text{C}$  I/Os PROTECTION:

If a ground protection network is used and negative transient are present on the  $V_{CC}$  line, the control pins will be pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the  $\mu\text{C}$  I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of  $\mu\text{C}$  and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of  $\mu\text{C}$  I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

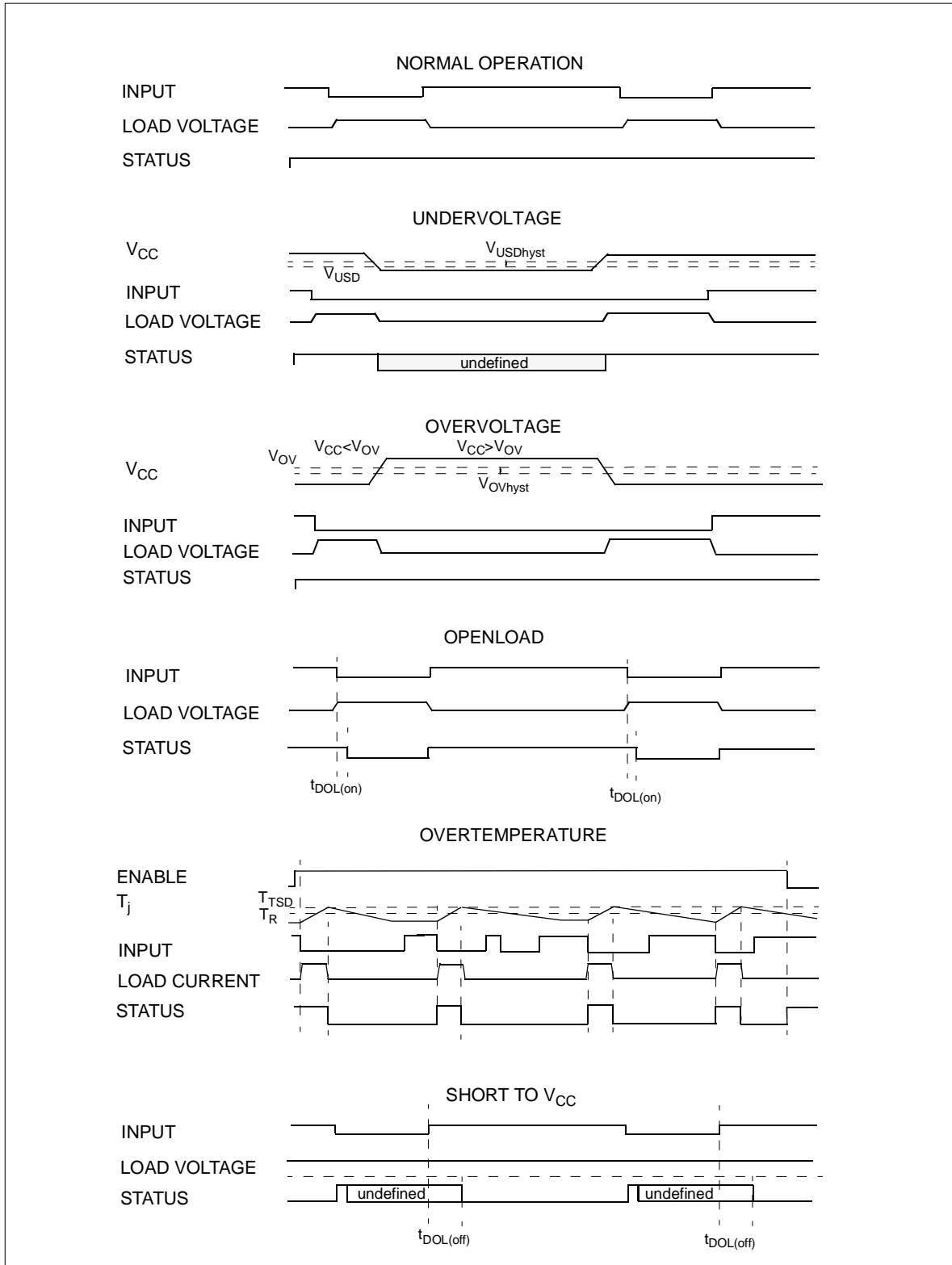
Calculation example:

$$\text{For } V_{CCpeak} = -100\text{V and } I_{latchup} \geq 20\text{mA; } V_{OH\mu C} \geq 4.5\text{V}$$

$$5\text{k}\Omega \leq R_{prot} \leq 18.57\text{k}\Omega.$$

Recommended  $R_{prot}$  value is  $10\text{k}\Omega$ .

Figure1: Waveforms

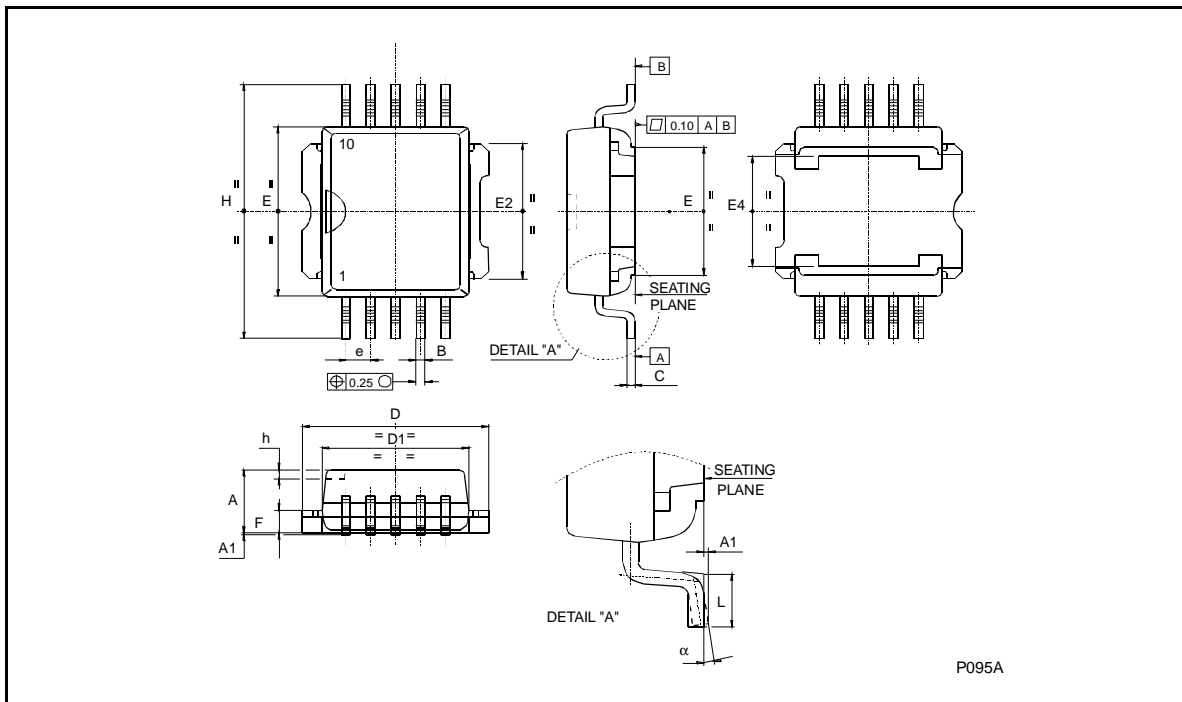




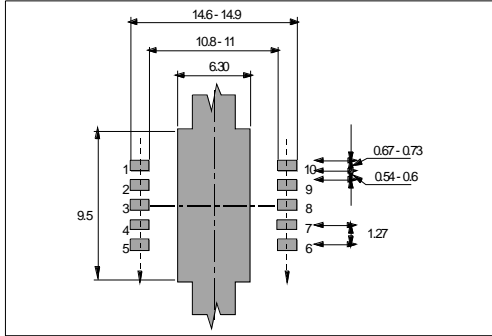
**PowerSO-10™ MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A (*)	3.4		3.6	0.134		0.142
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
B (*)	0.37		0.53	0.014		0.021
C	0.35		0.55	0.013		0.022
C (*)	0.23		0.32	0.009		0.0126
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E2	7.20		7.60	0.283		300
E2 (*)	7.30		7.50	0.287		0.295
E4	5.90		6.10	0.232		0.240
E4 (*)	5.90		6.30	0.232		0.248
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
F (*)	1.20		1.40	0.047		0.055
H	13.80		14.40	0.543		0.567
H (*)	13.85		14.35	0.545		0.565
h		0.50			0.002	
L	1.20		1.80	0.047		0.070
L (*)	0.80		1.10	0.031		0.043
α	0°		8°	0°		8°
α (*)	2°		8°	2°		8°

(\*) Muar only POA P013P



**PowerSO-10™ SUGGESTED PAD LAYOUT**



**TUBE SHIPMENT (no suffix)**

	Base Q.ty	Bulk Q.ty	Tube length (±0.5)	A	B	C (±0.1)
<b>Casablanca</b>	50	1000	532	10.4	16.4	0.8
<b>Muar</b>	50	1000	532	4.9	17.2	0.8

All dimensions are in mm.

**TAPE AND REEL SHIPMENT (suffix "13TR")**

REEL DIMENSIONS	Value
Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (±0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	60
T (max)	30.4

All dimensions are in mm.

**TAPE DIMENSIONS**  
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Parameter	Symbol	Value
Tape width	W	24
Tape Hole Spacing	P0 (±0.1)	4
Component Spacing	P	24
Hole Diameter	D (±0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (±0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (±0.1)	2

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