PI6CUA878

PLL Clock Driver for 1.8V DDR2 Memory

Features

- PLL clock distribution for DDR2 DIMM applications.
- Distributes one differential clock input pair to eleven differential clock output pairs.
- Differential Inputs (CLK, $\overline{\text{CLK}}$) and (FBIN, $\overline{\text{FBIN}}$)
- Input OE/OS: LVCMOS
- Differential Outputs (Y[0:9], $\overline{\text{Y[0:9]}}$ and (FBOUT, $\overline{\text{FBOUT}}$)
- External feedback pins (FBIN, $\overline{\text{FBIN}}$) are used to synchronize the outputs to the clock input.
- Operates at AV_{DD} = 1.8V for core circuit and internal PLL, and V_{DDQ} = 1.8V for differential output drivers
- Available Packages (Pb-free & Green):
  – 52-ball VFBGA (NF)

- PI6CUA878 is for DDR2-800/667/533/400 applications

Pin Configuration

	1	2	3	4	5	6
A	Y1	Y0	$\overline{\text{Y0}}$	$\overline{\text{Y5}}$	Y5	Y6
B	$\overline{\text{Y1}}$	GND	GND	GND	GND	$\overline{\text{Y6}}$
C	$\overline{\text{Y2}}$	GND	NB	NB	GND	$\overline{\text{Y7}}$
D	Y2	VDDQ	VDDQ	VDDQ	OS	Y7
E	CK	VDDQ	NB	NB	VDDQ	FBIN
F	$\overline{\text{CK}}$	VDDQ	NB	NB	OE	$\overline{\text{FBIN}}$
G	AGND	VDDQ	VDDQ	VDDQ	VDDQ	$\overline{\text{FBOUT}}$
H	AVDD	GND	NB	NB	GND	FBOUT
J	Y3	GND	GND	GND	GND	Y8
k	$\overline{\text{Y3}}$	$\overline{\text{Y4}}$	Y4	Y9	$\overline{\text{Y9}}$	$\overline{\text{Y8}}$

Description

PI6CUA878 PLL clock driver is developed for Registered DDR2 DIMM applications with 1.8V operation and differential data input and output levels.

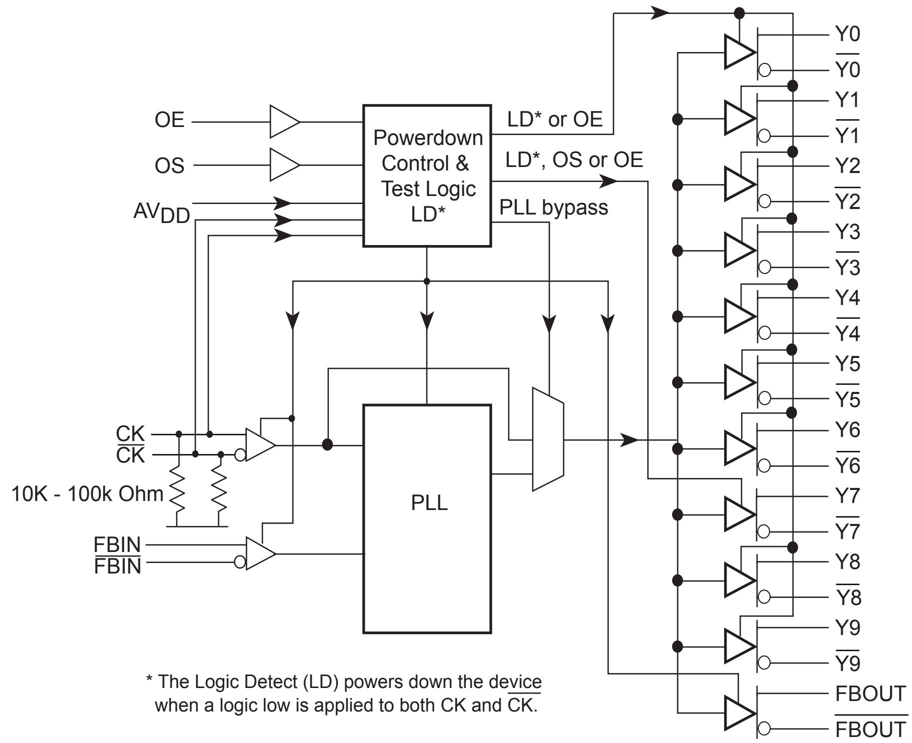
The device is a zero delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to eleven differential pairs of clock outputs which includes feedback clock (Y[0:9], $\overline{\text{Y[0:9]}}$; FBOUT, $\overline{\text{FBOUT}}$).

The clock outputs are controlled by CLK/$\overline{\text{CLK}}$, FBOUT, $\overline{\text{FBOUT}}$, the LVCMOS inputs (OE, OS) and the Analog Power input (AV_{DD}). When OE is LOW, all the outputs except for FBOUT, $\overline{\text{FBOUT}}$, are disabled while the internal PLL continues to maintain its locked-in frequency. OS is a program pin that must be tied to GND or V_{DD}. When OS is high, OE will function as described above. When OS is low, OE has no effect on Y7/$\overline{\text{Y7}}$, they are free running. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

When CLK/$\overline{\text{CLK}}$ are logic LOW, the device will enter a low power mode. An input logic detection circuit will detect the logic low level and perform a low power state where all Y[0:9], $\overline{\text{Y[0:9]}}$; FBOUT, $\overline{\text{FBOUT}}$, and PLL are OFF.

The PI6CUA878 is a high performance, low skew, and low jitter PLL clock driver, and is also able to track Spread Spectrum Clocking (SSC) for reduced EMI.

Block Diagram



Pinout Table

Pin Name	Characteristics	Description
AGND	Ground	Analog ground
AV_{DD}	1.8V nominal	Analog power
CK	Differential Input	Clock input with a (10k - 100kΩ) pulldown resistor
$\overline{CK}$	Differential Input	Complementary clock input with a (10k - 100kΩ) pulldown resistor
$\overline{FBIN}$	Differential Input	Complementary feedback clock input
FBIN	Differential Input	Feedback clock input
$\overline{FBOUT}$	Differential Output	Complementary Feedback clock output
FBOUT	Differential Output	Feedback clock output
OE	LVCMOS input	Output enable (async.)
OS	LVCMOS input	Output select (tied to GND or V_{DDQ})
GND	Ground	Ground
V_{DDQ}	1.8V nominal	Logic and Output power
Y[0:9]	Differential Outputs	Clock outputs
$\overline{Y[0:9]}$	Differential Outputs	Complementary clock outputs
NB		No Ball

Function Table

Inputs					Outputs				PLL State
AV_{DD}	OE	OS	CK	$\overline{CK}$	Y	Y	FBOUT	$\overline{FBOUT}$	
GND	H	X	L	H	L	H	L	H	Bypass/Off
GND	H	X	H	L	H	L	H	L	Bypass/Off
GND	L	H	L	H	L(Z)(1)	L(Z)(1)	L	H	Bypass/Off
GND	L	L	H	L	L(Z)(1), Y7 active	L(Z)(1), Y7 active	H	L	Bypass/Off
1.8V (nom)	L	H	L	H	L(Z)(1)	L(Z)(1)	L	H	On
1.8V (nom)	L	L	H	L	L(Z)(1), Y7 active	L(Z)(1), Y7 active	H	L	On
1.8V (nom)	H	X	L	H	L	H	L	H	On
1.8V (nom)	H	X	H	L	H	L	H	L	On
1.8V (nom)	X	X	L	L	L(Z)(1)	L(Z)(1)	L(Z)(1)	L(Z)(1)	Off
1.8V (nom)	X	X	H	H	Reserved				

Notes:
1. $L_{(Z)}$ means the outputs are disabled to a low state meeting the I_{ODL} limit on DC Specification

Absolute Maximum Ratings (Over operating free-air temperature range)

Symbol	Parameter	Min.	Max.	Units
V_{DDQ}, AV_{DD}	I/O supply voltage range and analog /core supply voltage range	-0.5	2.5	V
V_I	Input voltage range(2, 3)	-0.5	V_{DDQ} +0.5	
V_O	Output voltage range(2, 3)	-0.5	V_{DDQ} +0.5	
I_{IK}	Input clamp current	-50	50	mA
I_{OK}	Output clamp current	-50	50	
I_O	Continuous output current	-50	50	
$I_{O(PWR)}$	Continuous current through each V_{DDQ} or GND	-100	100	
T_{STG}	Storage temperature	-65	150	ºC

Notes:
1. Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

DC Specifications Recommended Operating Conditions

Symbol	Parameter		Min.	Typ.	Max.	Units
V_{DDQ}	Output supply Voltage		1.7	1.8	1.9	V
AV_{DD}	Supply voltage(4)			V_{DDQ}		
V_{IL}	Low-level input voltage(5)	OE, OS, CK, $\overline{CK}$			0.35 x V_{DDQ}	
V_{IH}	High-level input voltage(5)	OE, OS, CK, $\overline{CK}$	0.65 x V_{DDQ}			
I_{OH}	High-level output current, see Fig 2		-		-9	mA
I_{OL}	Low-level output current, see Fig. 2		-		9	
V_{IX}	Input differential-pair crossing voltage		(V_{DDQ}/2) -0.15		(V_{DDQ}/2) +0.15	
V_{IN}	Input voltage level		-0.3		V_{DDQ} +0.3	V
V_{ID}	Input differential voltage, See Fig 9 (5)	DC	0.3		V_{DDQ} +0.4	
		AC	0.6		V_{DDQ} +0.4	
T_A	Operating free air temperature		0		70	ºC

Notes:
4. The PLL is turned off and bypassed for test purposes when AV_{DD} is grounded. During this test mode, V_{DDQ} remains within the recommended operating conditions and no timing parameters are guaranteed.
5. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$, see Figure 9 for definition. The CK and $\overline{CK}$, V_{IH} and V_{IL} limits are used to define the DC low and high levels for the logic detect state.

Timing Requirements (Over recommended operating free-air temperature)

Symbol	Description		AV_{DD}, V_{DDQ} = 1.8V ±0.1V		Units
			Min.	Max.	
f_{CK}	Operation clock frequency(7, 9)		125	410	MHz
	Application clock frequency(7, 9)		160	410	
t_L	Stabilization time(10)	f_{CK} = 160 - 410 MHz		6	µs
t_{DC}	Input clock duty cycle		40	60	%
t_{OFF}	Device power down(10)			8	ns

Notes:

7. The PLL is able to handle spread spectrum induced skew.
8. Operating clock frequency indicates a range over which the PLL is able to lock, but in which it is not required to meet the other timing parameters. (Used for low-speed debug).
9. Application clock frequency indicates a range over which the PLL must meet all timing parameters.
10. Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up . During normal operation, the stabilization time is also the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal when CK and CK go to a logic low state, enter the power-down mode and later return to active operation. CK and CK maybe left floating after they have been driven low for one complete clock cycle.

DC Specifications

Parameter	Description	Test Condition	AV_{DD}, V_{DDQ}	Min.	Typ.	Max.	Units
V_{IK}	All Inputs	I_I= -18mA	1.7V			1.2	V
V_{OH}	HIGH output voltage	I_{OH} = -100µA	1.7 to 1.9V	V_{DDQ} -0.2			
		I_{OH} = -9mA	1.7	1.1			
I_{ODL}	Output disabled low current	OE = L, V_{ODL} = 100mV	1.7V	100			µA
V_{OD}	Output differential voltage, the magnitude of the difference between the true and complimentary outputs, see fig. 9 for dimentions			0.6			V
I_I	CK, $\overline{CK}$	V_I = V_{DDQ} or GND	1.9V			±250	µA
	OE, OS, FBIN, $\overline{FBIN}$	V_I = V_{DDQ} or GND				±10	
I_{DDLD}	Static Supply current, I_{DDQ} + I_{ADD}	CK and $\overline{CK}$ = L				500	
I_{DD}	Dynamic supply current, I_{DDQ} + I_{ADD}, see note 6 for CPD calculation	CK and $\overline{CK}$ = 410 MHz, all outputs are open (not connected to a PCB)				300	mA
CI	CK, $\overline{CK}$	V_I = V_{DDQ} or GND	1.8V	2		3	pF
	FBIN, $\overline{FBIN}$	V_I = V_{DDQ} or GND		2		3	
CI(Δ)	CK, $\overline{CK}$	V_I = V_{DDQ} or GND				0.25	
	FBIN, $\overline{FBIN}$	V_I = V_{DDQ} or GND				0.25	

Notes:

6. Total I_{DD} = I_{DDQ} + I_{ADD} = F_{CK} *C_{PD} *V_{DDQ}, solving for C_{PD} = (I_{DDQ} + I_{ADD})/(F_{CK}*V_{DDQ}) where F_{CK} is the input frequency, V_{DDQ} is the power supply and C_{PD} is the Power Dissipation Capacitance.

AC Specifications

Switching characteristics over recommended operating free-air temperature range (unless otherwise noted)(15)

Parameter	Description	Diagram	f_{CK} (MHz)	AV_{DD}, V_{DDQ} = 1.8V ±0.1V Min.	Nom.	Max.	Units
ten	OE to and Y/$\overline{Y}$	see Fig 11				8	ns
tdis	OE to and Y/$\overline{Y}$	see Fig 11				8	
tjit(cc+)	Cycle-to-cycle jitter	see Fig 4		0		40	ps
tjit(cc-)				0		-40	
t(Ø)	Static phase offset (11)	see Fig 5		-50		50	
t(Ø)dyn	Dynamic phase offset	see Fig 10		-50		50	
tsk(o)	Output clock skew	see Fig 6				40	
tjit(per)	Period jitter(12)	see Fig 7		-40		40	
tjit(hper)	Half period jitter (12)	see Fig 8	160 to 270	-75		75	
	Half period jitter (12)	see Fig 8	271 to 350	-50		50	
∑t(su)	| tjit(per) | + | t(Ø)dyn | + tsk(o) (see note 17)		271 to 410			80	
∑t(h)	| t(Ø)dyn | + tsk(o) (see note 17)		271 to 410			60	
slr(i)	Input clock slew rate	see Fig 9		1	2.5	4	V/ns
	Output enable (OE)	see Fig 9		0.5			
slr(o)	Output clock slew rate (14, 16)	see Fig 1, 9		1.5	2.5	3	
V_{OX}	Output differential-pair cross voltage(13)	see Fig 2		(V_{DDQ}/2) -0.1		(V_{DDQ}/ 2) +0.1	V
The PLL on the PI6CUA878 is capable of meeting all the above test parameters while supporting SSC synthesirers with the following parameters:							
	SSC modulation frequency			30.00		33	kHz
	SSC clock input frequency deviation			0.00		-0.50	%
PI6CUA878 PLL design should target the values below to minimize the SCC induced skew:							
	PLL Loop Bandwidth			2.0			MHz

Notes:

11. Static Phase Offset does not include Jitter
12. Period Jitter and Half-Period Jitter specifications are separate specifications that must be met independently of each other.
13. VOX specified at the DRAM clock input or the test load.
14. To eliminate the impact of input slew rates on static phase offset, the input slew rates of Reference Clock Input CK, $\overline{CK}$ and Feedback Clock Input FBIN, $\overline{FBIN}$ are recommended to be nearly equal. The 2.5V/ns slew rates are shown as a recommended target. Compliance with these Nom values is not mandatory if it can be adequately demonstrated that alternative characteristics meet the requirements of the registered DDR2 DIMM application.
15. There are two terminations that are used with the above ac tests. The load/board in Figure 2 is used to measure the input and output differential-pair cross-voltage only. The load/board in Figure 3 is used to measure all other tests. For consistency, equal length cables should be used.
16. The Output slew rate is determined from IBIS model load shown in Figure 1. It is measured single-ended.
17. In the Frequency Range of 271 MHz to 410 MHz, the minimum and maximum values for tjit(per) and (t(Ø)dyn and the minimum value for tsk(o) must not exceed the corresponding minimum and maximum values of the 160 MHz to 270 MHz range and sum of the specified values for | tjit(per) |, | t(Ø)dyn | and tsk(o) must meet the requirement for ∑t(su) and the sum of the specified values for | t(Ø)dyn | adn tsk(o) must meet the requirment for ∑t(h).

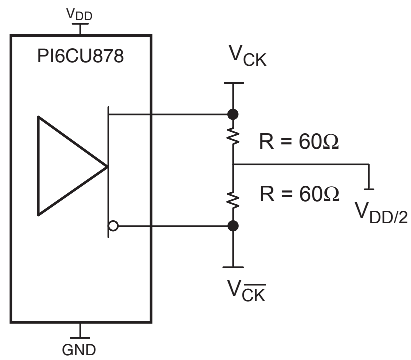


Figure 1. IBIS Model Output Load

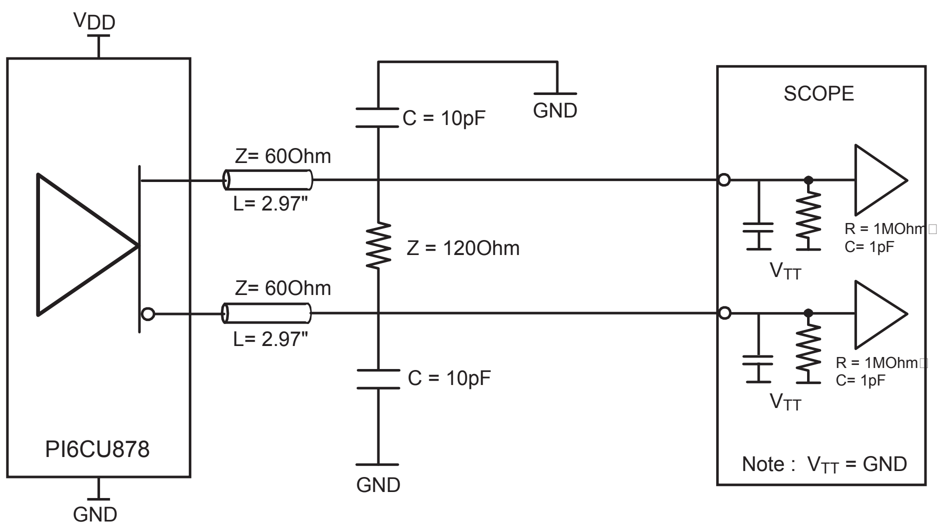


Figure 2. Output Load Test Circuit 1

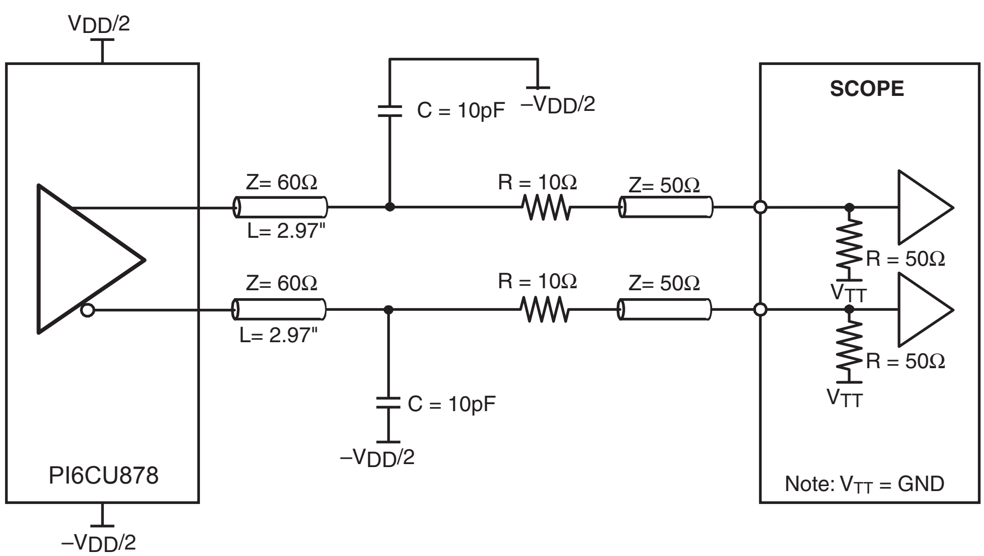


Figure 3. Output Load Test Circuit 2

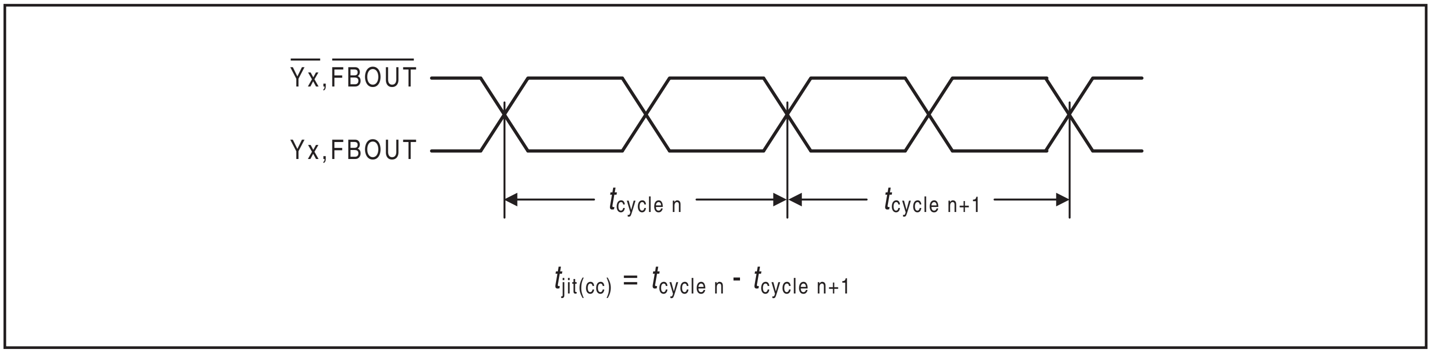


Figure 4. Cycle-to-Cycle Jitter

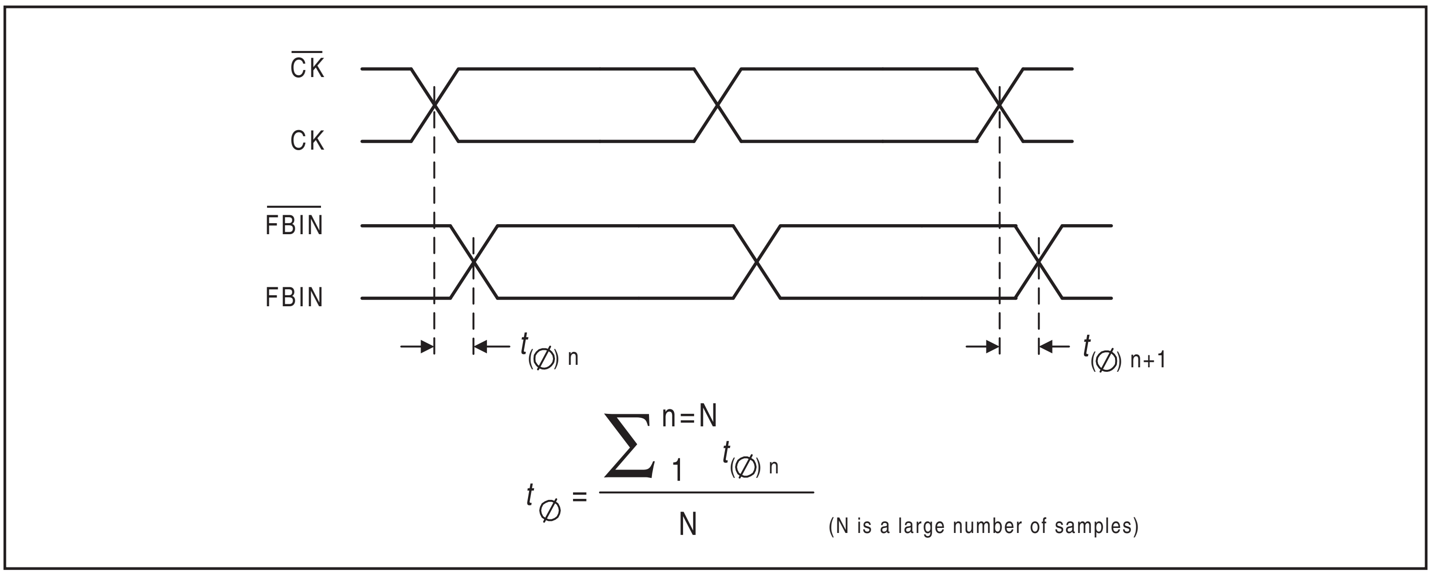


Figure 5. Static Phase Offset

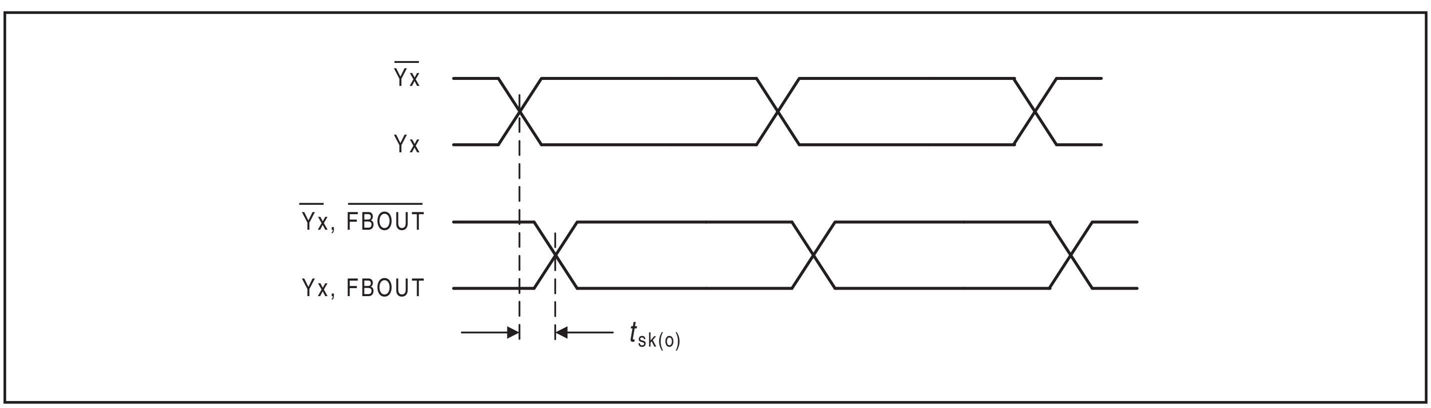


Figure 6. Output Skew

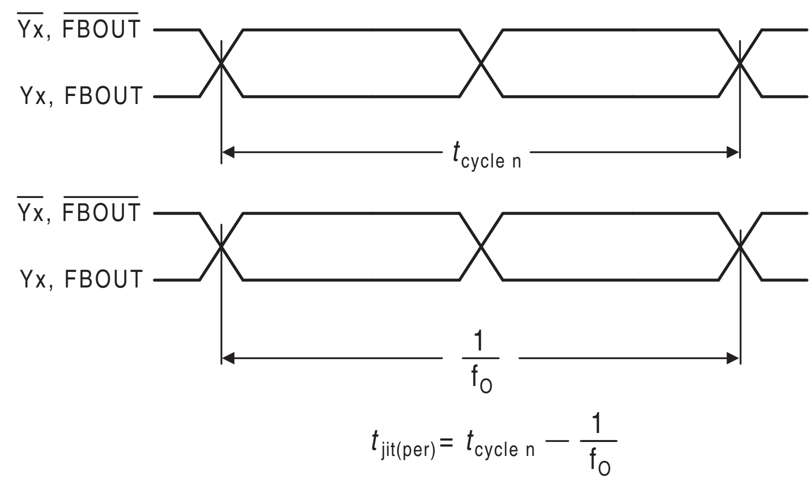


Figure 7. Period Jitter (fo = average input frequency measured at CK/$\overline{CK}$)

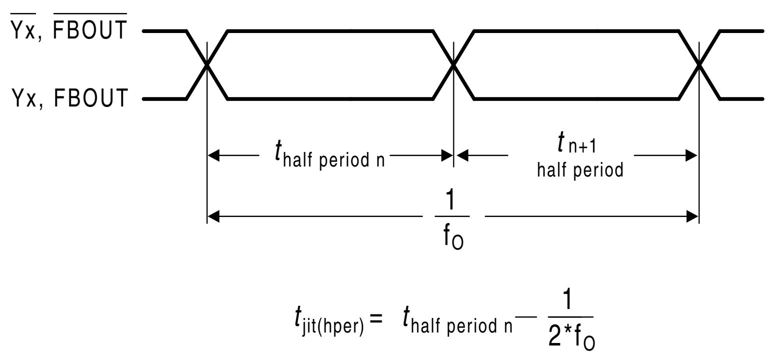


Figure 8. Half-Period Jitter

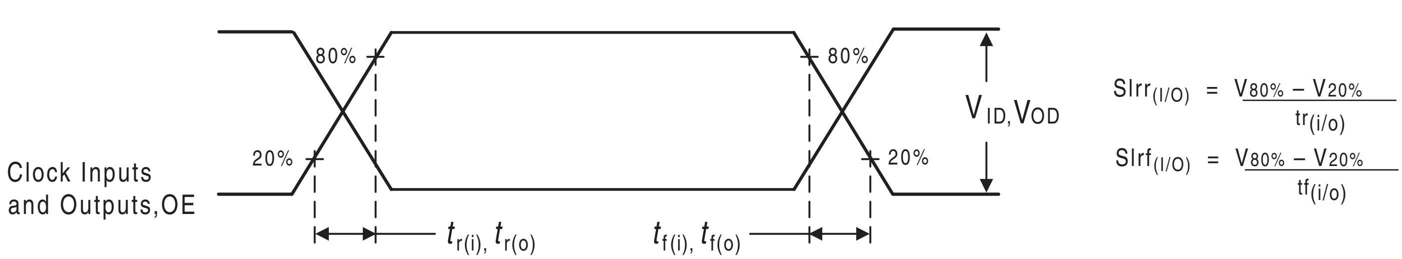


Figure 9. Input and Output Slew Rates

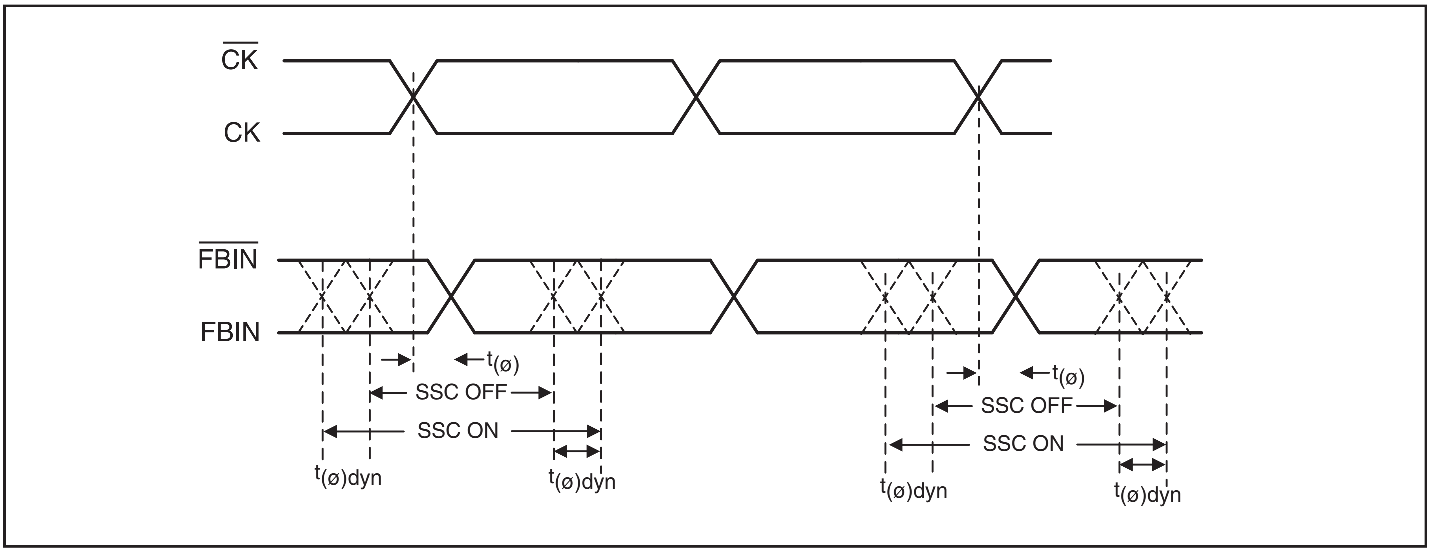


Figure 10. Dynamic Phase Offset

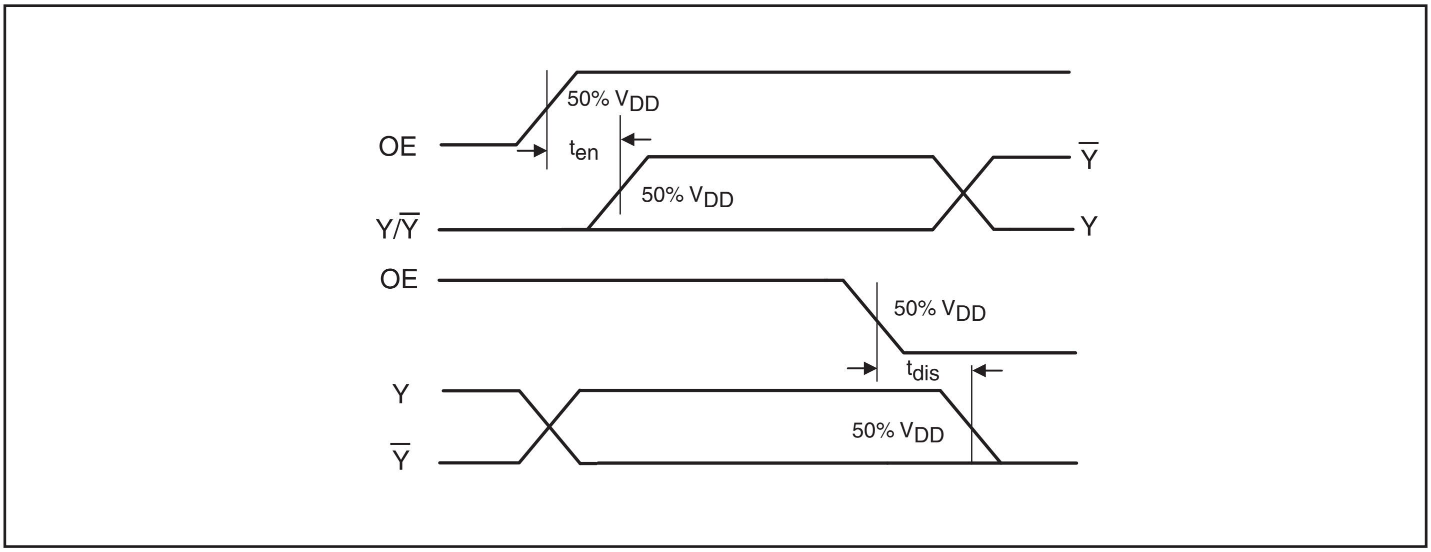


Figure 11. Time Delay Between Output Enable (OE) and Clock Output ($\overline{Y}$, Y)

Packaging Mechanical: 52-Pin VFBGA (NF)

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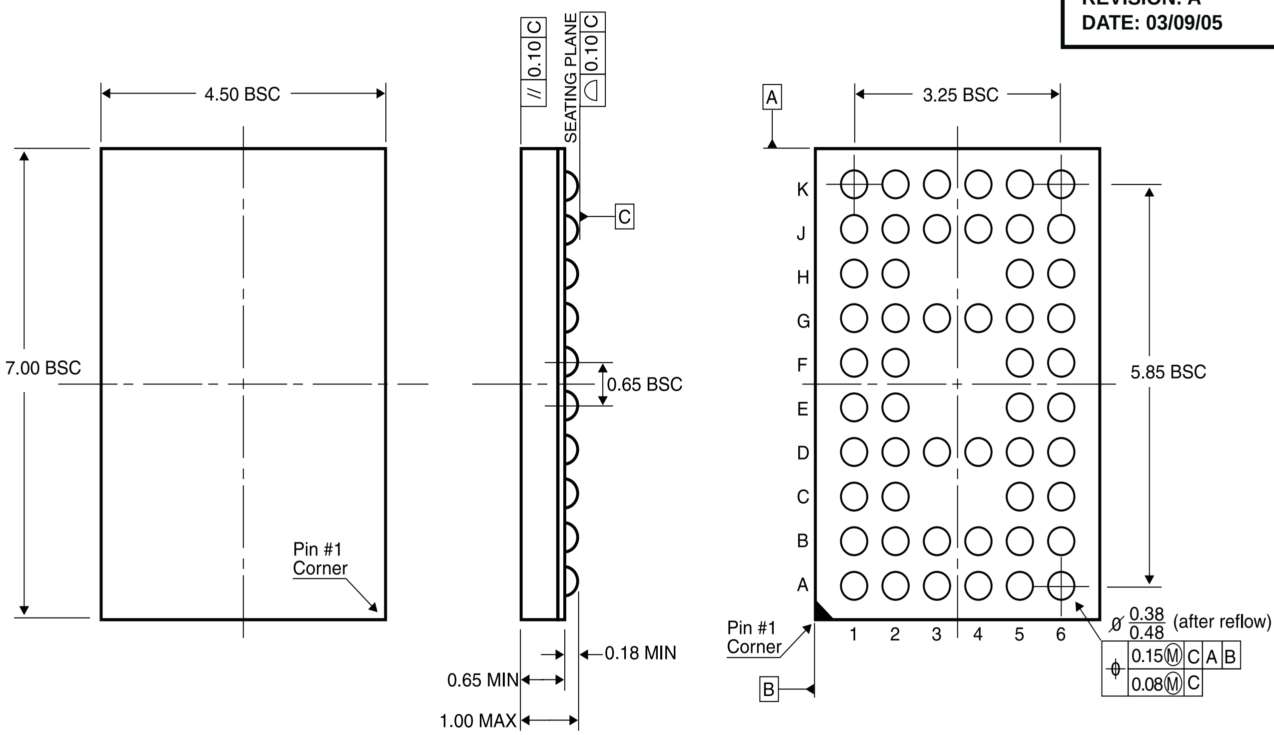

Notes:
1) Controlling dimensions in millimeters
2) Ref: JEDEC MO-225B/BA

Pericom Semiconductor Corporation
3545 N. 1st Street, San Jose, CA 95134
1-800-435-2335 • www.pericom.com

DESCRIPTION: 52-Ball, Very Thin Profile Fine Pitch Ball Grid Array, VFBGA

PACKAGE CODE: NF

Ordering Information

Ordering Code	Packaging Code	Package Type
PI6CUA878NFE	NF	Pb-free & Green, 52-ball VFBGA

Notes:

1. Thermal characteristics can be found on the company web site at http://www.pericom.com/packaging/