Features

- **SPARC V8 High-performance Low-power 32-bit Architecture**
  - **8 Register Windows**
- **Integrated 32/64-bit Floating Point Unit**
- **Advanced Architecture**
  - **On-chip AMBA Bus**
  - **5-stage Pipeline**
  - **16-Kbyte Multi-sets Data Cache**
  - **32-Kbyte Multi-sets Instruction Cache**
- **On-chip Peripherals**
  - **Memory Interface**
    Chip Select Generator
    Waitstate Generator
    SDRAM Controller
  - **Timers**
    Two 24-bit Timers
    Watchdog Timer
  - **Two 8-bit UARTs**
  - **Interrupt Controller with 4 External Programmable Inputs**
  - **32 Parallel I/O Interface**
  - **33 MHz PCI Interface Compliant with 2.2 PCI Specification**
- **Fault Tolerance by Design**
  - **Full Triple Modular Redundancy (TMR)**
  - **EDAC Protection**
  - **Parity Protection**
- **Debug and Test Facilities**
  - **Debug Support Unit (DSU) for Trace and Debug**
  - **IEEE 1149.1 JTAG Interface**
  - **Four Hardware Watchpoints**
- **Speed Optimized Code RAM Interface**
  8 or 40-bit boot-PROM (Flash) Interface Possibilities
- **Clock: 100 MHz (Target)**
- **Core Consumption: To Be Defined**
- **Performance: To Be Defined**
- **Voltage Operating Range: 3.3V I/O - 1.8V Core**
- **Temperature Operating Range: -55°C to 125°C**
- **Total Dose Radiation Capability (Parametric & Functional)**
  - **100 Krads (Si) (Target)**
- **Latch-up Immunity Better than 70 MeV.cm²/mg (Target)**
- **Package: MCGA 349 (Multi-Layer Column Grid Array)**

Overview

The AT697E is a highly-integrated, high-performance 32-bit RISC embedded processor implementing the SPARC architecture V8 specification. The implementation is based on the European Space Agency (ESA) LEON2 fault tolerant model.

The processor is manufactured using the Atmel standard 0.18 µm CMOS commercial process. It operates at a low voltage. It has been especially designed for space, as it has on-chip concurrent transient and permanent error detection.

The AT697E includes an on-chip Integer Unit (IU), a Floating Point Unit (FPU), separate instruction and data caches, hardware multiplier and divider, interrupt controller, debug support unit with trace buffer, two 24-bit timers, Parallel and Serial interfaces, Idle mode function, Watchdog, a PCI Interface and a flexible Memory Controller.

The design is highly testable with the support of a Debug System Unit (DSU) and a boundary scan through JTAG interface.

Rad-Hard 32-bit SPARC Embedded Processor

AT697E

Advance Information

Summary
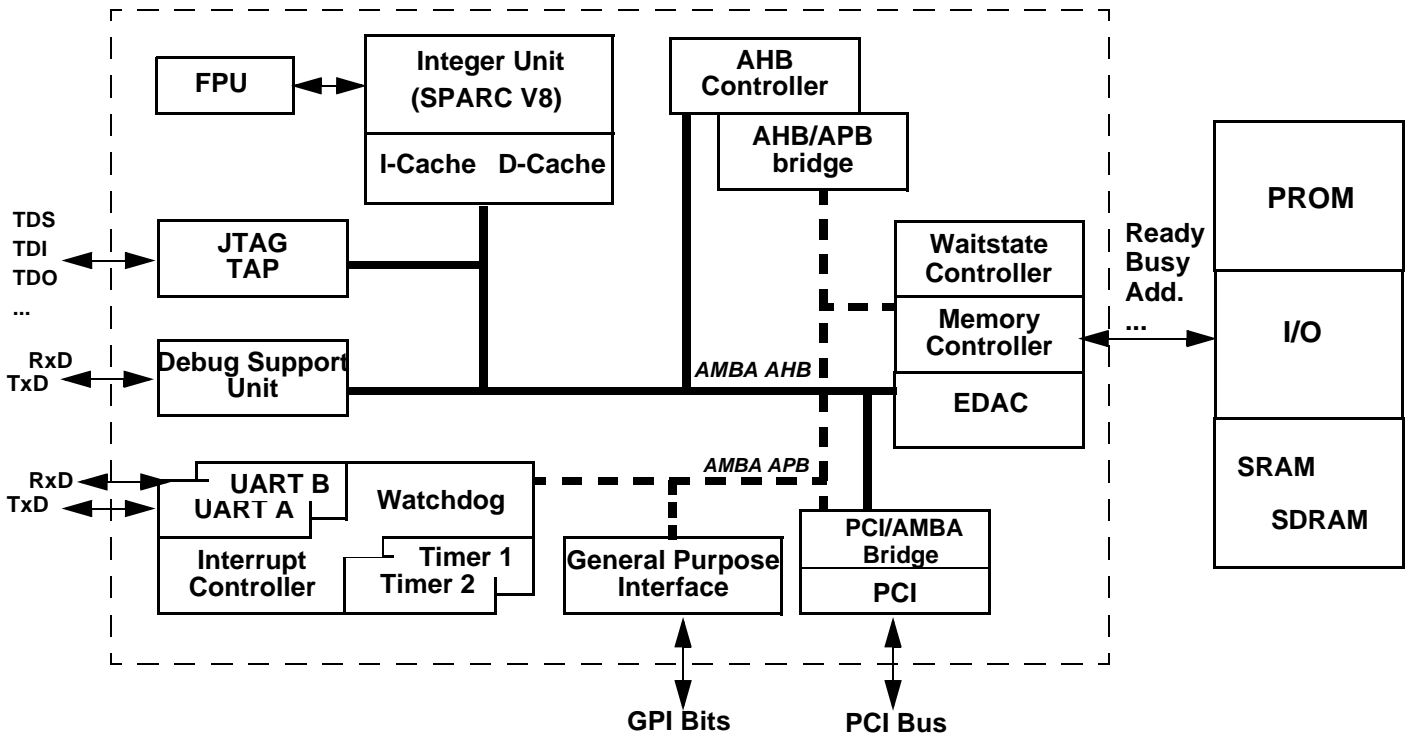
Block Diagram

Figure 1. AT697E Block Diagram

Pin Description

Signal	Type	Active	Description	
A[27:0]	Output	High	Memory address	
D[31:0]	Bidir	High	Memory Data	
CB[7:0]	Bidir	High	Check bits	
BEXC	Input	Low	Bux exception	
BRDY	Input	Low	Bus Ready Strobe	
IOS	Output	Low	Local I/O select	
OE	Output	Low	Output Enable	
RAMOE [4:0]	Output	Low	SRAM output enable	
RAMS [4:0]	Output	Low	SRAM chip-select	
READ	Output	High	Read strobe	
ROMS [1:0]	Output	Low	PROM chip select	
RWE [3:0]	Output	Low	SRAM write enable	
SDCAS	Output	Low	SDRAM column address strobe	
SDCLK	Output	–	SDRAM clock	

(Continued)

Signal	Type	Active	Description	
SDCS [1:0]	Output	Low	SDRAM chip select	
SDDQM [3:0]	Output	Low	SDRAM data mask	
SDRAS	Output	Low	SDRAM row address strobe	
SDWE	Output	Low	SDRAM write enable	
WRITE	Output	Low	Write strobe	
CLK	Input	High	System Clock	
ERROR		Low	System Error	
PIO[15..0]	Bidir		Parallel I/O interface	
RST	Input	Low	System Reset	
WDOG	Output	Low	Watchdog Output	
DSUACT	Output	High	DSU Active	
DSUBRE	Input	High	DSU Break	
DSUEN	Input	High	DSU Enable	
DSURX	Input	High	DSU UART Input	
DSUTX	Output	High	DSU UART Output	
TCK	Input		Test (JTAG) clock	
TRST	Input	Low	Test (JTAG) reset	
TMS	Input		Test (JTAG) mode select	
TDI	Input		Test (JTAG) data input	
TDO	Output		Test (JTAG) data output	
PA[31:0]	In/Out	High	PCI Address	
C/BE[3:0]	In/Out	Low	PCI byte enable	
PAR	In/Out		PCI parity	
FRAME	In/Out	Low	PCI cycle frame	
TRDY	In/Out	Low	PCI target ready	
IRDY	In/Out	Low	PCI initiator ready	
STOP	In/Out	Low	PCI stop	
DEVSEL	In/Out	Low	PCI device select	
IDSEL	Input	high	PCI initialization device select	
PERR	In/Out	Low	PCI parity error	
SERR	In/Out	Low	PCI system error	
REQ	Output	Low	PCI bus request	
GNT	Input	Low	PCI bus granted	
PCLK	Input		PCI clock	

Signal	Type	Active	Description	
PRST	Input	Low	PCI	
LOCK	In/Out	Low	PCI	
HOST	Input	Low	Host/Satellite mode selection	
AGNT [3:0]	Output	Low	PCI bus granted	
AREQ [3:0]	Input	Low	PCI bus request	
BYPASS	Input	High	Enable/Disable PLL	
CLKDIV4	Output		PLL divider clock output	
PLOCK	Output	High	PLL lock	
FLT	Analog		Passive filter	
VCC18			Dedicated power supply	1.8V
VCC33			Dedicated power supply	3.3V
VSS			Dedicated power supply	0V
TEST			Test mode	

Product Description

Integer Unit
The AT697E integer unit (IU) implements SPARC integer instructions as defined in *SPARC Architecture Manual Version 8.* The IU is designed for highly dependable space and military applications, and includes support for error detection. The RISC architecture makes possible the creation of a processor that can execute instructions at a rate approaching one instruction per processor clock.

Floating Point Unit (FPU)
The FPU is designed to provide execution of single and double-precision floating point instructions. The processor is stopped during the execution of floating point instructions.

Instruction Set
AT697E instruction set describes six functional categories: load/store, arithmetic/logical/shift, control transfer, read/write control register, floating-point, and miscellaneous. Please refer to SPARC V8 architecture manual that presents implemented instructions.

Cache Sub-System
Separate instruction and data caches are provided. The instruction cache uses streaming during line-refill to minimize refill latency. The data cache uses writethrough policy and implements a double-word write-buffer. The data cache also performs bus-snooping on the AHB bus.

Memory Interface
The AT697E is designed to allow easy interfacing to internal/external memory resources. The flexible memory interface provides a direct interface for PROM, memory mapped I/O devices, static RAM (SRAM) and synchronous dynamic RAM (SDRAM). The memory areas can be programmed to either 8-, 16- or 32-bit data width.

Address Range	Size	Mapping
0x00000000 - 0x1FFFFFFF	512 MB	PROM
0x20000000 - 0x3FFFFFFF	512 MB	I/O
0x40000000 - 0x7FFFFFFF	1 GB	SRAM/SDRAM

Fault Tolerance
The AT697E includes fault tolerance features to prevent the processor from arbitrary single-event upset errors. This feature is implemented to withstand these errors without data loss. AT697E device is based on a full triple modular redundancy design.

The main features that make AT697E radiation tolerant are the following:

- Three internal clock trees
- Register file protection
- Data protection
- Cache protection

TRAPs

The AT697E supports two types of traps:

- Synchronous traps
- Asynchronous traps also called interrupts

Synchronous traps are caused by hardware responding to a particular instruction: they occur during the instruction that caused them. Asynchronous traps occur when an external event interrupts the processor. They are not related to any particular instruction and occur between the execution of instructions.

Timers

General Purpose Timers

Two 24-bit timers are provided on-chip. The timers can work in periodic or one-shot mode. Both timers are clocked by a common 10-bit prescaler.

Watchdog Timer

A 24-bit watchdog is provided on-chip. The watchdog is clocked by the timer prescaler. When the watchdog reaches zero, an output signal (WDOG) is asserted. This signal can be used to generate system reset.

Communication Interfaces

Serial Interfaces – UARTs

Two full duplex asynchronous receiver transmitters (UART) are included. The data format of the UART's is eight data bits with one stop bit. It is possible to choose between no parity, even and odd parity. UART's provide double buffering, i.e. each UART consists of a transmitter holding register, a receiver holding register, a transmitter shift register, and a receiver shift register. Each of these registers are 8-bit wide. For each UART a data register is provided. The baud rate of both the UART's is individually programmable.

Parallel Interface

A 32-bit parallel I/O port is provided. 16 bits are always available and can be individually programmed by software to be an input or an output. The additional 16 bits are only available when the memory bus is configured for 8- or 16-bit operation.

Some of the bits have alternate usage, such as UART inputs/outputs and external interrupts inputs.

PCI interface

The PCI implementation standing on the AT697E is PCI 2.2 compliant. It is a high performance 32-bit bus with multiplexed address and data lines. It is intended for use as an interconnect mechanism between processor/memory systems and peripheral controller components.

Test and Diagnostics   The design is highly testable with the support of a Debug System Unit (DSU), an internal and boundary scan through JTAG interface.

Test Access Port (TAP)   A TAP is provided through a JTAG interface.

DSU   The on-chip debug support unit (DSU) allows non-intrusive debugging on target hardware. The DSU allows to insert instruction and data watchpoints, and access to all on-chip registers from a remote debugger. A trace buffer is provided to trace the executed instruction flow and/or AHB bus traffic. Communication to an outside debugger (e.g. gdb) is done using a dedicated UART (RS232).

Watchpoint Registers   To aid software debugging, up to four watchpoint registers are provided. Each register can cause a debug-trap on an arbitrary instruction or data address range. If the debug support unit is enabled, the watchpoints can be used to enter debug mode.

Signals Description

All signals are clocked on the rising edge of CLK.

IU and FPU Signals

A[27:0] – Address Bus (Output)

These active high outputs carry the address during accesses on the memory bus. When no access is performed, the address of the last access is driven (also internal cycles).

D[31:0] – Data Bus (Bi-directional)

D[31:0] carries the data during transfers on the memory bus. The processor only drives thebus during write cycles. During accesses to 8-bit areas, only D[31:24] are used.

CB[7:0] – Check Bits (Bi-directional)

CB[6:0] carries the EDAC checkbits. CB[7][1] takes the value of tcb[7] in the error control register. Processor only drives CB[7:0] during write cycles to areas programmed to be EDAC protected.

Note: 1. CB[7] is implemented to enable programming of flash memories. When only 7 bits are useful for EDAC protection, 8 are needed for programming. That is why there is an addition 8th bit in the check bits.

Memory Interface Signals

Globals

OE* – Output Enable (Output)

This active low output is asserted during read cycles on the memory bus.

BRDY* – Bus Ready (Input)

This active low input indicates that the access to a memory mapped I/O area can be terminated on the next rising clock edge.

READ – Read Cycle

This active high output is asserted during read cycles on the memory bus.

WRITE* – Write Enable (Output)

This active low output provides a write strobe during write cycles on the memory bus.

PROM	**ROMS*[1:0] – PROM Chip-select (Output)**

These active low outputs provide the chip-select signal for the PROM area. ROMSN[0] is asserted when the lower half of the PROM area is accessed (0 - 0x10000000), while ROMSN[1] is asserted for the upper half.

SRAM   **RAMOE*[4:0] – RAM Output Enable (Output)**

These active low signals provide an individual output enable for each RAM bank.

RAMS*[4:0] – RAM Chip-select (Output)

These active low outputs provide the chip-select signals for each RAM bank.

RWEN [3:0] – RAM Write Enable (Output)

These active low outputs provide individual write strobes for each byte lane. RWEN[0] controls D[31:24], RWEN[1] controls D[23:16], etc.

I/O   **IOS* – I/O Select (Output)**

This active low output is the chip-select signal for the memory mapped I/O area.

SDRAM Interface   **SDCLK – SDRAM Clock**

SDRAM clock, can be configured to be identical or inverted in relation to the system clock.

SDCASN – SDRAM Column Address Strobe

This active low signal provides a common CAS for all SDRAM devices.

SDCSN[1:0] – SDRAM Chip Select

These active low outputs provide the chip select signals for the two SDRAM banks.

SDDQM[3:0] – SDRAM Data Mask

These active low outputs provide the DQM signals for both SDRAM banks.

SDRAS* – SDRAM Row Address Strobe

This active low signal provides a common RAS for all SDRAM devices.

SDWEN – SDRAM Write Strobe

This active low signal provides a common write strobe for all SDRAM devices.

System Signals

CLK – Processor Clock (Input)

This active high input provides the main processor clock.

RESET* – Processor Reset (Input)

When asserted, this active low input will reset the processor and all on-chip peripherals.

WDOG* – Watchdog Time-out (Open-drain Output)

This active low output is asserted when the watchdog times-out.

BEXC* – Bus Exception (Input)

This active low input is sampled simultaneously with the data during accesses on the memory bus. If asserted, a memory error will be generated.

ERROR* – Processor Error (Open-drain Output)

This active low output is asserted when the processor has entered error state and is halted. This happens when traps are disabled and an synchronous (un-maskable) trap occurs.

TEST – Test Mode Input

When asserted, this active high input will make processor enter test mode.

PIO[15:0] – Parallel I/O Port (Bi-directional)

These bi-directional signals can be used as inputs or outputs to control external devices.

BYPASS – PLL Bypass

When asserted, this active high input set the PLL in bypass mode. The device is directly clocked by the external clock. When not asserted, the device is clocked through the PLL.

PDIV4 – PLL Divider Output

This output provides the main clock delivered by the PLL inner divider.

SKEW[1:0] – Clock Tree Skew

This input signals configure the programmable skew on the redundant clock trees.

PLOCK – PLL Lock

This active high output is asserted when the PLL is locked in the functioning frequency corresponding to the input command

PLFT – PLL Passive Low Pass Filter

This input is used to connect the PLL passive low pass filter.

SKEW[0:1] – Skew on Internal Clocks

Those inputs are used to program the skew on internal clock trees

DSU Signals

DSUACT – DSU Active (Output)

This active high output is asserted when the processor is in debug mode and controlled by the DSU.

DSUBRE – DSU Break Enable

A low-to-high transition on this active high input will generate break condition and put the processor in debug mode.

DSUEN – DSU Enable (Input)

The active high input enables the DSU unit. If de-asserted, the DSU trace buffer will continue to operate but the processor will not enter debug mode.

DSURX – DSU Receiver (Input)

This active high input provides the data to the DSU communication link receiver

DSUTX – DSU Transmitter (Output)

This active high input provides the output from the DSU communication link transmitter.

JTAG Signals

TCK – Test Clock (Input)

Used to clock serial data into scan latches and control sequence of the test state machine. TCK can be asynchronous with CLK.

TMS – Test Mode Select (Input)

Primary control signal for the state machine. Synchronous with TCK. A sequence of values on TMS adjusts the current state of the TAP.

TDI – Test Data Input (Input)

Serial input data to the scan latches. Synchronous with TCK

TDO – Test Data Output (Output)

Serial output data from the scan latches. Synchronous with TCK

TRST – Test Reset (Input)

Resets the test state machine. can be asynchronous with TCK

PCI Arbiter

AREQ*[3:0] – PCI Bus Request (Input)

When asserted, this active low input indicates that a PCI agent is requesting the bus.

AGNT*[3:0] – PCI Bus Grant (Output)

When asserted, this active low output indicates that PCI agent is granted the PCI bus.

PCI Interface Signals

PA[31:0] – PCI Address Data

Address and Data are multiplexed on the same PCI pins.

During the address phase, AD[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases, AD[07::00] contain the least significant byte and AD[31::24] contain the most significant byte.

C/BE[3:0]* – PCI Bus Command and Byte Enables

During the address phase of a transaction, C/BE[3::0]# define the bus command. During the data phase, C/BE[3::0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase.

PAR – Parity

The number of "1"s on AD[31::00], C/BE[3::0]#, and PAR equals an even number

FRAME* – Cycle Frame

It is driven by the current master to indicate the beginning and duration of an access. FRAME* is asserted to indicate a bus transaction is beginning. While FRAME* is asserted, data transfers continue. When FRAME* is deasserted, the transaction is in the final data phase or has completed.

IRDY* – Initiator Ready

IRDY* indicates the initiating agent's ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. During a write, IRDY# indicates that valid data is present on AD[31::00]. During a read, it indicates the master is prepared to accept data.

TRDY* – Target Ready

TRDY* indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates the target is prepared to accept data.

STOP* – Stop

STOP* indicates the current target is requesting the master to stop the current transaction.

LOCK* – Lock

LOCK* indicates an atomic operation to a bridge that may require multiple transactions to complete.

IDSEL – Initialization Device Select

Initialization Device Select is used as a chip select during configuration read and write transactions.

DEVSEL* – Device Select

When actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL* indicates whether any device on the bus has been selected.

REQ* – PCI Bus Request

REQ* indicates to the arbiter that this agent desires use of the bus. This is a point-to-point signal. Every master has its own REQ* which must be tri-stated while RST* is asserted.

GNT* – PCI Bus Grant

GNT* indicates to the agent that access to the bus has been granted. This is a point-to-point signal. Every master has its own GNT# which must be ignored while RST# is asserted.

PCLK – PCI Clock

Clock provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RST*, are sampled on the rising edge of CLK and all other timing parameters are defined with respect to this edge.

RST* – PCI Reset

Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state.

PERR* – Parity Error

Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected.

SERR* – System Error

System Error is for reporting address parity errors, data parity errors on the special cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required.

HOST – PCI Host

To be defined.

Package Description

MCGA 349 Package
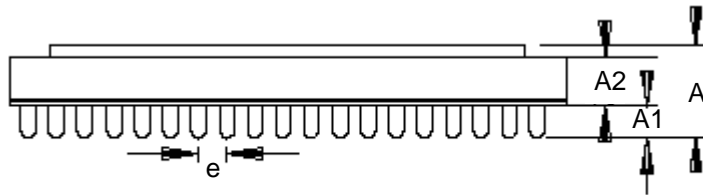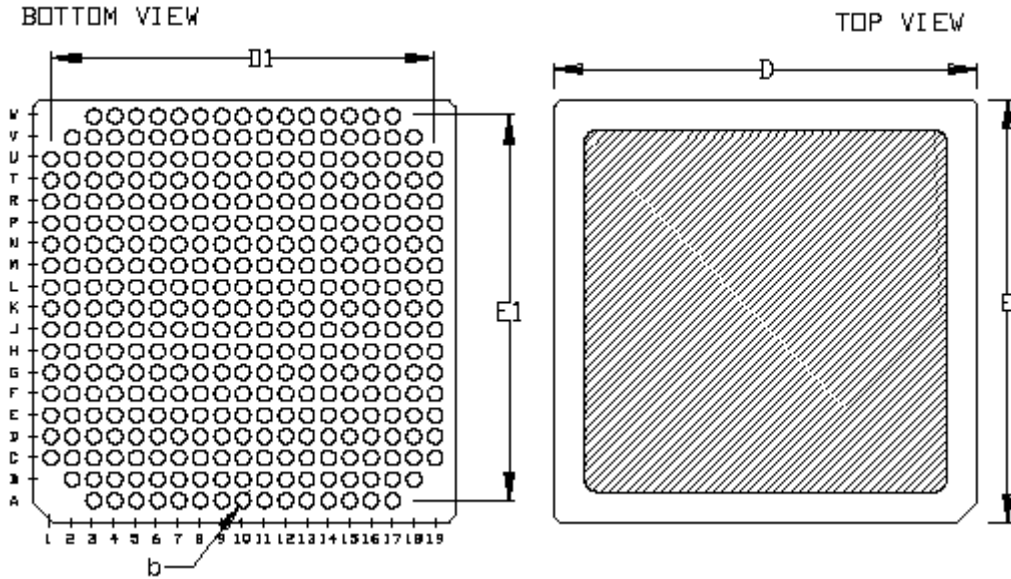
	mm		inch	
	min	max	min	max
D/E	24,8	25,2	0,976	0,992
D1/E1	22,86		0,9	
A1	1,4	1,85	0,055	0,073
A2	2,4	3,45	0,094	0,136
A	4,3	5,9	0,169	0,232
b	0,79	0,99	0,031	0,04
e	1,27		0,05	

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