x-mGC

Part Number: FCU-022M101

Features

- **Compliant with IEEE802.3ak (10GBASE-CX4)**
- **X2 MSA Rev 1.0b Compatible module**
- **Industry standard electrical connector, microGiGaCN™ (I/O interface)**
- **XAUI Four channel electrical interface (Host side card edge)**
- **XAUI Standard 70 pin connector for host connection**
- **Front panel hot swap ability.**
- **X2 MSA Rev 1.0b compliant MDIO**
- **Link Alarm Status Interrupt (LASI) support**
- **Total Power consumption under 3.0 watt**
- **20 meters over standard InfiniBand copper cable (24AWG)**
- **With media detect converter (o-mGC), up to 300 meters over standard multi mode fiber.**
- **No external clocks requirement – oscillator on board**

Description

The x-mGC is a 10Gigabit Ethernet CX4 Module that designed to ease X2 MSA Rev 1.0b and it is an electrical module that incorporates the complete physical layer functionality from XAUI compliant 4 lanes x 3.125 Gb/s four differential electrical interface to the microGiGaCN™ CX4 compliant electrical interface. The x-mGC is plugged into a X2 hosting system and connects to a 4X InfiniBand cable. The control interface (MDIO)is also integrated. The x-mGC module includes 10Gb/s Ethernet transmitter and receiver ports. The host may control the x-mGC registers using XAUI interface as defined in the X2 MSA. The MUX/DEMUX, XAUI interface and MDIO management functions are all integrated into the module, as is a precision oscillator that removes any need for an external reference clock.

x-mGC Block Diagram

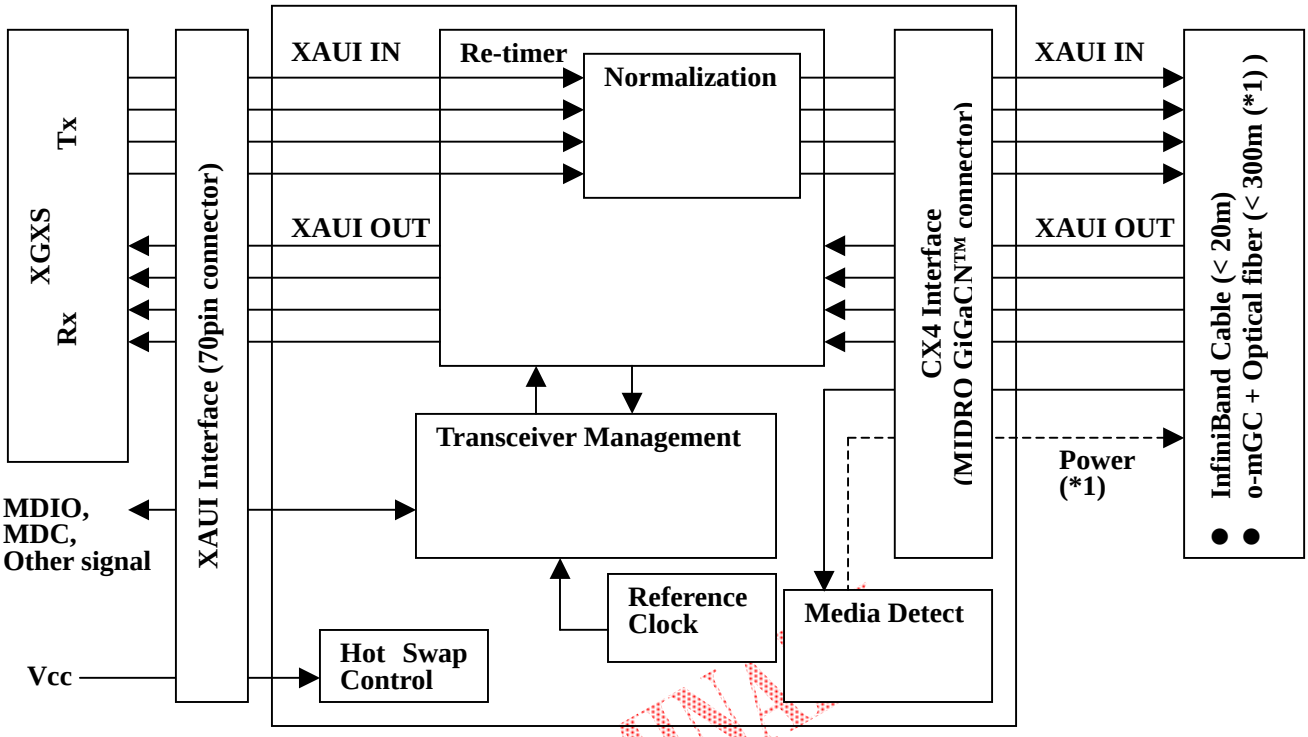


Figure 1: Functional Brock Diagram of x-mGC module

(*1) In case of InfiniBand cable is connected, the power does not supply to cable, and if o-mGC is connected, a ground contact is changed Vcc for power supply to o-mGC by Media detect function.

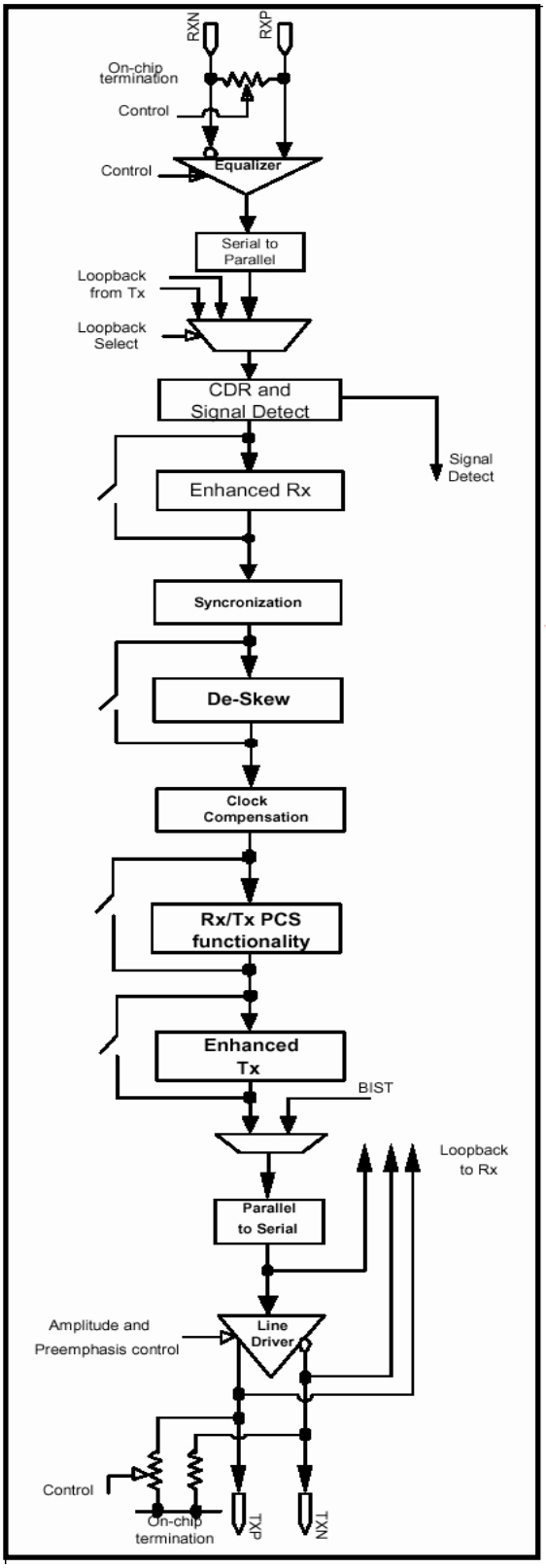
General Electrical Specification

- Interface: XAUI side; 70 pin SMT connector (See X2 MSA Rev1.0b, chapter 6.7)
  CX4 side; InfiniBand 4X connector (microGiGaCN™ , Fujitsu Component LTD. Patent)
- Differential signal rate: Tx and Rx each 3.125 Gb/s x 4 pair
- Impedance: 100 ohms differential, AC-coupled I/O
- Adaptable Cable and Link Length: ; InfiniBand 4X cable 20m over
- Supply Voltage: 3.3V and 1.5V
- Supports standard LVCMOS 1.2V host interface.

Environmental Specification

- Operating case temperature: 0 - 70 degree (In an uniform air flow of 0.5 m/s.)
- Power consumption: 2.1 Watt Max

Figure 2: Top Level Brock Diagram of x-mGC Driver



Technical specification

Table 1: Transmitter characteristics

Parameter	Typical	Units	Notes
Signal data rate	3.125	Gb/s	+/-100ppm
Unit interval (UI) nominal	320	ps	
Differential peak to peak output voltage Maximum Minimum	 1200 800	 mVp-p mVp-p	
Differential peak to peak output voltage difference	150	mVp-p	Maximum
Differential output return loss	See figure 3	dB	Minimum
Differential output template	See figure 4	V	
Transition time (20-80%) Maximum Minimum	 130 60	 ps ps	
Output jitter Random jitter Deterministic jitter Total jitter	 0.27 0.17 0.35	 UIpp UIpp UIpp	

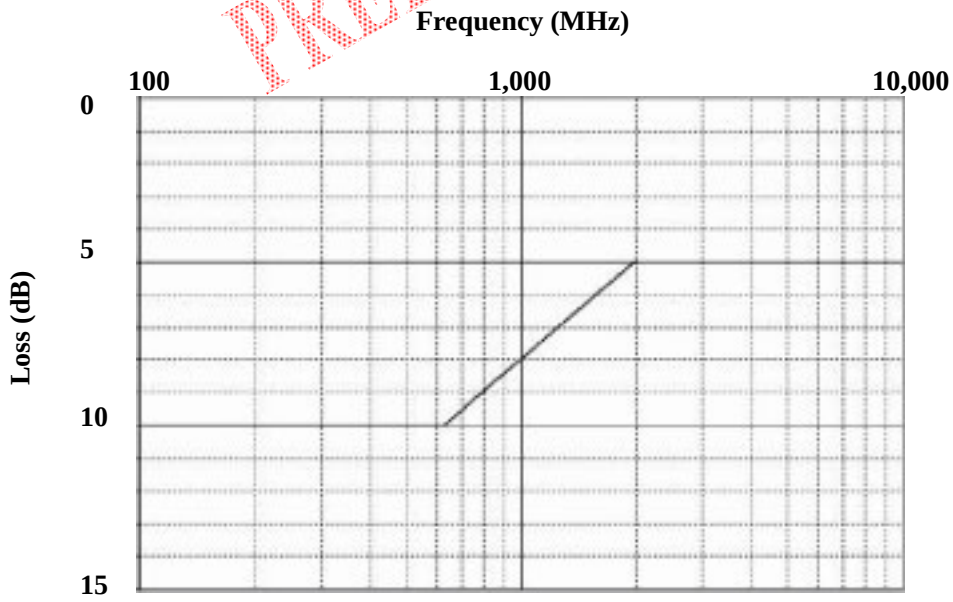


Figure 3: Transmit differential output return loss

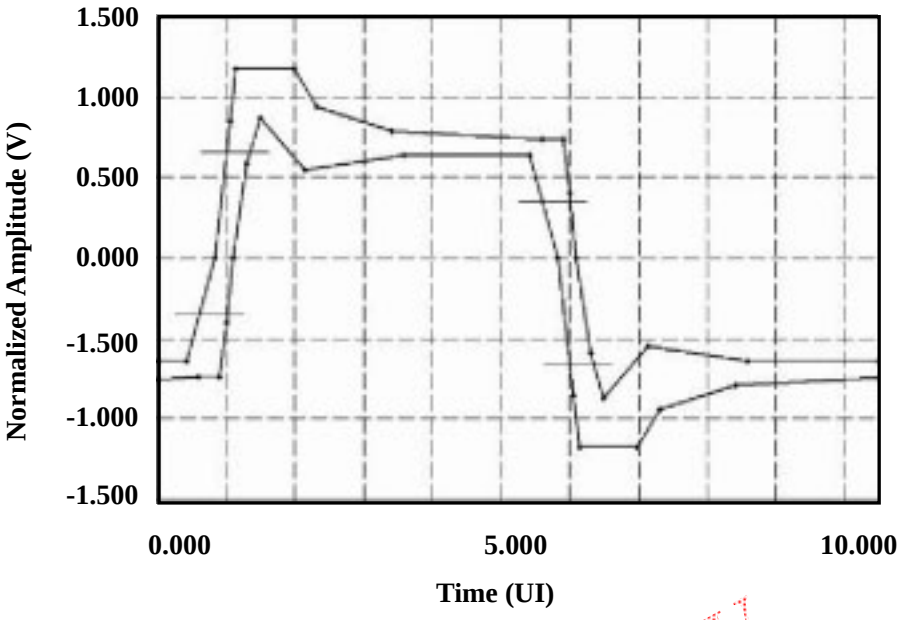


Figure 4: Normalized transmit template

Table 2: Receiver characteristics

Parameter	Typical	Units	Notes
Bit error ratio	10^{-12}		
Signal data rate	3.125	Gb/s	+/-100ppm
Unit interval (UI) nominal	320	ps	
Differential input amplitude	1200	mVp-p	Maximum
Return loss differential (minimum)	See figure 3	dB	100ohm

XAUI Interface

Table 3: Driver characteristics

Parameter	Typical	Units	Notes
Transmit data rate	3.125	Gb/s	+/-100ppm
Unit interval nominal	320	ps	
Differential amplitude	1600	mVp-p	Maximum
Absolute output voltage limits Maximum Minimum	 2.3 -0.4	 V V	
Differential skew	15	ps	Maximum
Differential output return loss	10	dB	Minimum
Common mode output return loss	6	dB	Minimum
Eye mask	See figure 5		

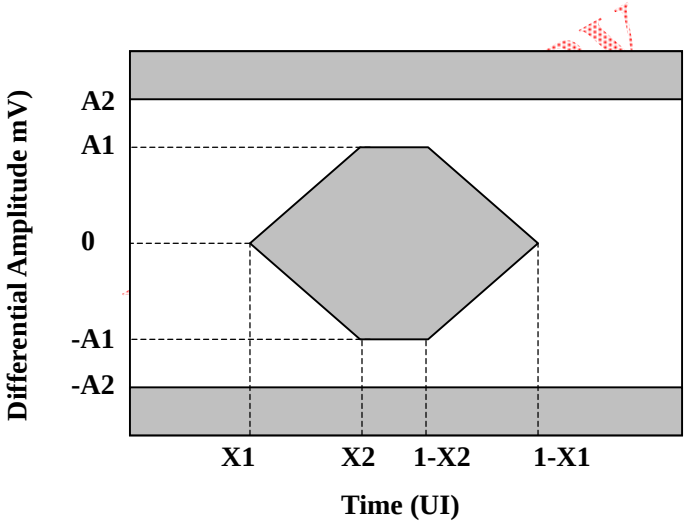


Figure 5: Driver Template

Table 4: Driver Template

Symbol	Near-End Value	Far-End Value	Units
X1	0.175	0.275	UI
X2	0.390	0.4	UI
A1	400	100	mV
A2	800	800	mV

Table 5: Receive Input parameters

Parameter	Typical	Units	Notes
Transmit data rate	3.125	Gb/s	+/-100ppm
Unit interval nominal	320	ps	
Differential input amplitude Maximum Minimum	 1600 200	 mVp-p mVp-p	
Return loss Differential Common	 10 6	 dB dB	
Input differential skew	75	ps	Maximum
Jitter amplitude tolerance Peak-to-peak total jitter Peak-to-peak deterministic jitter	 0.65 0.47	 UIpp UIpp	

x-mGC XAUI Pin out

70	GND	1	GND
69	GND	2	GND
68	RESERVED	3	GND
67	RESERVED	4	5.0V
66	GND	5	3.3V
65	TX LANE3-	6	3.3V
64	TX LANE3+	7	APS (1.5V)
63	GND	8	APS (1.5V)
62	TX LANE2-	9	LASI
61	TX LANE2+	10	RESET
60	GND	11	VEND SPECIFIC
59	TX LANE1-	12	TX ON/OFF
58	TX LANE1+	13	RESERVED
57	GND	14	MOD DETECT
56	TX LANE0-	15	VEND SPECIFIC
55	TX LANE0+	16	VEND SPECIFIC
54	GND	17	MDIO
53	GND	18	MDC
52	GND	19	PRTAD4
51	RX LANE3-	20	PRTAD3
50	RX LANE3+	22	PRTAD2
49	GND	21	PRTAD1
48	RX LANE2-	23	PRTAD0
47	RX LANE2+	24	VEND SPECIFIC
46	GND	25	APS SET
45	RX LANE1-	26	RESERVED
44	RX LANE1+	27	APS SENSE
43	GND	28	APS (1.5V)
42	RX LANE0-	29	APS (1.5V)
41	RX LANE0+	30	3.3V
40	GND	31	3.3V
39	RESERVED	32	5.0V
38	RESERVED	33	GND
37	GND	34	GND
36	GND	35	GND

Top of Transceiver PCB

Bottom of Transceiver PCB (as viewed through top)

Toward Bezel

Figure 6: x-mGC transceiver Electrical pad layout

1	GND		70	GND	
2	GND		69	GND	
3	GND		68	RESERVED	
4	5.0V		67	RESERVED	
5	3.3V		66	GND	
6	3.3V		65	TX LANE3-	
7	APS (1.5V)		64	TX LANE3+	
8	APS (1.5V)		63	GND	
9	LASI		62	TX LANE2-	
10	RESET		61	TX LANE2+	
11	VEND SPECIFIC		60	GND	
12	TX ON/OFF		59	TX LANE1-	
13	RESERVED		58	TX LANE1+	
14	MOD DETECT		57	GND	
15	VEND SPECIFIC		56	TX LANE0-	
16	VEND SPECIFIC		55	TX LANE0+	
17	MDIO		54	GND	
18	MDC		53	GND	
19	PRTAD4		52	GND	
20	PRTAD3		51	RX LANE3-	
22	PRTAD2		50	RX LANE3+	
21	PRTAD1		49	GND	
23	PRTAD0		48	RX LANE2-	
24	VEND SPECIFIC		47	RX LANE2+	
25	APS SET		46	GND	
26	RESERVED		45	RX LANE1-	
27	APS SENSE		44	RX LANE1+	
28	APS (1.5V)		43	GND	
29	APS (1.5V)		42	RX LANE0-	
30	3.3V		41	RX LANE0+	
31	3.3V		40	GND	
32	5.0V		39	RESERVED	
33	GND		38	RESERVED	
34	GND		37	GND	
35	GND		36	GND	
Lower Row			Upper Row		

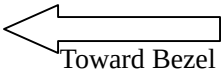


Figure 7: 10Gb host board pad layout

Pin function definitions

Pin No	Name	Dir	Function	Notes
1	GND		Electrical Ground	1
2	GND		Electrical Ground	1
3	GND		Electrical Ground	1
4	5.0V		Power	2
5	3.3V		Power	2
6	3.3V		Power	2
7	APS (1.5V)		Adaptive Power Supply	2
8	APS (1.5V)		Adaptive Power Supply	2
9	LASI		LVCMOS 1.2V Open Drain	3
10	RESET	I	LVCMOS 1.2V Open Drain	3
11	VEND SPECIFIC-signal detect		Passive	
12	TX ON/OFF			
13	RESERVED		Reserved	4
14	MOD DETECT	O	Passive	
15	VEND SPECIFIC-spare		Passive	
16	VEND SPECIFIC-spare		Passive	
17	MDIO	I/O	Management Data IO LVCMOS 1.2V Open Drain	3,4
18	MDC	I	Management Data Clock	3,4
19	PRTAD4	I	Port Address Bit 4 (Low = 0)	3
20	PRTAD3	I	Port Address Bit 3 (Low = 0)	3
21	PRTAD2	I	Port Address Bit 2 (Low = 0)	3
22	PRTAD1	I	Port Address Bit 1 (Low = 0)	3
23	PRTAD0	I	Port Address Bit 0 (Low = 0)	3
24	VEND SPECIFIC-not connected		Passive	
25	APS SET (1.5V)		Passive	
26	RESERVED		Reserved	4
27	APS SENSE		Passive Connector to a 348 ohm resistor	
28	APS (1.5V)		Adaptive Power Supply	2
29	APS (1.5V)		Adaptive Power Supply	2
30	3.3V		Power	2
31	3.3V		Power	2
32	5.0V		Power	2
33	GND		Electrical Ground	1
34	GND		Electrical Ground	1
35	GND		Electrical Ground	1

Table 6: XAUI Pin function 1

Pin No	Name	Dir	Function	Notes
36	GND		Electrical Ground	1
37	GND		Electrical Ground	1
38	RESERVED		Reserved	
39	RESERVED		Reserved	
40	GND		Electrical Ground	1
41	RX LANE0+		Module XAUI Output Lane 0+	5
42	RX LANE0-		Module XAUI Output Lane 0-	5
43	GND		Electrical Ground	1
44	RX LANE1+		Module XAUI Output Lane 1+	5
45	RX LANE1-		Module XAUI Output Lane 1-	5
46	GND		Electrical Ground	1
47	RX LANE2+		Module XAUI Output Lane 2+	5
48	RX LANE2-		Module XAUI Output Lane 2-	5
49	GND		Electrical Ground	1
50	RX LANE3+		Module XAUI Output Lane 3+	5
51	RX LANE3-		Module XAUI Output Lane 3-	5
52	GND		Electrical Ground	1
53	GND		Electrical Ground	1
54	GND		Electrical Ground	1
55	TX LANE0+		Module XAUI Input Lane 0+	5
56	TX LANE0-		Module XAUI Input Lane 0-	5
57	GND		Electrical Ground	1
58	TX LANE1+		Module XAUI Input Lane 1+	5
59	TX LANE1-		Module XAUI Input Lane 1-	5
60	GND		Electrical Ground	1
61	TX LANE2+		Module XAUI Input Lane 2+	5
62	TX LANE2-		Module XAUI Input Lane 2-	5
63	GND		Electrical Ground	1
64	TX LANE3+		Module XAUI Input Lane 3+	5
65	TX LANE3-		Module XAUI Input Lane 3-	5
66	GND		Electrical Ground	1
67	RESERVED		Reserved	
68	RESERVED		Reserved	
69	GND		Electrical Ground	1
70	GND		Electrical Ground	1

Table 7: XAUI Pin function 2

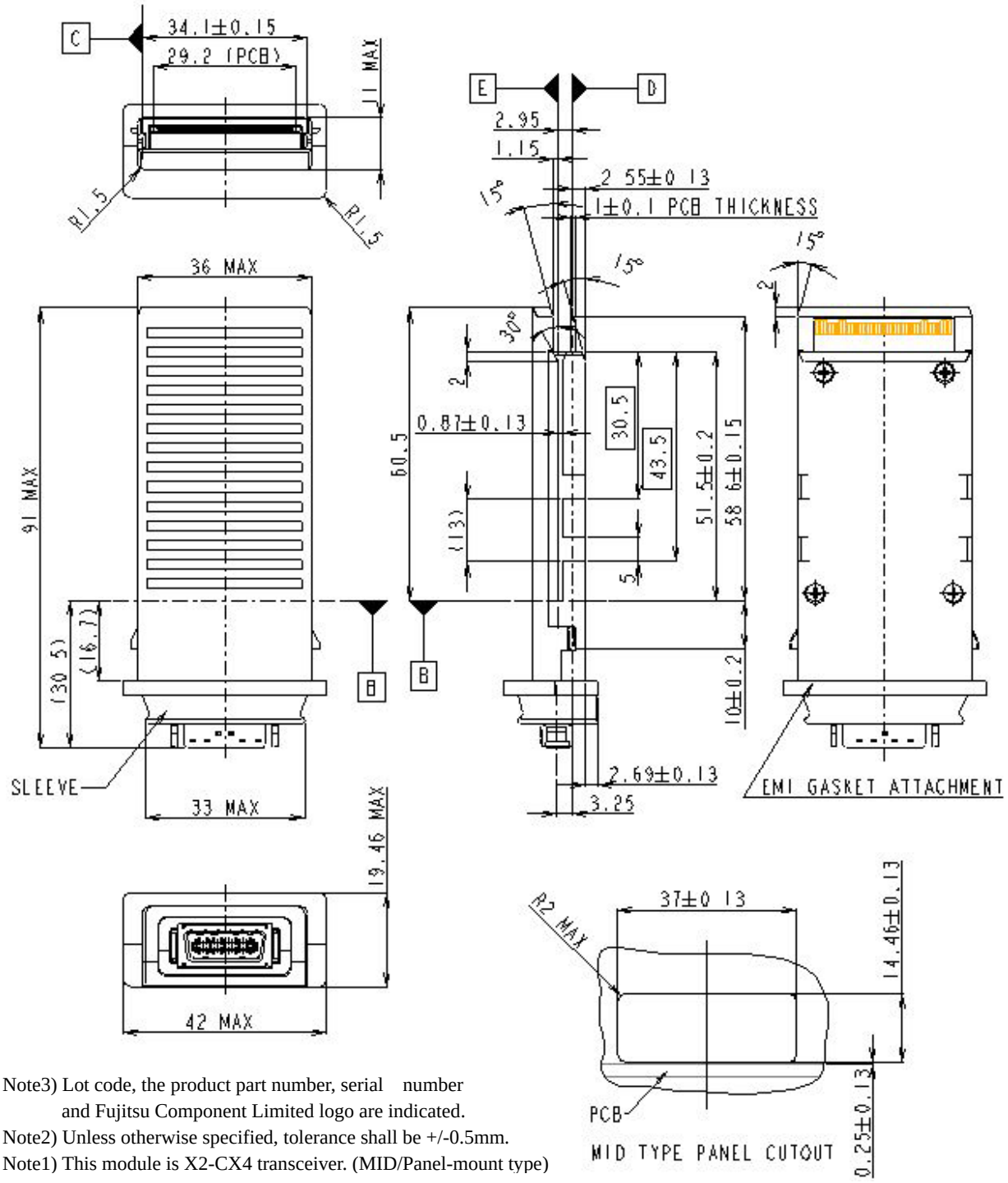
Notes:
1) Ground connections are common for TX and RX.
2) All contacts of XAUI 70 pin connector are rated at 0.5A nominal.
3) 1.2V CMOS compatible.
4) MDIO and MDC timing must comply with IEEE802.3ae, Clause 45.3
5) XAUI output characteristics should comply with IEEE802.3ae Clause 47.

Package Design

Mechanical design of x-mGC is shown as in following figure8.

It is preliminary design and subject to change without notice, please check with us for the latest design.

Datum B is physical hard stop for transceiver.
Datum C is inside edge of slot on transceiver.
Datum D is vertical center of transceiver PCB.
Datum E is top surface of slot on transceiver.



Note3) Lot code, the product part number, serial number and Fujitsu Component Limited logo are indicated.
Note2) Unless otherwise specified, tolerance shall be +/-0.5mm.
Note1) This module is X2-CX4 transceiver. (MID/Panel-mount type)

Figure 8: x-mGC schematic drawing