CMOS Image Sensor
with Image Signal Processing

HV7121GP

Preliminary
V1.0

Revision History

Revision	Issue Date	Comments
0.5	January 30, 2002	HV7121GP V0.5 Preliminary is released
1.0	April 10, 2002	HV7121GP V1.0 Preliminary is released

Disclaimer

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Contents

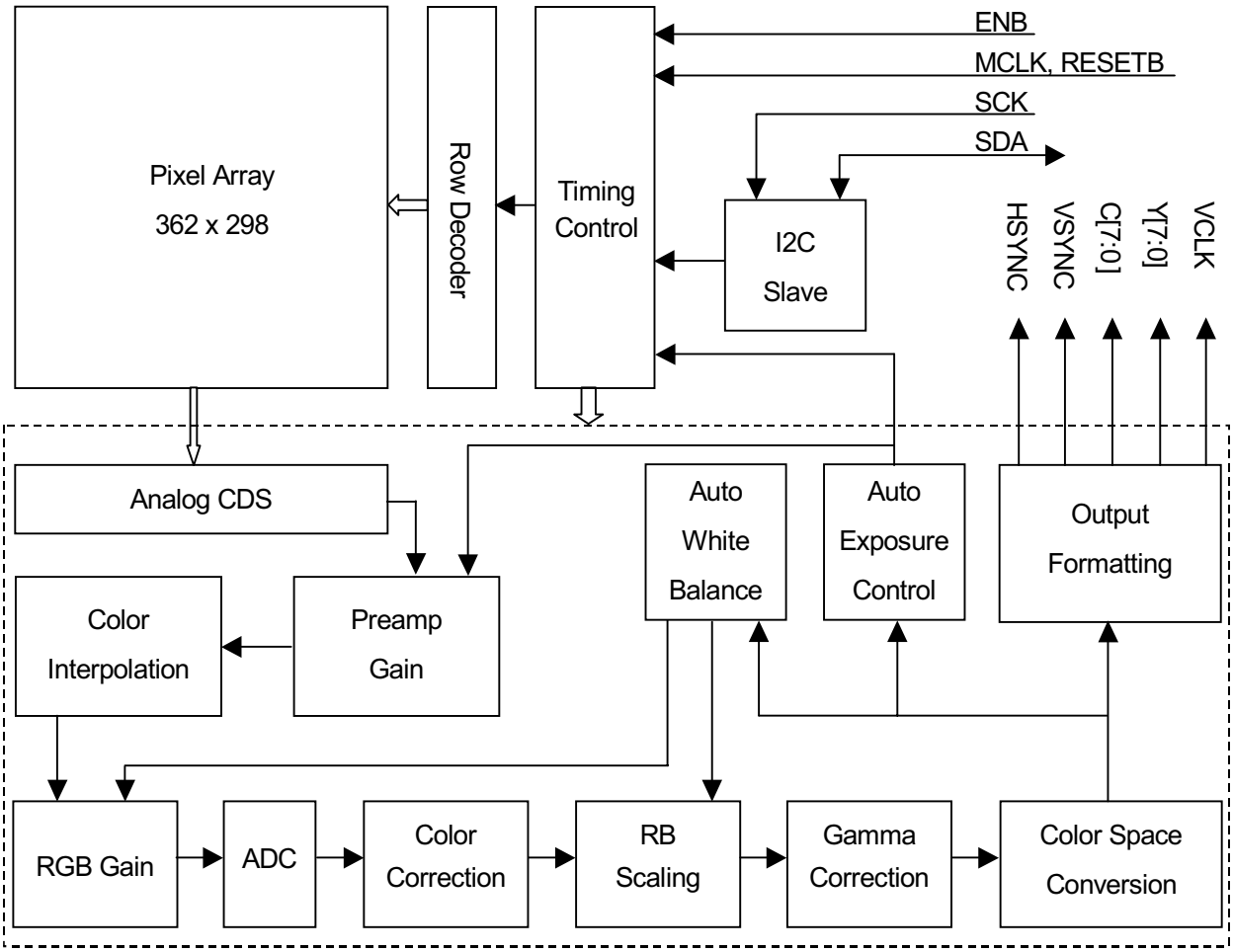
General Description

HV7121GP is a highly integrated single chip CMOS color image sensor implemented by proprietary Hynix 0.35um CMOS sensor process realizing high sensitivity and wide dynamic range. Total pixel array size is 362x298. Each active pixel is composed of 4 transistors, it has a micro-lens to enhance sensitivity and converts photon energy to analog pixel voltage. On-chip 8bit Analog to Digital Converter(ADC) is configured to digitize analog pixel voltage, and on-chip Correlated Double Sampling(CDS) scheme reduces Fixed Pattern Noise(FPN) dramatically. General image processing functions such as color interpolation, color correction, gamma correction, color space conversion, auto exposure, and auto white balance are implemented to diversify its applications, various output formats are supported for the sensor to easily interface with different video codec chips. The integration of sensor function and image processing functions make HV7121GP especially very suitable for mobile imaging systems such as IMT-2000 phone's video part that requires very low power and system compactness.

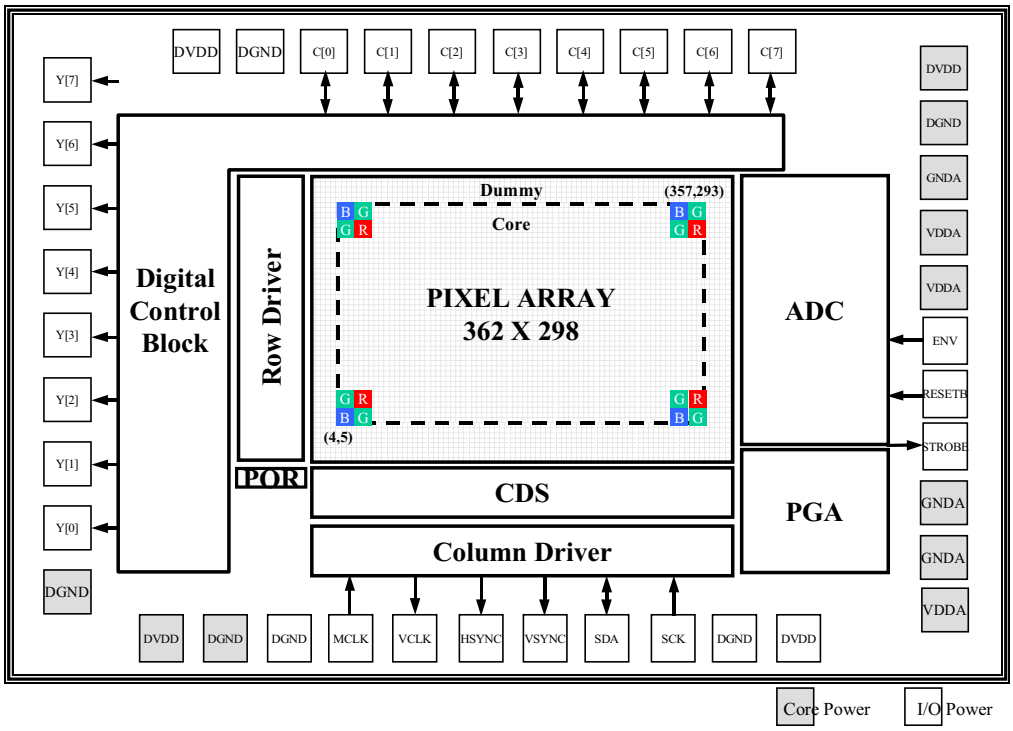
Features

- 1/7 inch optical format
- Active pixel resolution: 354x289
- 5.6um x 5.6um active square pixel
- Micro-lens for high sensitivity
- RGB mosaic color filter array
- On-chip 8 bit ADC
- Correlated double sampling for reduction of Fixed Pattern Noise
- Gamma correction by programmable piecewise linear approximation
- Color correction by programmable 3x3 matrix operation
- Color space conversion from RGB to YCbCr
- Various output formats : YCbCr 4:2:2, YCbCr 4:4:4, RGB 4:4:4, Bayer
- 8bit/16bit Data Bus Mode
- Automatic Exposure Control / Automatic White Balance Control
- Low Power Consumption / Power down mode / Power sleep mode
- Operation Voltage Range : 2.6V ~ 3.0V, Operation Temperature : -10 ~ +50 degrees Celsius
- Package Types : CLCC 48 PIN, COB(Chip-on-Board), COF(Chip-on-Flex)
- Programmable frame rate up to 30 frame/sec at 24Mhz master clock (CIF)
- Multiple video mode : CIF(352X288), SIF(320X240), QCIF(176X144), QSIF(160X120), Sub-Sample QCIF(176X144), Sub-Sample QSIF(160X120)
- Programmable video window
- Controllable full function through standard IIC bus
- Strobe control signal generation

Block Diagram



Chip Layout Information



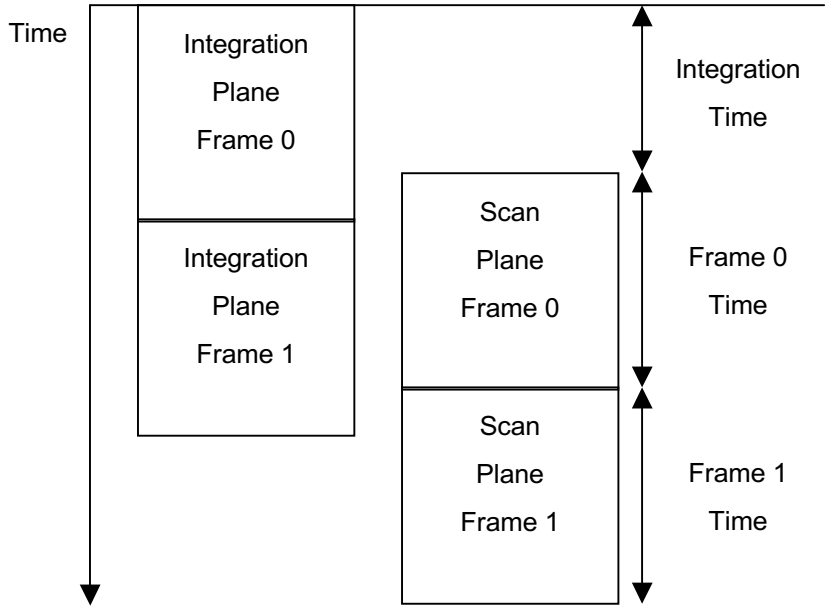
Functional Description

Pixel Architecture

Pixel architecture is a 4-transistor NMOS pixel design. The additional use of a dedicated transfer transistor in the architecture reduces most of reset level noise so that fixed pattern noise is not visible. Furthermore, micro-lens is placed upon each pixel in order to increase fill factor so that high pixel sensitivity is achieved.

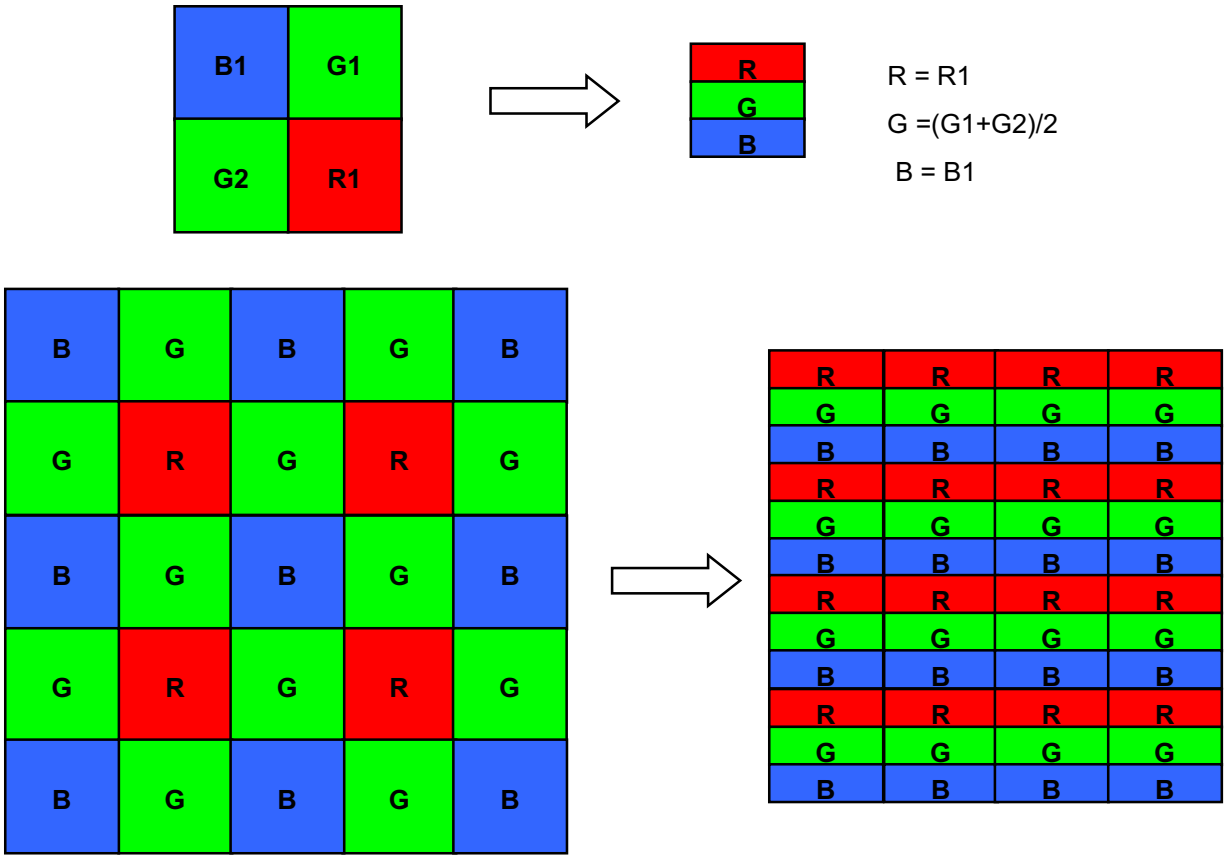
Sensor Imaging Operation

Imaging operation is implemented by the offset mechanism of integration domain and scan domain(rolling shutter scheme). First integration plane is initiated, and after the programmed integration time is elapsed, scan plane is initiated, then image data start being produced.



Color Interpolation

2x2 linear color interpolation is used to interpolate missing R, G, or B for Bayer image data from pixel array. Color interpolation is done by moving 2x2-interpolation window.



Bayer RGB Color Pattern(5X5)

Color Interpolation Pattern(4X4)

Color Correction

The color spread effect mainly caused by color filter characteristics. The effect is compensated by 3x3-color matrix operation. Nine registers for matrix coefficients are used in color matrix operation to get the optimal pure color reproduction. The relationship between input color and color-corrected color is defined as below formula.

$$\begin{bmatrix} R' \\ G' \\ B' \end{bmatrix} = \begin{bmatrix} CMA11 & CMA12 & CMA13 \\ CMA21 & CMA22 & CMA23 \\ CMA31 & CMA32 & CMA33 \end{bmatrix} \bullet \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

Where R, G, and B : Sensor color output.

R', G', and B' : Color-corrected output.

Color matrix coefficients are programmable from –127/64 to 127/64. Programming register value for intended color matrix coefficients should be resolved by the following equations.

For positive values, CMAxx = Integer(Real Coefficient Value x 64);

For negative values, CMAxx = Two's Complement(Integer(Real Coefficient Value x 64));

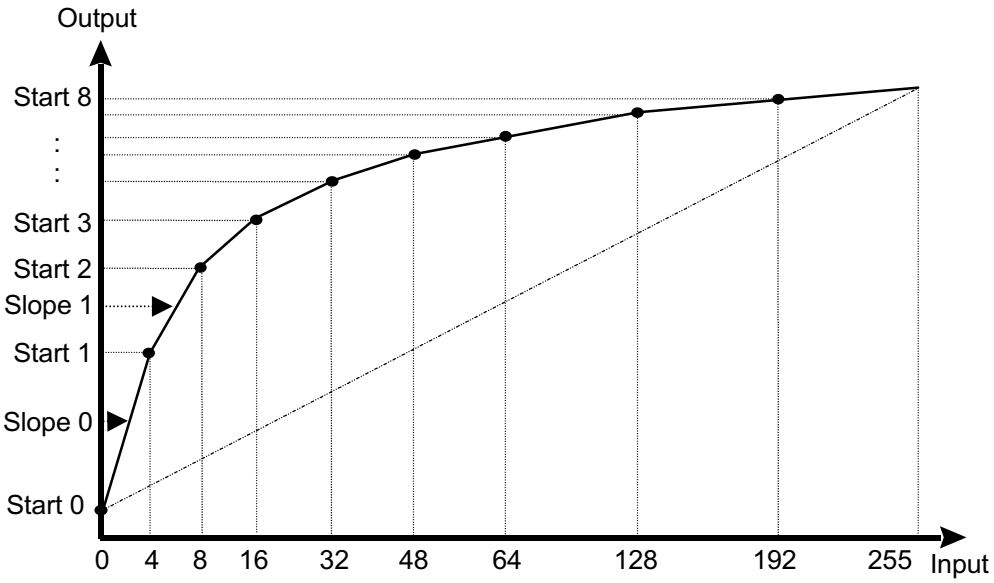
Real Coefficient Value : From –127/64 to 127/64.

RB Scaling

R and B values are scaled by this block that receives scaling values from Auto White Balance block. Scaling resolution is 1/64 and value range is 0.1 ~ 3.9.

Gamma Correction

Piecewise linear gamma approximation method is implemented. Nine piece linear segments are supported and user-programmable.



Gamma Control

$$Slope_N = \frac{Start_{N+1} - Start_N}{In_{N+1} - In_N}$$

$$Output = Slope_N (Input - In_N) + Start_N$$

Where In_N(Fixed Value) : 0, 4, 8, 16, 32, 48, 64, 128, and 192, 255.

Gamma Slope Registers are programmed as the integer value of real slope multiplied by 8 or 16. For Gamma Slope 0 register, multiplier 8 is used for the program value calculation, and for others multiplier 16 is used.

Color Space Conversion

CCIR-601 YCbCr color space conversion is implemented.

< Conversion Equation >

$$Y = \frac{77R + 150G + 29B}{256} \qquad \text{Range: 16 ~ 235}$$

$$Cb = \frac{-44R - 87G + 131B}{256} + 128 \qquad \text{Range: 16 ~ 240}$$

$$Cr = \frac{131R - 110G - 21B}{256} + 128 \qquad \text{Range: 16 ~ 240}$$

< Reverse Conversion >

$$R = Y + 1.371(Cr - 128)$$
$$G = Y - 0.698(Cr - 128) - 0.336(Cb - 128)$$
$$B = Y + 1.732(Cb - 128)$$

In the above equations, R, G, and B are gamma-corrected values.

Output Formatting

The output formats such as RGB 4:4:4, YCbCr 4:4:4, and YCbCr 4:2:2 are supported. Possible output bus widths are 8 bits and 16bits, and the sequence of Cb and Cr are programmable.

Auto Exposure

Y mean value is continuously calculated every frame, then the integration time or preamp gain value are increased or decreased according to the displacement between current frame Y mean value and target Y mean value.

Auto White Balance Control

Cb/Cr frame mean value is calculated every frame and according to Cb/Cr frame mean values' displacement from Cb/Cr white target point, R/B scaling values and R/B gain for R/B data are resolved.

Register Description

Register	Symbol	Address (Hex)	Default (Hex)	Description
Device ID	DEVID	00	30	Product Identification, Revision Number
Sensor Control A	SCTRA	01	13	Operation Mode, X/Y Flip, Video Mode
Sensor Control B	SCTRB	02	00	Clock Division, Power Sleep, and SYNC Control, VSYNC Unit
Sensor Control C	SCTRC	03	00	C output control, Clock Inversion, Strobe Function
Half-Window Height	WNHEIGHT	0d	30	Half Window Height for Windowing
Half-Window Width	WNWIDTH	0f	40	Half Window Width for Windowing
HBLANK Time High	HBLANKH	10	00	HBLANK Time [15:8]
HBLANK Time Lower	HBLANKL	11	64	HBLANK Time [7:0]
VBLANK Time High	VBLANKH	12	00	VBLANK Time [15:8]
VBLANK Time Lower	VBLANKL	13	05	VBLANK Time [7:0]
Red Color Gain	RCG	14	10	Gain for Red Pixel Output
Green Color Gain	GCG	15	10	Gain for Green Pixel Output
Blue Color Gain	BCG	16	10	Gain for Blue Pixel Output
Preamp Gain	PREAMP	17	10	Preamp Gain for Pixel Output
Preamp Gain Min	PREMIN	18	00	Preamp Gain Min Value for AE
Preamp Gain Max	PREMAX	19	2f	Preamp Gain Max Value for AE
Preamp Gain Normal	PRENOM	1a	10	Preamp Gain Normal Value for AE
ASP Bias	ASPBIAS	1b	33	Amp Bias, Pixel Bias
Reset Clamp	RSTCLMP	1c	07	Reset Level Clamping Value
ADC Bias	ADCBIAS	20	00	ADC Bias
ADC Offset	ADCOFFSET	21	00	ADC Offset
ISP Function Enable	ISPFEN	30	0f	Image Processing Functions
Output Format	OUTFMT	31	39	Data Output Format.
Color Matrix Coefficient 11	CMA11	34	45	Color Matrix Coefficient 11
Color Matrix Coefficient 12	CMA12	35	f6	Color Matrix Coefficient 12
Color Matrix Coefficient 13	CMA13	36	04	Color Matrix Coefficient 13
Color Matrix Coefficient 21	CMA21	37	f8	Color Matrix Coefficient 21
Color Matrix Coefficient 22	CMA22	38	5d	Color Matrix Coefficient 22
Color Matrix Coefficient 23	CMA23	39	eb	Color Matrix Coefficient 23
Color Matrix Coefficient 31	CMA31	3a	03	Color Matrix Coefficient 31
Color Matrix Coefficient 32	CMA32	3b	ed	Color Matrix Coefficient 32
Color Matrix Coefficient 33	CMA33	3c	51	Color Matrix Coefficient 33
Gamma Segment Point 0	GMAP0	40	00	Start Point for Gamma Line Segment 0
Gamma Segment Point 1	GMAP1	42	18	Start Point for Gamma Line Segment 1
Gamma Segment Point 2	GMAP2	43	2c	Start Point for Gamma Line Segment 2
Gamma Segment Point 3	GMAP3	44	47	Start Point for Gamma Line Segment 3
Gamma Segment Point 4	GMAP4	45	6c	Start Point for Gamma Line Segment 4
Gamma Segment Point 5	GMAP5	46	88	Start Point for Gamma Line Segment 5
Gamma Segment Point 6	GMAP6	47	a0	Start Point for Gamma Line Segment 6
Gamma Segment Point 7	GMAP7	48	e0	Start Point for Gamma Line Segment 7
Gamma Segment Point 8	GMAP8	49	f5	Start Point for Gamma Line Segment 8
Gamma Segment Slope 0	GMAS0	50	30	Slope Value for Gamma Line Segment 0
Gamma Segment Slope 1	GMAS1	52	50	Slope Value for Gamma Line Segment 1
Gamma Segment Slope 2	GMAS2	53	36	Slope Value for Gamma Line Segment 2
Gamma Segment Slope 3	GMAS3	54	25	Slope Value for Gamma Line Segment 3
Gamma Segment Slope 4	GMAS4	55	1c	Slope Value for Gamma Line Segment 4
Gamma Segment Slope 5	GMAS5	56	18	Slope Value for Gamma Line Segment 5
Gamma Segment Slope 6	GMAS6	57	10	Slope Value for Gamma Line Segment 6
Gamma Segment Slope 7	GMAS7	58	05	Slope Value for Gamma Line Segment 7
Gamma Segment Slope 8	GMAS8	59	03	Slope Value for Gamma Line Segment 8
AE Mode 1	AEM1	60	6b	Auto Exposure Mode Selection 1
AE Mode 2	AEM2	61	02	Auto Exposure Mode Selection 2
Integration Time High	INTH	63	02	Integration Time [23:16]
Integration Time Middle	INTM	64	71	Integration Time [15:8]
Integration Time Low	INTL	65	00	Integration Time [7:0]

AE Target	AETGT	66	70	Target Luminance(Y) Value
AE Lock Boundary	AELBND	67	02	Boundary Value from Target Luminance to determine Lock state for AE
AE UnLock Boundary	AEUBND	68	2a	Boundary Value from Target Luminance to determine UnLock0 state for AE
AE Speed Boundary	AESBND	69	30	Boundary Value from Target Luminance to determine UnLock1 state and UnLock2 state for AE
AE Anti-Banding Integration Step High	AEANTH	6a	00	Anti-Banding Integration Increment Step Unit [19:16]
AE Anti-Banding Integration Step Middle	AEANTM	6b	9c	Anti-Banding Integration Increment Step Unit [15:8]
AE Anti-Banding Integration Step Low	AEANTL	6c	40	Anti-Banding Integration Increment Step Unit [7:0]
AE Integration Limit High	AELMH	6d	07	Integration Time Limit [23:16]
AE Integration Limit Middle	AELMM	6e	a1	Integration Time Limit [15:8]
AE Integration Limit Low	AELML	6f	20	Integration Time Limit [7:0]
AWB Mode	AWBM	70	01	AWB Mode Selection
Cb Target	CBTGT	73	80	Target Cb Value
Cr Target	CRTGT	74	80	Target Cr Value
AWB Lock Boundary	AWBLB	75	02	Boundary Value from Target Cb/Cr to determine Lock state for AWB
AWB Unlock Boundary	AWBULB	76	06	Boundary Value from Target Cb/Cr to determine UnLock0 state for AWB
AWB White Pixel Boundary	AWBWPB	77	30	Boundary Value from Target Cb/Cr to determine UnLock1 state and UnLock2 state for AWB
AWB B Scaling	AWBSCLB	78	40	B Scaling Value in RB Scaling Block
AWB R Scaling	AWBSCLR	79	40	R Scaling Value in RB Scaling Block
AE/AWB Status	AEWBST	7a	RO	AE/AWB Lock Status
Y Frame Mean	YFMEAN	7b	RO	Y Frame Mean Value
Cb Frame Mean	CBFMEAN	7c	RO	Cb Frame Mean Value
Cr Frame Mean	CRFMEAN	7d	RO	Cr Frame Mean Value
AWB Luminance Limit	AWBYLMT	8a	00	Luminance Limit Value for AWB
AWB Chrominance Limit	AWBCLMT	8b	ff	Chrominance Limit Value for AWB
AWB Valid Pixel Number Threshold	AWBPXLTH	8c	02	Valid Pixel Number Threshold for AWB
AWB Valid Pixel Number Count High	AWBPXLH	8d	RO	Valid Pixel Number Count High Byte
AWB Valid Pixel Number Count Low	AWBPXLL	8e	RO	Valid Pixel Number Count Low Byte
Dark Bad Integration Time High	DPCINTH	91	06	Integration Time High Byte where filtering operation gets active when dark bad pixel filtering mode is enabled
Dark Bad Integration Time High	DPCINTM	92	1a	Integration Time High Byte where filtering operation gets active when dark bad pixel filtering mode is enabled
Dark Bad Integration Time High	DPCINTL	93	80	Integration Time High Byte where filtering operation gets active when dark bad pixel filtering mode is enabled
Dark Bad Green Threshold	DPCGTH	94	0a	Neighbor-differential threshold value that specify Green dark bad pixel
Dark Bad Red Threshold	DPCRTH	95	0a	Neighbor-differential threshold value that specify Red dark bad pixel
Dark Bad Blue Threshold	DPCBTH	96	0a	Neighbor-differential threshold value that specify Blue dark bad pixel

* RO : Read Only.

Device ID [DEVID : 00h : 30h]

7	6	5	4	3	2	1	0
Product ID				Revision Number			
0	0	1	1	0	0	0	0

High nibble represents Sensor Array Resolution, Low Nibble represents Revision Number.

Sensor Control A [SCTRA : 01h : 13h]

7	6	5	4	3	2	1	0
Reserved			X-Flip	Y-Flip	Video Mode		
0	0	0	1	0	0	1	1

X-Flip

0 : Normal.

1 : Image is horizontally flipped.

Y-Flip

0 : Normal.

1 : Image is vertically flipped.

Video Mode

000 : QSIF(160x120).

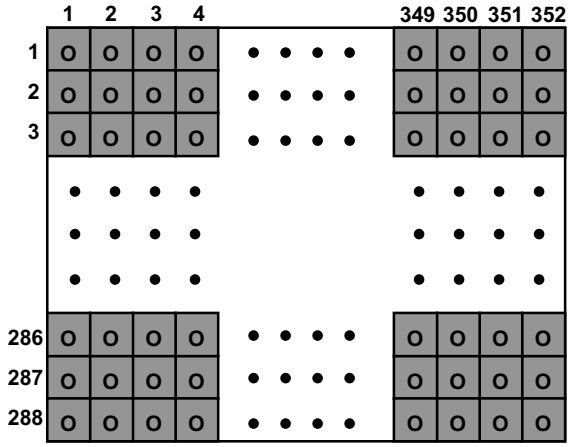
001 : QCIF(176x144).

010 : SIF(320x240).

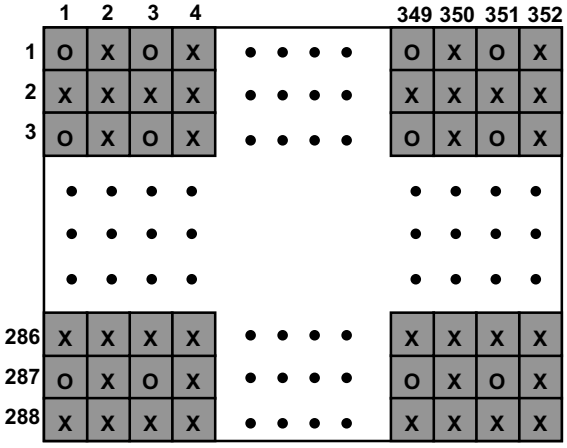
011 : CIF(352x288).

100 : Sub-Sample QSIF(160x120).

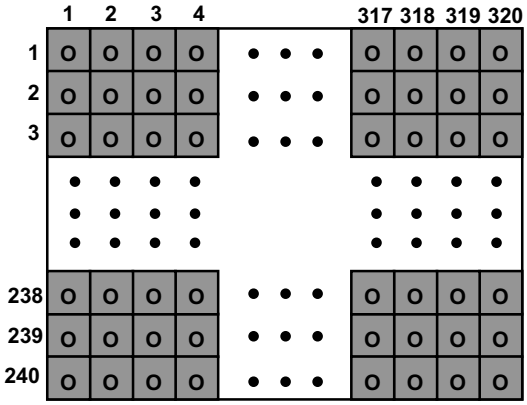
101 : Sub-Sample QCIF(176x144).



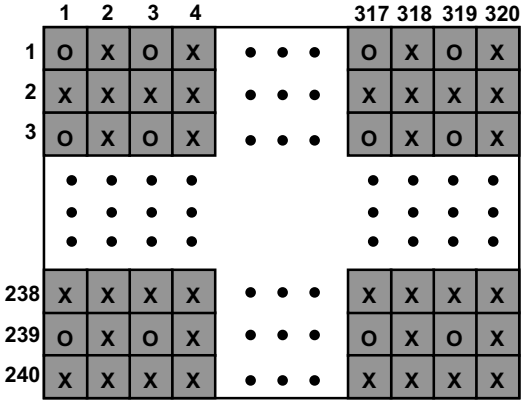
CIF (352 X 288)



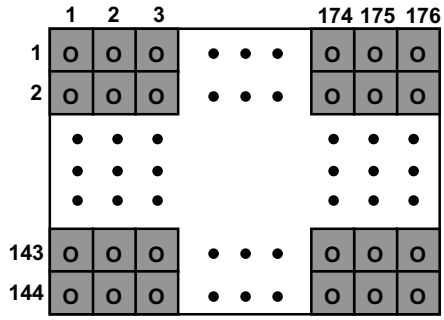
Sub-Sample QCIF (176 X 144)



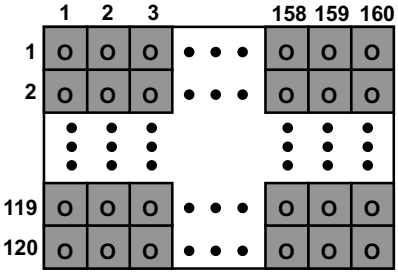
SIF (320 X 240)



Sub-Sample QSIF (160 X 120)



QCIF (176 X 144)



QSIF (160 X 120)

o Valid Pixel Data x Invalid Pixel Data

Sensor Control B [SCTRB : 02h : 00h]

7	6	5	4	3	2	1	0
VSYNC Unit	HSYNC in VSYNC	Reserved	Power Down	HSYNC Polarity	VSYNC Polarity	Clock Division	
0	0	0	0	0	0	0	0

< Clock Acronym Definition >

MCF(Master Clock Frequency) : MCLK	DCF(Divided Clock Frequency) : MCF/Clock Division
SCF(Sensor Clock Frequency) : DCF/6	ICF(Image Processing Clock Frequency) : SCF for CIF/SIF/QCIF/QSIF : SCF/2 for Sub-Sample QCIF/QSIF
VCF(Video Clock Frequency) : ICF for 16bit 422 : ICF*2 for 8bit 422 / 16bit 444	LCF(Line Clock Frequency) : SCF/ (HBLANK Time + Video Width Time)

SCP(Sensor Clock Period) = 1/SCF, LCP(Line Clock Period) = 1/LCF

< Video Width and Height>

Video Mode	Width		Height	
	Time	Number of Pixel in Line	Time	Number of Line
CIF	352SCP	352EA	288LCP	288EA
SIF	320SCP	320EA	240LCP	240EA
QCIF	176SCP	176EA	144LCP	144EA
QSIF	160SCP	160EA	120LCP	120EA
Sub-Sample QCIF	352SCP	176EA	288LCP	144EA
Sub-Sample QSIF	320SCP	160EA	240LCP	120EA

Example) MCF is 24Mhz, Clock Division is 1, Video Mode is CIF, Video Width Time = 352 ,

Output format is YCbCr 8bit 422 and HBLANK Time is 100.

DCF = 24Mhz / 1 =24Mhz, SCF = 24Mhz / 6 = 4Mhz, ICF = 4Mhz, VCF = 8Mhz,

LCF = 4Mhz/(100 + 352) = 4/452 MHz

VSYNC Unit

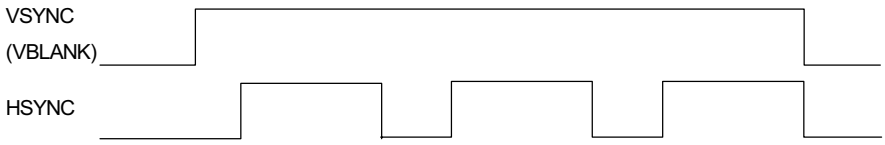
0 : Line unit. Valid duration of VSYNC is calculated by VBLANK Time * LCP.

1 : Pixel unit. Valid duration of VSYNC is calculated by VBLANK Time * SCP.

HSYNC in VSYNC

0 : There are no valid HSYNC signals during valid VSYNC signal.

1 : There are valid HSYNC signals during valid VSYNC signal. Number of valid HSYNC is same as number of VBLANK register when VSYNC unit is line unit. Do not use this mode when VSYNC unit is pixel unit



Power Sleep

0 : Software power sleep mode off.

1 : Software power sleep mode on.

HSYNC Polarity

0 : HSYNC signal is valid High.

1 : HSYNC signal is valid Low.

VSYNC Polarity

0 : VSYNC signal is valid High.

1 : VSYNC signal is valid Low.

Clock Division

00 : DCF=MCF, 01: DCF=MCF/2, 10: DCF=MCF/4, 11: DCF=MCF/8

Sensor Control C [SCTRC : 03h : 00h]

7	6	5	4	3	2	1	0
Reserved	C[7:0] pad output low	C[7:0] pad output high	Reserved		Video Clk Inversion	Reserved	Strobe
0	0	0	0	0	0	0	0

C[7:0] pad output low

When this bit and 8bit-output mode are enabled, C[C:0] pads go into zero-driving state. When this bit is disabled and 8bit-output mode is enabled, C[C:0] pads go into tri-state.

C[7:0] pad output high

When this bit and 8bit-output mode are enabled, C[C:0] pads go into high-driving state. When this bit is disabled and 8bit-output mode is enabled, C[C:0] pads go into tri-state.

Video Clk Inversion

This bit changes the polarity of Video Clock.

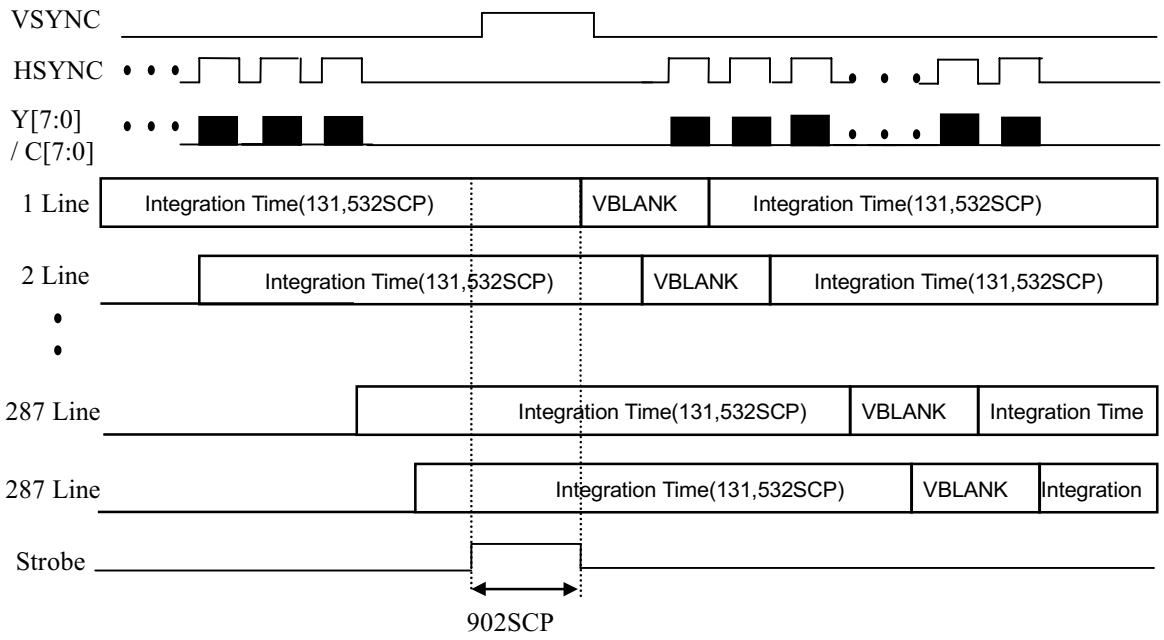
Strobe

Though sensor has enough integration time to capture image, sensor can't obtain good image quality in dark environment. For this situation, sensor can generate strobe signal for driving external strobe circuit. The strobe output is active high when integration time is over than core frame time((Video Height Time + 1) X (Video Width Time + HBLANK)). Because sensor uses progressive exposure method, strobe signal should cover all line(all pixels). The following figure shows that the relationships between strobe signal and exposure time. In this example picture, we set Window

Width = 352, Window Height = 288, Integration Time = 131,532SCP, HBLANK = 100SCP, and VBLANK = 2LCP. Then Strobe Signal duration is 902SCP(131,532-289*452).

0: Disable

1: Enable



Half Window Height [WNHEIGHT : 0dh : 30h]

7	6	5	4	3	2	1	0
Half Window Height							
0	0	1	1	0	0	0	0

Window Height is double of half window height when programmable windowing(7bit of 31H) mode is enabled. However, this register means window height when video mode is Sub-Sample QCIF/QSIF. This value should be even number (multiple integer of 4 for Sub-Sample QCIF/QSIF) and under the maximum values for each video mode.

Video Mode	Maximum Value of Half Window Height register
CIF/Sub-Sample QCIF	144
SIF/Sub-Sample QSIF	120
QCIF	72
QSIF	60

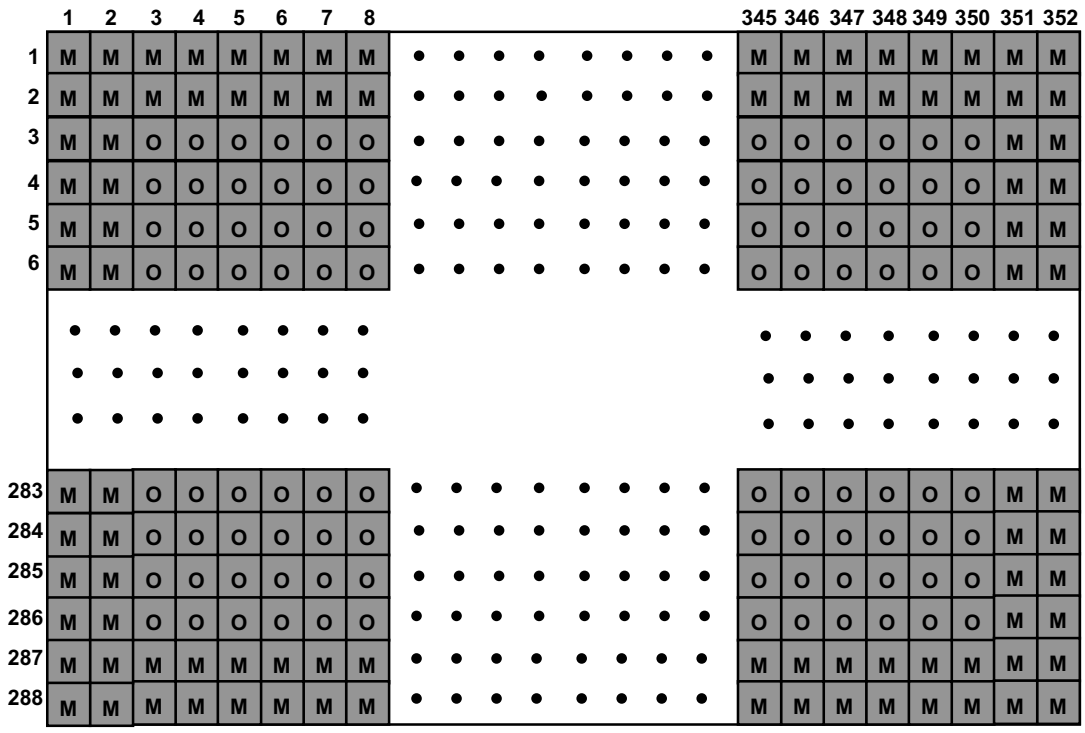
Half Window Width [WNWIDTH : 0fh : 40h]

7	6	5	4	3	2	1	0
Half Window Width							
0	1	0	0	0	0	0	0

Window Width is double of half window width when programmable window mode(Refer to 7bit of 31H register) is enabled. However, this register means window width when video mode is Sub-Sample QCIF/QSIF. This value should be even number(multiple integer of 4 for Sub-Sample QCIF/QSIF) and under the maximum values for each video mode.

Video Mode	Maximum Value of Half Window Width register
CIF/Sub-Sample QCIF	176
SIF/Sub-Sample QSIF	160
QCIF	88
QSIF	80

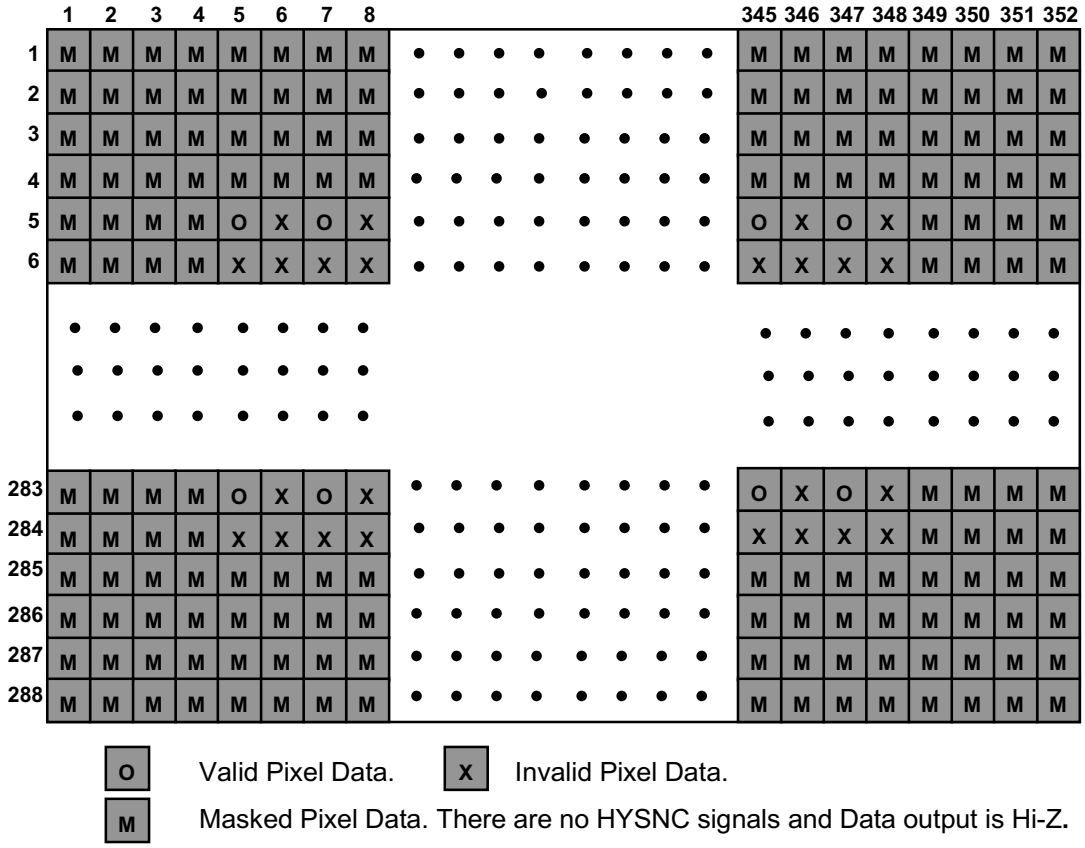
Following Figure shows windowing image data when programmable window is enabled and Half window width = 174, Half window height = 142 and CIF mode.



O Valid Pixel Data.

M Masked Pixel Data. There are no HYSNC signals and Data output is Hi-Z.

Following Figure shows windowing image data when programmable window is enabled and Half window width = 172, Half window height = 140 and Sub-Sample QCIF mode.



O Valid Pixel Data. X Invalid Pixel Data.

M Masked Pixel Data. There are no HYSNC signals and Data output is Hi-Z.

Horizontal Blanking Time High [HBLANKH : 10h : 00h]

7	6	5	4	3	2	1	0
HBLANK Time[15:8]							
0	0	0	0	0	0	0	0

Horizontal Blanking Time Low [HBLANKL : 11h : 64h]

7	6	5	4	3	2	1	0
HBLANK Time[7:0]							
0	1	1	0	0	1	0	0

Horizontal Blanking(HBLANK) Time register defines data blank time between current line and next line by using Sensor Clock Frequency Unit(SCF), and should be larger than 100(64h) and even number. Default HBLANK Time is HBLANK * SCP(100/4Mhz = 25us) where MCF is 24Mhz, Clock Divide is 1, and SCF = 4Mhz.

Vertical Blanking Time High [VBLANKH : 12h : 00h]

7	6	5	4	3	2	1	0
VBLANK Time[15:8]							
0	0	0	0	0	0	0	0

Vertical Blanking Time Low [VBLANKL : 13h : 05h]

7	6	5	4	3	2	1	0
VBLANK Time[7:0]							
0	0	0	0	0	1	0	1

Vertical Blanking(VBLANK) Time register defines valid duration of VSYNC output which indicates frame boundary between continuous frames by using VSYNC Unit(Refer to 7bit of 02H register) . Because default of VSYNC unit is line unit, valid duration of VSYNC is VBLANK Time * LCP. If VSYNC Unit is Pixel Unit, valid duration of VSYNC is VBLANK Time * SCP. However, VBLANK Time register should be larger than 452 and even number at Pixel Unit. Default VSYNC time is 5 * 452/(4Mhz) where MCF is 24Mhz, Clock Division is 1, Video Mode is CIF, HBLANK Time is 100 and LCF = 4/452 MHz. For VSYNC-HSYNC timing relation in the frame transition, please refer to Frame Timing section.

Red Color Gain [RCG : 14h : 10h]

7	6	5	4	3	2	1	0
Reserved		R Color Gain					
0	0	0	1	0	0	0	0

Green Color Gain [RCG : 15h : 10h]

7	6	5	4	3	2	1	0
Reserved		G Color Gain					
0	0	0	1	0	0	0	0

Blue Color Gain [RCG : 16h : 10h]

7	6	5	4	3	2	1	0
Reserved		B Color Gain					
0	0	0	1	0	0	0	0

There are three color gain registers for R, G, B pixels, respectively.
R, G, B color gain are used to amplify R, G, B channel. Programmable range is from 0.5X ~ 2.5X. Default gain is 1X.

Gain = 0.5 + B<5:0>/32

Preamp Gain [PREAMP : 17h : 10h]

7	6	5	4	3	2	1	0
Preamp Gain							
0	0	0	1	0	0	0	0

Preamp Gain is common gain for R, G and B channel and used for auto exposure control. Programmable range is from 0.5X ~ 16.5X. Default gain is 1.5X.

Gain = 0.5 + B<7:0>/16

Preamp Gain Min [PREMIN : 18h : 00h]

7	6	5	4	3	2	1	0
Preamp Gain Min							
0	0	0	0	0	0	0	0

Preamp Gain Min is minimum value of preamp gain when sensor adjusts pre-amplifier gain for auto exposure control. Programmable range is same as preamp gain. Default value is 0.5X.

Preamp Gain Max [PREMAX : 19h : 2fh]

7	6	5	4	3	2	1	0
Preamp Gain Max							
0	0	1	0	1	1	1	1

Preamp Gain Max is maximum value of preamp gain when sensor adjusts preamp gain for auto exposure control. Programmable range is same as preamp gain. Default value is 3.43X.

Preamp Gain Normal [PRENOM : 1ah : 10h]

7	6	5	4	3	2	1	0
Preamp Gain Normal							
0	0	0	1	0	0	0	0

Preamp Gain Normal is reference value of preamp gain when sensor adjusts preamp gain for auto exposure control. First, sensor controls integration time before adjusting preamp gain for auto exposure control. After integration time is changed to the minimum or maximum value, sensor adjusts preamp gain from this register value. Refer to figure of AE mode1 register(60H).

Programmable range is same as preamp gain. Default value is 1.5X.

ASP Bias [ASPBIAS : 1bh : 33h]

7	6	5	4	3	2	1	0
Reserved		Amp Bias		Reserved		Pixel Bias	
0	0	1	1	0	0	1	1

Amp Bias[1:0]

Amp Bias controls the amount of current in internal amplifier bias circuit to amplify pixel output effectively. The larger register value increases the amount of current.

Pixel Bias[1:0]

Pixel Bias controls the amount of current in internal pixel bias circuit to amplify pixel output effectively. The larger register value increases the amount of current.

Reset Level Clamp [RSTCLMP : 1ch : 07h]

7	6	5	4	3	2	1	0
Reserved				Reset Level Clamp			
0	0	0	0	0	1	1	1

Because extremely bright image like sun affects reset data voltage of pixel to lower, bright image is captured as black image in image sensor regardless of correlated double sampling. To solve this extraordinary phenomenon, we adopt the method to clamp reset data voltage. Reset Level Clamp controls the reset data voltage to prevent inversion of extremely bright image. The larger register value clamps the reset data level at highest voltage level. Default value is 7 to clamp the reset data level at appropriate voltage level.

ADC Bias [ADCBIAS : 20h : 00h]

7	6	5	4	3	2	1	0
Reserved		ADC Overflow	ADC Underflow	ADC Bias			
0	0	Read Only	Read Only	0	0	0	0

ADC Overflow

This bit is high when ADC is overflow output.

ADC Underflow

This bit is high when ADC is underflow output.

ADC Bias[3:0]

ADC Bias controls the amount of current in ADC bias circuit to operate ADC effectively. The larger register value increases the amount of current.

ADC Offset [ADCOFFS : 21h : 00h]

7	6	5	4	3	2	1	0
Reserved		ADC Offset					
0	0	0	0	0	0	0	0

ADC Offset<4:0> controls the amount of dc-offset voltage in the ADC input to compensate dark signal effectively. ADC Offset<5> is polarity bit.

ADC Offset<5> = 0 : Add ADC Offset<4:0> (dc-offset value) to the ADC input.

ADC Offset<5> = 1 : Substract ADC Offset<4:0> (dc-offset value) to the ADC input.

ISP Function Enable [ISPFEN : 30h : 0fh]

7	6	5	4	3	2	1	0
Reserved		Dark Bad Pixel Concealment	Analog RB Scaling	Digital RB Scaling	Color Space Conversion	Gamma Correction	Color Correction
0	0	0	0	1	1	1	1

Dark Bad Pixel Concealment

0 : Disable

1 : Dark Bad Pixel Concealment is performed when integration time(63-65H) exceeds Dark Bad Integration Time(91-93H)

Analog RB Scaling

0 : Disable

1 : This bit enables sensor to control Analog R, B Gain amplifier for Auto White Balance

Digital RB Scaling

0 : Disable

1 : This bit enables sensor to scale Digital R, B values before gamma correction for Auto White Balance

Color Space Conversion

0 : RGB Output

1 : YCbCr Output

Gamma Correction

0 : Disable. Linear Output

1 : Enable. Gamma Corrected Output

Color Correction

0 : Disable

1 : Enable

Output Formatting

The output formats such as YCbCr 4:4:4, YCbCr 4:2:2, RGB4:4:4 and Bayer are supported. Possible output bus widths are 8 bits and 16bits, and the sequence of Cb and Cr are programmable.

Output Format [OUTFMT : 31h : 39h]

7	6	5	4	3	2	1	0
Programmable Window	False Color Reduction Filter	Cb First	Y First	8-bit Output	Bayer Output	YCbCr 4:4:4	YCbCr 4:2:2
0	0	1	1	1	0	0	1

Programmable Window

0 : User can't program image size but select Video Mode such as CIF/SIF/QCIF/QSIF/Sub-Sample CIF/SIF. (Refer to Video Mode and Image Size in 01H register)

1 : User can adjust window of image size by programming Half Window Height and Half Window Width. (Refer to 0DH and 0FH register)

False Color Reduction Filter

0 : Disable

1 : False Color is reduced by using the horizontal low pass filter.

Cb First

0 : Cr value in front of Cb value in 16bit or 8bit video data output modes.

1 : Cb value in front of Cr value in 16bit or 8bit video data output modes.

Y First

0 : Cb and Cr value is outputted in front of Y in 8bit video output

1 : Y value is outputted in front of Cb and Cr value in 8bit video output.

This option is meaningful only with 8bit output mode.

8-bit Output

0 : 16bit Image Data are outputted through Y[7:0] and C[7:0].

1 : 8bit Image Data is produced only in Y[7:0]. C[7:0] are selected by Mode C register[03H]

Bayer Output

0 : Disable

1 : 8bit Bayer Data is produced only in Y[7:0] .

YCbCr 4:4:4

0 : Disable

1 : YCbCr 4:4:4 YCbCr 24bit data for a pixel is produced with 16bit-output mode. With color space conversion disabled, RGB 24bit data for a pixel is produced in this mode. This mode is meaningful only with 16bit-output mode.

YCbCr 4:2:2

0 : Disable

1 : YCbCr data for a pixel is produced with 8/16 bit-output mode.

Color Matrix (Color Correction)

The color spread effect mainly caused by color filter characteristics. The effect is compensated by 3x3-color matrix operation. Nine registers for matrix coefficients are used in color matrix operation to get the optimal pure color reproduction. The relationship between input color and color-corrected color is defined as below formula.

$$\begin{bmatrix} R' \\ G' \\ B' \end{bmatrix} = \begin{bmatrix} CMA11 & CMA12 & CMA13 \\ CMA21 & CMA22 & CMA23 \\ CMA31 & CMA32 & CMA33 \end{bmatrix} \bullet \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

Where R, G, and B : Sensor color output.

R', G', and B' : Color-corrected output.

Color matrix coefficients are programmable from –127/64 to 127/64. Programming register value for intended color matrix coefficients should be resolved by the following equations.

For positive values, CMAxx = Integer(Real Coefficient Value x 64);

For negative values, CMAxx = Two's Complement(Integer(Real Coefficient Value x 64));

Real Coefficient Value : From –127/64 to 127/64.

Color Matrix Coefficient 11 [CMA11 : 34h : 45h]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 11							
0	1	0	0	0	1	0	1

Color Matrix Coefficient 12 [CMA12 : 35h : f6h]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 12							
1	1	1	1	0	1	1	0

Color Matrix Coefficient 13 [CMA13 : 36h : 04h]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 13							
0	0	0	0	0	1	0	0

Color Matrix Coefficient 21 [CMA21 : 37h : f8h]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 21							
1	1	1	1	1	0	0	0

Color Matrix Coefficient 22 [CMA22 : 38h : 5dh]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 22							
0	1	0	1	1	1	0	1

Color Matrix Coefficient 23 [CMA23 : 39h : ebh]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 23							
1	1	1	0	1	0	1	1

Color Matrix Coefficient 31 [CMA31 : 3ah : 03h]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 31							
0	0	0	0	0	0	1	1

Color Matrix Coefficient 32 [CMA32 : 3bh : edh]

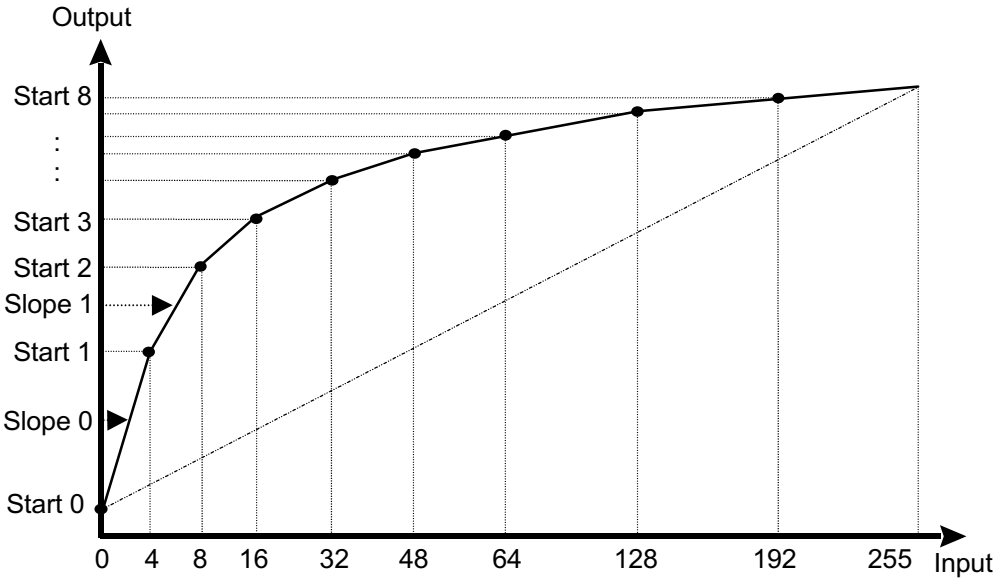
7	6	5	4	3	2	1	0
Color Matrix Coefficient 32							
1	1	1	0	1	1	0	1

Color Matrix Coefficient 33 [CMA33 : 3ch : 51h]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 33							
0	1	0	1	0	0	0	1

Gamma Correction

Piecewise linear gamma approximation method is implemented. Nine piece linear segments are supported and user-programmable.



Gamma Control

$$Slope_N = \frac{Start_{N+1} - Start_N}{In_{N+1} - In_N}$$

$$Output = Slope_N (Input - In_N) + Start_N$$

Where In_N(Fixed Value) : 0, 4, 8, 16, 32, 48, 64, 128, and 192, 255.

Gamma Slope Registers are programmed as the integer value of real slope multiplied by 8 or 16. For Gamma Slope 0 register, multiplier 8 is used for the program value calculation, and for others multiplier 16 is used.

Gamma Segment Start Points

Gamma Segment Start Points specify the start points of nine line segments for piecewise gamma approximation.

Gamma Point 0 [GAMP0 : 40h : 00h]

7	6	5	4	3	2	1	0
Gamma Point 0							
0	0	0	0	0	0	0	0

Gamma Point 1 [GMAP1 : 42h : 18h]

7	6	5	4	3	2	1	0
Gamma Point 1							

0	0	0	1	1	0	0	0

Gamma Point 2 [GMAP2 : 43h : 2ch]

7	6	5	4	3	2	1	0
Gamma Point 2							
0	0	1	0	1	1	0	0

Gamma Point 3 [GMAP3 : 44h : 47h]

7	6	5	4	3	2	1	0
Gamma Point 3							
0	1	0	0	0	1	1	1

Gamma Point 4 [GMAP4 : 45h : 6ch]

7	6	5	4	3	2	1	0
Gamma Point 4							
0	1	1	0	1	1	0	0

Gamma Point 5 [GMAP5 : 46h : 88h]

7	6	5	4	3	2	1	0
Gamma Point 5							
1	0	0	0	1	0	0	0

Gamma Point 6 [GMAP6 : 47h : a0h]

7	6	5	4	3	2	1	0
Gamma Point 6							
1	0	1	0	0	0	0	0

Gamma Point 7 [GMAP7 : 48h : e0h]

7	6	5	4	3	2	1	0
Gamma Point 7							
1	1	1	0	0	0	0	0

Gamma Point 8 [GMAP8 : 49h : f5h]

7	6	5	4	3	2	1	0
Gamma Point 8							
1	1	1	1	0	1	0	1

Gamma Slope Values

Gamma Slope Registers are programmed as the integer value of real slope multiplied by 8 or 16. For Gamma Slope 0 register, multiplier 8 is used for the program value calculation, and for others, multiplier 16 is used. Gamma Slope 0 is B<6:0>/8 and programmable range is 0 ~ 16. and for others are B<6:0>/16 and programmable range is 0 ~ 8.

Gamma Slope 0 [GMAS0 : 50h : 30h]

7	6	5	4	3	2	1	0
Reserved	Gamma Slope 0						
0	0	1	1	0	0	0	0

Gamma Slope 1 [GMAS1 : 52h : 50h]

7	6	5	4	3	2	1	0
Reserved	Gamma Slope 1						
0	1	0	1	0	0	0	0

Gamma Slope 2 [GMAS2 : 53h : 36h]

7	6	5	4	3	2	1	0
Reserved	Gamma Slope 1						
0	0	1	1	0	1	1	0

Gamma Slope 3 [GMAS3 : 54h : 25h]

7	6	5	4	3	2	1	0
Reserved	Gamma Slope 3						
0	0	1	0	0	1	0	1

Gamma Slope 4 [GMAS4 : 55h : 1ch]

7	6	5	4	3	2	1	0
Reserved	Gamma Slope 4						
0	0	0	1	1	1	0	0

Gamma Slope 5 [GMAS5 : 56h : 18h]

7	6	5	4	3	2	1	0
Reserved	Gamma Slope 5						
0	0	0	1	1	0	0	0

Gamma Slope 6 [GMAS6 : 57h : 10h]

7	6	5	4	3	2	1	0
Reserved	Gamma Slope 6						
0	0	0	1	0	0	0	0

Gamma Slope 7 [GMAS7 : 58h : 05h]

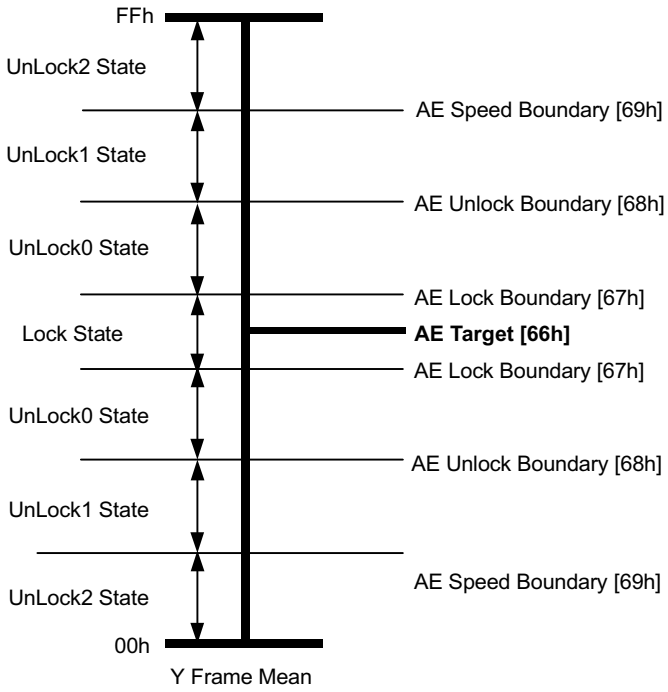
7	6	5	4	3	2	1	0
Reserved	Gamma Slope 7						
0	0	0	0	0	1	0	1

Gamma Slope 8 [GMAS8 : 59h : 03h]

7	6	5	4	3	2	1	0
Reserved	Gamma Slope 8						
0	0	0	0	0	0	1	1

Auto Exposure

Y mean value is continuously calculated every frame, then the integration time or preamp gain value are increased or decreased according to the displacement between current frame Y mean value and target Y mean value.



AE Mode Control 1 [AEM1 : 60h : 6bh]

7	6	5	4	3	2	1	0
AE Window			AE Method		AE Integration Time Speed		AE On
0	1	1	0	1	0	1	1

AE Window

1xx : Full window evaluation.

000 : 1/4 center only evaluation.

001 : 1/4 center weighted evaluation.

010 : 1/8 center only evaluation.

011 : 1/8 center weighted evaluation.

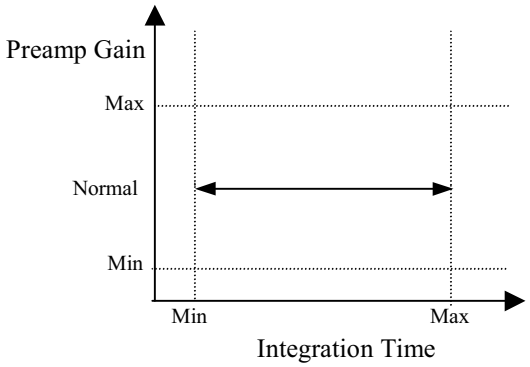
AE Method

00 : Use integration time only for AE.

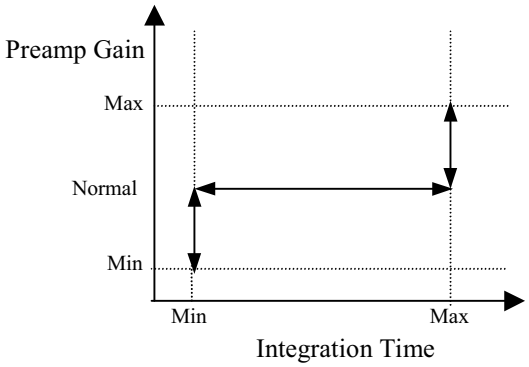
01 : Use integration time first and pre-amplifier gain at Max/Min of integration time for AE.

10 : Use multiple of anti-banding integration time only for AE.

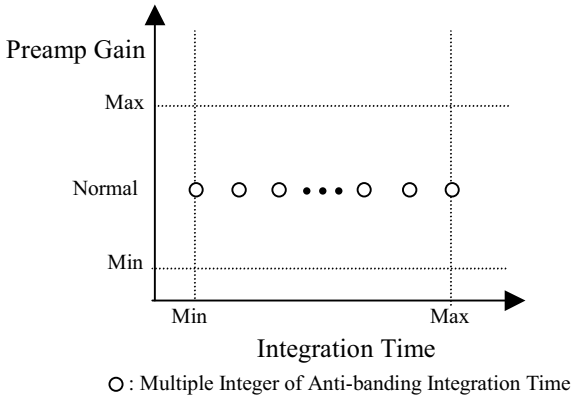
11 : Use multiple of anti-banding integration time first and pre-amplifier gain at Max/Min of integration time for AE.



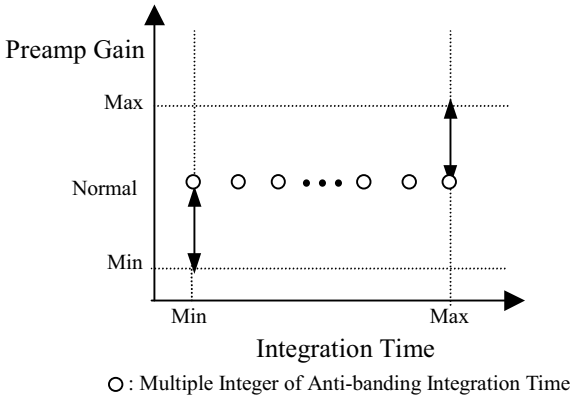
AE Method : 00



AE Method : 01



AE Method : 10



AE Method : 11

AE Integration Time Speed

(Slow) 00 -> 01 -> 10 -> 11(Fast)

AE On

0 : Auto exposure control disable.

1 : Auto exposure control enable.

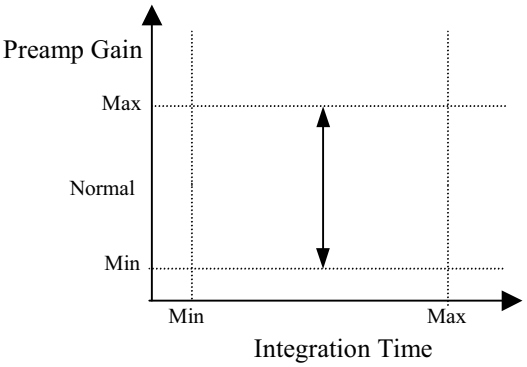
AE Mode Control 2 [AEM2 : 61h : 02h]

7	6	5	4	3	2	1	0
Reserved				AE Gain Only Mode	Anti-Banding Gain Mode	AE Gain Speed	
0	0	0	0	0	0	1	0

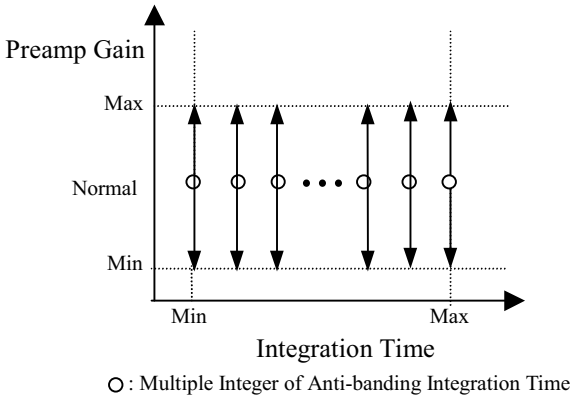
AE Gain Only Mode

0 : Disable

1 : When this bit is enabled, AE Method is disabled automatically and sensor doesn't adjust integration time but preamp gain for Auto Exposure. Therefore, user can get the image data at constant frame rate



AE Gain Only Mode



○ : Multiple Integer of Anti-banding Integration Time

Anti-Banding Gain Mode

Anti-Banding Gain Mode

0 : Disable

1 : When this bit is enabled and AE Method is 11, sensor adjusts preamp gain in Unlock0 state and integration time in UnLock1,2. However, sensor adjusts preamp gain when integration time reached Min/Max and AE state is Unlock(Unlock0, Unlock1 and Unlock2) state.

AE Gain Speed

(Slow) 00 -> 01 -> 10 -> 11(Fast)

Integration Time High [INTH: 63h : 02h]

7	6	5	4	3	2	1	0
Integration Time [23:16]							
0	0	0	0	0	0	1	0

Integration Time Middle [INTM: 64h: 71h]

7	6	5	4	3	2	1	0
Integration Time [15:8]							
0	1	1	1	0	0	0	1

Integration Time Low [INTL: 65h: 00h]

7	6	5	4	3	2	1	0
Integration Time [7:0]							
0	0	0	0	0	0	0	0

Integration time value register defines the time during which active pixel element evaluates photon energy that is converted to digital data output by internal ADC processing. Integration time is equivalent to exposure time of general film camera. So that integration time need to be increased in dark environment and decreased in bright environment. Because minimum value of integration time is 88, don't set integration time under 88. Maximum value of integration time is 2^{24}-1. This value should be even number. When master clock frequency(MCF) is 24Mhz and Clock Division is 1, default integration time is 40ms (160000(027100h) X 250ns (SCF = 4Mhz)).
Note : All three bytes should be updated together even though one of three bytes is changed.

AE Target [AETGT : 66h : 70h]

7	6	5	4	3	2	1	0
AE Target							
0	1	1	1	0	0	0	0

This register defines the target luminance(Y) value for Auto Exposure operation.

AE Lock Boundary [AELBND : 67h : 02h]

7	6	5	4	3	2	1	0
AE Lock Boundary							
0	0	0	0	0	0	1	0

AE Lock Boundary specifies the displacement from AE Target to determine Lock state for AE. When the displacement value from Y Frame Mean value to AE Target value is less than AE Lock Boundary, AE goes into Lock state.

AE Unlock Boundary [AEUBND : 68h : 2ah]

7	6	5	4	3	2	1	0
AE Unlock Boundary							
0	0	1	0	1	0	1	0

AE Unlock Boundary specifies the displacement from AE Target to determine UnLock0 state for AE. When the displacement value from Y Frame Mean value to AE Target value is more than AE Lock Boundary and less than AE Unlock Boundary, AE goes into UnLock0 state and integration time or preamplifier gain increment/decrement for AE is 1x.

AE Speed Boundary [AESBND : 69h : 30h]

7	6	5	4	3	2	1	0
AE Speed Boundary							
0	0	1	1	0	0	0	0

AE Speed Boundary specifies the displacement from AE Target to determine Unlock1 state and Unlock2 state for AE. When the displacement value from Y Frame Mean value to AE Target value is more than AE Unlock Boundary and less than AE Speed Boundary, AE goes into Unlock1 state and integration time or preamp gain increment/decrement for AE is 2x. When the displacement value from Y Frame Mean value to AE Target value is more than AE Speed Boundary, AE goes into Unlock2 State and integration time or preamp gain increment/decrement for AE is 4x to converge on Lock state fast.

AE Anti-Banding Step High [AEANTH : 6ah : 00h]

7	6	5	4	3	2	1	0
AE Anti-Banding Step[23:16]							
0	0	0	0	0	0	0	0

AE Anti-Banding Step Middle [AEANTM : 6bh : 9ch]

7	6	5	4	3	2	1	0
AE Anti-Banding Step[15:8]							
1	0	0	1	1	1	0	0

AE Anti-Banding Step Low [AEANTL : 6ch : 40h]

7	6	5	4	3	2	1	0
AE Anti-Banding Step[7:0]							
0	1	0	0	0	0	0	0

AE Anti-Banding Step specifies integration time unit value that AE uses when Anti-Banding is

enabled(Refer to AE Mode1). This value should be even number. Anti-Banding Step value is resolved by the following equation. The default value is 1/100 second at using Master Clock Frequency(MCF) as 24MHz, Clock Division as 1 and power line frequency is 50Hz.

Anti-Banding Step Value = Sensor Clock Frequency(SCF=MCF/6/Clock Division) / (2 x power line frequency)

Note : All three bytes should be updated together even though one of three bytes is changed.

AE Integration Time Limit High [AELMH : 6dh : 07h]

7	6	5	4	3	2	1	0
AE Integration Time Limit[23:16]							
0	0	0	0	0	1	1	1

AE Integration Time Limit Middle [AELMM : 6eh : a1h]

7	6	5	4	3	2	1	0
AE Integration Time Limit[15:8]							
1	0	1	0	0	0	0	1

AE Integration Time Limit Low [AELML : 6fh : 20h]

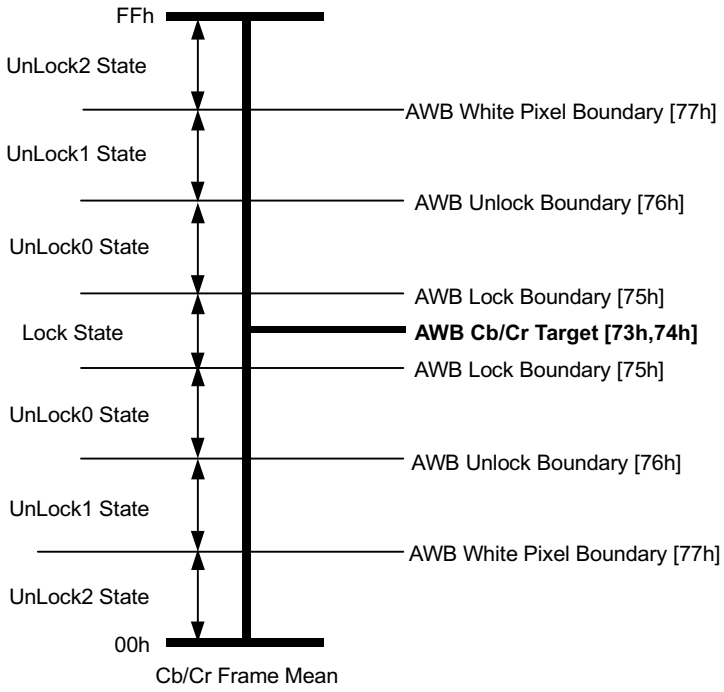
7	6	5	4	3	2	1	0
AE Integration Time Limit[7:0]							
0	0	1	0	0	0	0	0

These three registers define the maximum integration time value that is allowed to sensor operation. It is desirable to set the value to multiples of AE Anti-Banding Step to easily operate with Anti-banding mode enabled. This value should be even number. When master clock frequency(MCF) is 24Mhz and Clock Division is 1, default integration time limit is 125ms (500000(07a120h) X 250ns (SCF = 4Mhz))

Note : All three bytes should be updated together even though one of three bytes is changed.

Auto White Balance Control

Cb/Cr frame mean value is calculated every frame and according to Cb/Cr frame mean values' displacement from Cb/Cr white target point, R/B scaling values for R/B data are resolved.



AWB Mode Control [AWBM : 70h : 01h]

7	6	5	4	3	2	1	0
Reserved		AWB Coarse Speed			AWB Fine Speed		AWB On
0	0	0	0	0	0	0	1

AWB Coarse Speed

(Fast) 00 -> 01 -> 10 -> 11 (Slow)

AWB Fine Speed

(Slow) 00 -> 01 -> 10 -> 11 (Fast)

AWB On

0 : Auto white balance control disabled

1 : Auto white balance control enabled

Cb Target [CBTGT : 73h : 80h]

7	6	5	4	3	2	1	0
Cb Target							
1	0	0	0	0	0	0	0

This register defines Cb target frame mean value for AWB operation.

Cr Target [CRTGT : 74h : 80h]

7	6	5	4	3	2	1	0
Cr Target							
1	0	0	0	0	0	0	0

This register defines Cr target frame mean value for AWB operation.

AWB Lock Boundary [AWBLB : 75h : 02h]

7	6	5	4	3	2	1	0
AWB Lock Boundary							
0	0	0	0	0	0	1	0

AWB Lock Boundary specifies the displacement from Cb/Cr Target to determine Lock state for AWB. When the displacement value from Cb/Cr Frame Mean value to AWB Target value is less than AWB Lock Boundary, AWB goes into Lock state.

AWB Unlock Boundary [AWBUB : 76h : 06h]

7	6	5	4	3	2	1	0
AWB Unlock Boundary							
0	0	0	0	0	1	1	0

AWB Unlock Boundary specifies the displacement from AWB Target to determine Unlock0 state for AWB. When the displacement value from Cb/Cr Frame Mean value to AWB Target value is more than AWB Lock Boundary and less than AWB Unlock Boundary, AWB goes into Unlock0 state and R/B scaler increment/decrement for AWB is 1x.

AWB White Pixel Boundary [AWBWPB : 77h : 30h]

7	6	5	4	3	2	1	0
AWB White Pixel Boundary							
0	0	1	1	0	0	0	0

AWB White Pixel Boundary specifies the displacement from AWB Target to determine Unlock1 state and Unlock2 state for AWB. When the displacement value from Cb/Cr Frame Mean value to AWB Target value is more than AWB Unlock Boundary and less than AWB White Pixel Boundary, AWB goes into Unlock1 state and R/B scaler increment/decrement for AWB is 2x. When the displacement value from Cb/Cr Frame Mean value to AWB Target value is more than AWB White Pixel Boundary, AWB accept frame color as it is and does not try to correct white balance deviation.

AWB Blue Scaling [AWBSCLB : 78h : 40]

7	6	5	4	3	2	1	0
AWB B Scaling							
0	1	0	0	0	0	0	0

The register represents the current Blue scaling value (1/64 resolution) in RB Scaling block, and is updated every frame by AWB logic.

AWB Red Scaling [AWBSCLR : 79h : 40]

7	6	5	4	3	2	1	0
AWB R Scaling							
0	1	0	0	0	0	0	0

The register represents the current Red scaling value(1/64 resolution) in RB Scaling block, and is updated every frame by AWB logic.

AWB / AE Status [AEWBST : 7ah : RO]

7	6	5	4	3	2	1	0
Reserved		Y AE state		Cb AWB State		Cr AWB State	
-	-	RO	RO	RO	RO	RO	RO

Y Frame Mean [YFMEAN : 7bh : RO]

7	6	5	4	3	2	1	0
Y Frame Mean							
RO	RO	RO	RO	RO	RO	RO	RO

The register reports current Y plane frame mean value.

Cb Frame Mean [CBFMEAN : 7ch : RO]

7	6	5	4	3	2	1	0
Cb Frame Mean							
RO	RO	RO	RO	RO	RO	RO	RO

The register reports current Cb plane frame mean value.

Cr Frame Mean [CRFMEAN : 7dh : RO]

7	6	5	4	3	2	1	0
Cr Frame Mean							
RO	RO	RO	RO	RO	RO	RO	RO

The register reports current Cr plane frame mean value.

AWB Luminance Limit [AWBYLMT : 8ah : 00]

7	6	5	4	3	2	1	0
Y Upper Limit				Y Lower Limit			
0	0	0	0	0	0	0	0

Luminance(Y) value of each pixel is valid for AWB, when it is over (8xY Lower Limit) and under (255 – 8xY Upper Limit).

8xY Lower Limit < Luminance of Valid Pixel for AWB < 255 – 8xY Upper Limit – Eq.(1)

Default Value : 0 < Luminance of Valid Pixel for AWB < 255

AWB Chrominance Limit [AWBCLMT : 8bh : ff]

7	6	5	4	3	2	1	0
C Upper Limit				C Lower Limit			
1	1	1	1	1	1	1	1

Chrominance(Cb, Cr) value of each pixel is valid for AWB, when it is over (C target – 8xC Lower Limit) and under (C target + 8xC Upper Limit).

C target – 8xC Lower Limit < Chrominance of Valid Pixel for AWB < C target + 8xC Upper Limit–Eq.(2)

Default Value : 8 < Chrominance of Valid Pixel for AWB < 248

AWB Valid Pixel Number Threshold [AWBPXLTH : 8ch : 02]

7	6	5	4	3	2	1	0
AWB Valid Pixel Number Threshold							
0	0	0	0	0	0	1	0

This register means number threshold of valid pixel in one frame for AWB. Number threshold of valid pixel in one frame for AWB should be over (128 x this register).

Number threshold of valid pixel in one frame > 128 x AWB Valid Pixel Number Threshold –Eq.(3)

Default is 256.

AWB Valid Pixel Number Count High[AWBPXLH : 8dh : RO]

7	6	5	4	3	2	1	0
AWB Valid Pixel Number Count High							
RO	RO	RO	RO	RO	RO	RO	RO

AWB Valid Pixel Number Count Low[AWBPXLL : 8eh : RO]

7	6	5	4	3	2	1	0
AWB Valid Pixel Number Count Low							
RO	RO	RO	RO	RO	RO	RO	RO

This two byte registers have a value representing a second(1/2) of pixels that follow Eq.(1,2,3) during one frame time and is updated every a frame.

Dark Bad Integration Time High[DPCINTH : 91h : 06]

7	6	5	4	3	2	1	0
Dark Bad Integration Time High							
0	0	0	0	0	1	1	0

Dark Bad Integration Time Middle[DPCINTM : 92h : 1a]

7	6	5	4	3	2	1	0
Dark Bad Integration Time Middle							
0	0	0	1	1	0	1	0

Dark Bad Integration Time Low[DPCINTL : 93h : 80]

7	6	5	4	3	2	1	0
Dark Bad Integration Time Low							
1	0	0	0	0	0	0	0

Dark Bad Integration Time registers(91h-93h) specify minimum integration time value(63h-65h) where dark bad concealment is performed when dark bad pixel concealment is enable.

Dark Bad Green Threshold[DPCGTH : 94h : 0ah]

7	6	5	4	3	2	1	0
Dark Bad Green Threshold							
0	0	0	0	1	0	1	0

This register value checks whether current Green pixel is dark bad pixel or not. When the current G pixel's different value with neighbor G pixels is over this register, sensor replaces current pixel with compensated pixel.

Dark Bad Red Threshold[DPCRTH : 95h : 0ah]

7	6	5	4	3	2	1	0
Dark Bad Red Threshold							
0	0	0	0	1	0	1	0

This register value checks whether current Red pixel is dark bad pixel or not. When the current R pixel's different value with neighbor R pixels is over this register, sensor replaces current pixel with compensated pixel.

Dark Bad Blue Threshold[DPCBTH : 96h : 0ah]

7	6	5	4	3	2	1	0
Dark Bad Blue Threshold							
0	0	0	0	1	0	1	0

This register value checks whether current Blue pixel is dark bad pixel or not. When the current B pixel's different value with neighbor B pixels is over this register, sensor replaces current pixel with compensated pixel.

Frame Timing

For clear description of frame timing, clocks' acronym and relation are reminded in here again.

< Clock Acronym Definition >

MCF(Master Clock Frequency) : MCLK	DCF(Divided Clock Frequency) : MCF/Clock Division
SCF(Sensor Clock Frequency) : DCF/6	ICF(Image Processing Clock Frequency) : SCF for CIF/SIF/QCIF/QSIF : SCF/2 for Sub-Sample QCIF/QSIF
VCF(Video Clock Frequency) : ICF for 16bit 422 : ICF*2 for 8bit 422 / 16bit 444	LCF(Line Clock Frequency) : SCF/ (HBLANK Time + Video Width Time)

SCP(Sensor Clock Period) = 1/SCF, LCP(Line Clock Period) = 1/LCF

< Video Width and Height>

Video Mode	Width		Height	
	Time	Number of Pixel in Line	Time	Number of Line
CIF	352SCP	352EA	288LCP	288EA
SIF	320SCP	320EA	240LCP	240EA
QCIF	176SCP	176EA	144LCP	144EA
QSIF	160SCP	160EA	120LCP	120EA
Sub-Sample QCIF	352SCP	176EA	288LCP	144EA
Sub-Sample QSIF	320SCP	160EA	240LCP	120EA

< Frame Time Calculation >

Core Frame Time = IDLE Slot + Video Height * LCP

Real Frame Time

Case 1) Integration Time > Core Frame Time

Real Frame Time = Integration Time + VBLANK * LCP

Case 2) Integration Time <= Core Frame Time

Real Frame Time = Core Frame Time + VBLANK * LCP

HOLD Slot Time

Case 1) Integration Time > Core Frame Time

HOLD Slot Time = Integration Time - Core Frame Time

Case 2) Integration Time <= Core Frame Time

HOLD Slot Time = 0

where IDLE Slot is 1LCP.

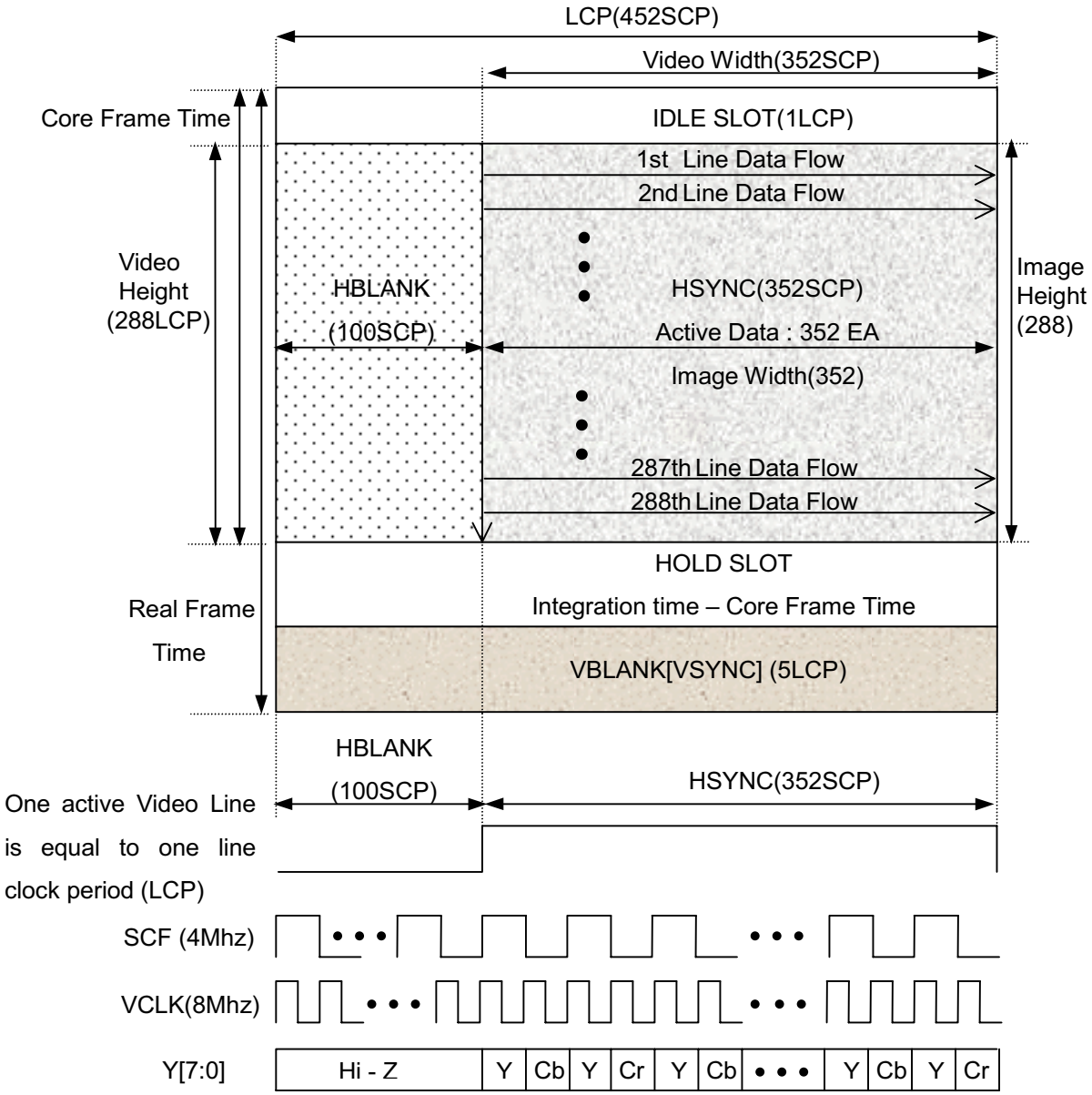
1. CIF Timing when Programmable Window is disabled

CIF Frame Timing Related Parameters			
Master Clock Frequency(MCF)	24Mhz	Clock Division	1
Sensor Clock Frequency(SCF)	24Mhz/1/6 = 4Mhz	Sensor Clock Period(SCP)	1/4Mhz = 250ns
HBLANK Value	100 SCP	VBLANK Value	5 LCP
VSYNC Mode	Line Mode	Line Clock Period(LCP)	452 SCP
Output Bus Width	8bit	CIF Video Output Frequency	SCF * 2 = 8Mhz
Programmable Window	OFF	Half Window Width / Height	
Y First / Cb First	ON / ON	Integration Time	160,000

LCP = (100 + 352)*SCP = 0.113ms, IDLE Slot = 1*LCP=0.113ms

Core Frame Time = 1*LCP + 288*LCP = 32.657ms, Hold Slot = 160,000*SCP – 289*LCP = 7.343ms

Real Frame Time = 160,000*SCP + 5*LCP = 40.565ms



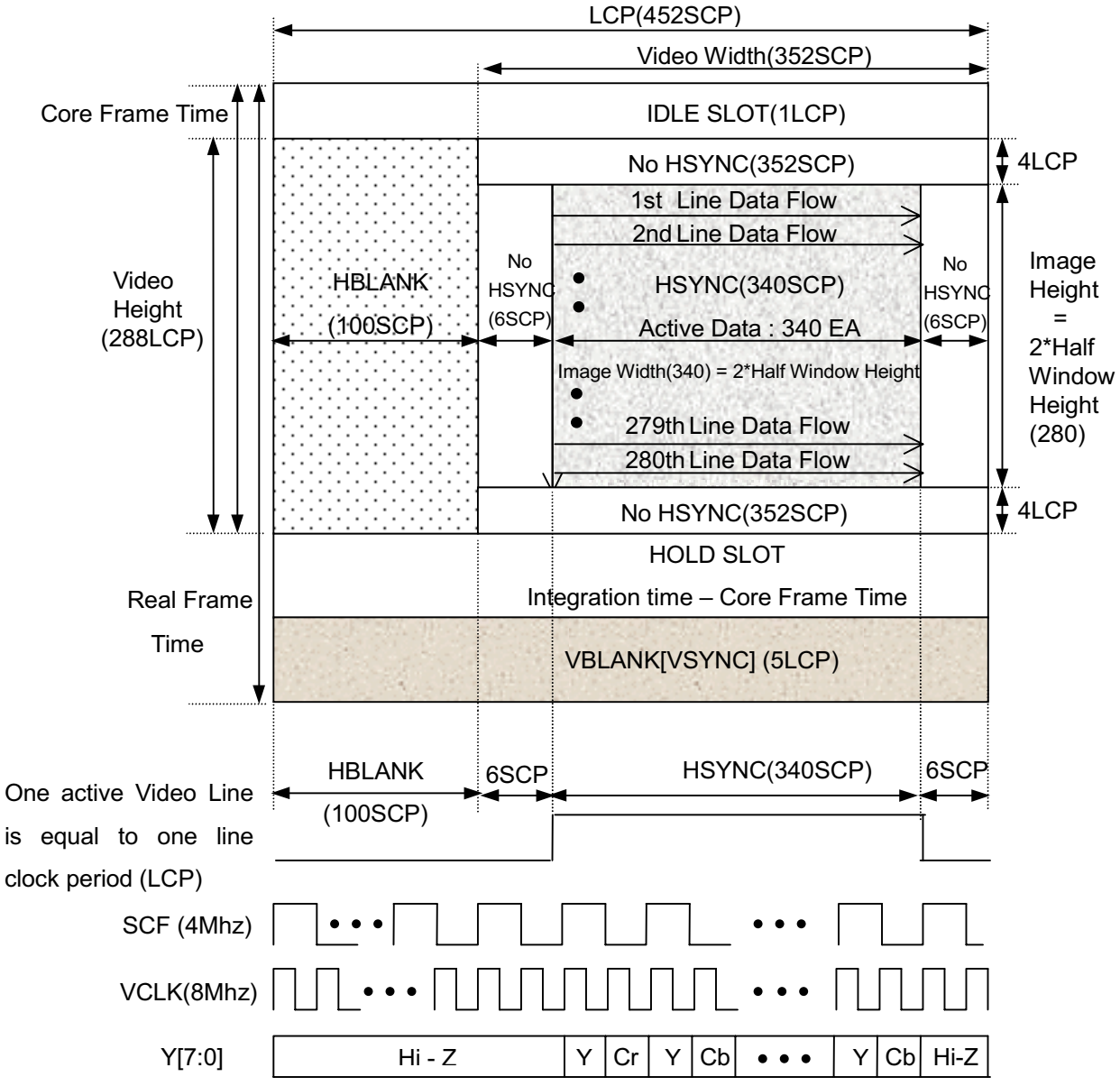
2. CIF Timing when Programmable Window is enabled

CIF Frame Timing Related Parameters			
Master Clock Frequency(MCF)	24Mhz	Clock Division	1
Sensor Clock Frequency(SCF)	24Mhz/1/6 = 4Mhz	Sensor Clock Period(SCP)	1/4Mhz = 250ns
HBLANK Value	100 SCP	VBLANK Value	5 LCP
VSYNC Mode	Line Mode	Line Clock Period(LCP)	452 SCP
Output Bus Width	8bit	CIF Video Output Frequency	SCF * 2 = 8Mhz
Programmable Window	ON	Half Window Width / Height	170/140
Y First / Cb First	ON / ON	Integration Time	132,888

LCP = (100 + 352)*SCP = 0.113ms, IDLE Slot = 1*LCP=0.113ms

Core Frame Time = 1*LCP + 288*LCP = 32.657ms, Hold Slot = 160,000*SCP – 289*LCP = 7.343ms

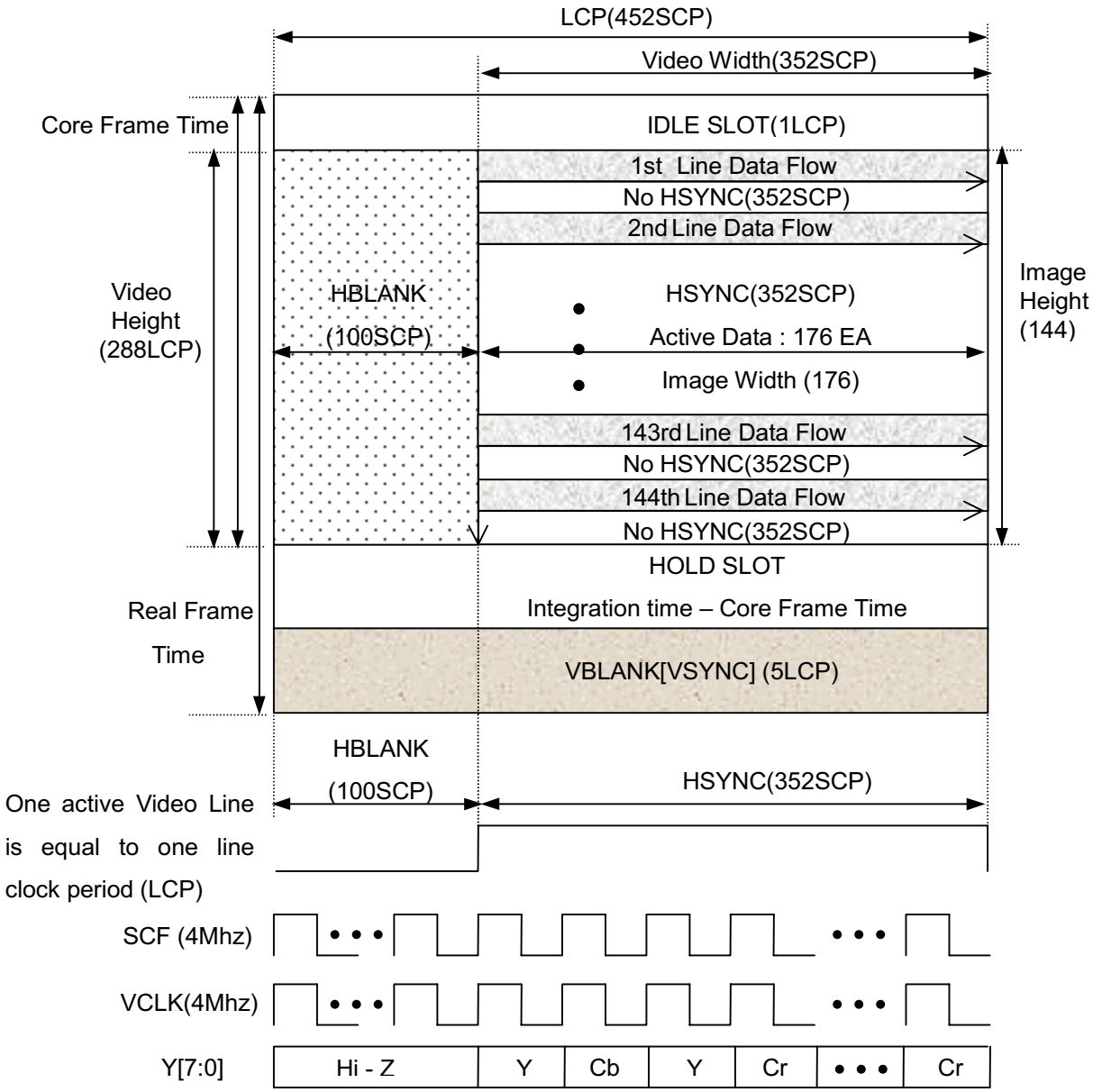
Real Frame Time = 160,000*SCP + 5*LCP = 40.565ms



3. Sub-Sample QCIF Timing when Programmable Window is disabled

Sub-Sample QCIF Frame Timing Related Parameters			
Master Clock Frequency(MCF)	24Mhz	Clock Division	1
Sensor Clock Frequency(SCF)	24Mhz/1/6 = 4Mhz	Sensor Clock Period(SCP)	1/4Mhz = 250ns
HBLANK Value	100 SCP	VBLANK Value	5 LCP
VSYNC Mode	Line Mode	Line Clock Period(LCP)	452 SCP
Output Bus Width	8bit	CIF Video Output Frequency	SCF * 2 = 8Mhz
Programmable Window	OFF	Half Window Width / Height	
Y First / Cb First	ON / ON	Integration Time	132,888

LCP = (100 + 352)*SCP = 0.113ms, IDLE Slot = 1*LCP=0.113ms
Core Frame Time = 1*LCP + 288*LCP = 32.657ms, Hold Slot = 160,000*SCP – 289*LCP = 7.343ms
Real Frame Time = 160,000*SCP + 5*LCP = 40.565ms



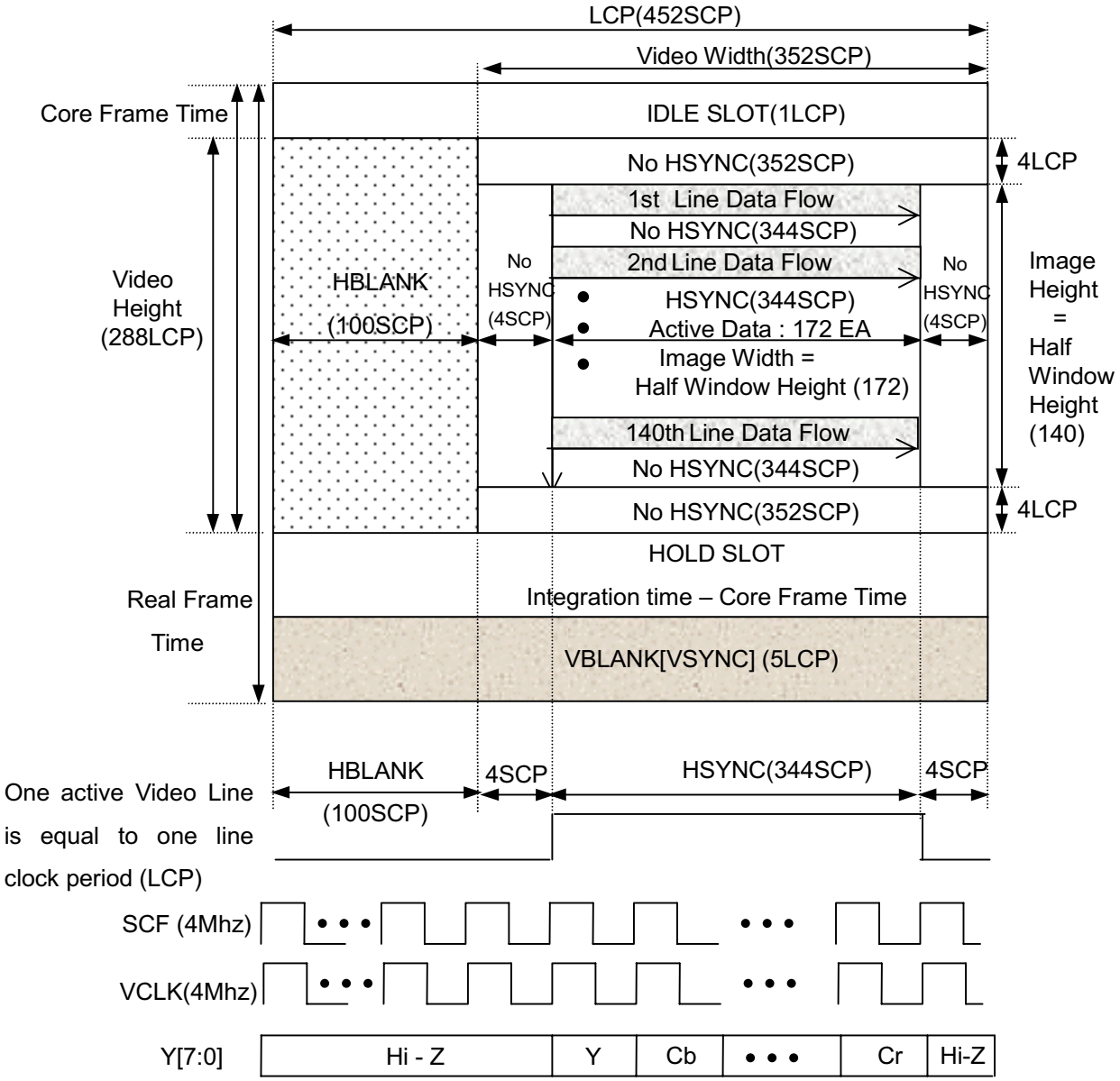
4. Sub-Sample QCIF Timing when Programmable Window is enabled

Sub-Sample QCIF Frame Timing Related Parameters			
Master Clock Frequency(MCF)	24Mhz	Clock Division	1
Sensor Clock Frequency(SCF)	24Mhz/1/6 = 4Mhz	Sensor Clock Period(SCP)	1/4Mhz = 250ns
HBLANK Value	100 SCP	VBLANK Value	5 LCP
VSYNC Mode	Line Mode	Line Clock Period(LCP)	452 SCP
Output Bus Width	8bit	CIF Video Output Frequency	SCF * 2 = 8Mhz
Programmable Window	ON	Half Window Width / Height	172/140
Y First / Cb First	ON / ON	Integration Time	132,888

LCP = (100 + 352)*SCP = 0.113ms, IDLE Slot = 1*LCP=0.113ms

Core Frame Time = 1*LCP + 288*LCP = 32.657ms, Hold Slot = 160,000*SCP – 289*LCP = 7.343ms

Real Frame Time = 160,000*SCP + 5*LCP = 40.565ms



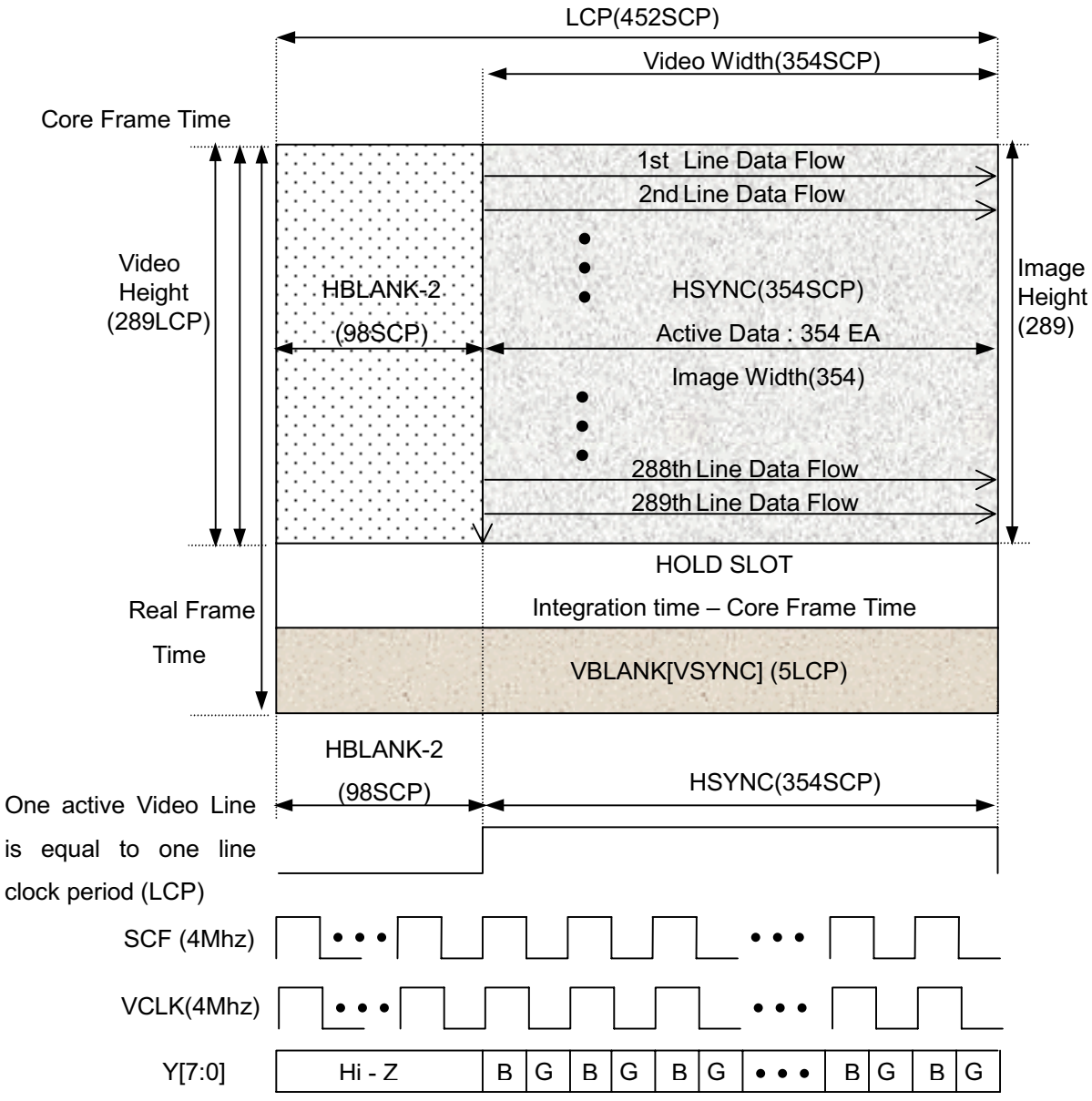
5. Bayer Output

Bayer Output Timing Related Parameters			
Master Clock Frequency(MCF)	24Mhz	Clock Division	1
Sensor Clock Frequency(SCF)	24Mhz/1/6 = 4Mhz	Sensor Clock Period(SCP)	1/4Mhz = 250ns
HBLANK Value	100 SCP	VBLANK Value	5 LCP
VSYNC Mode	Line Mode	Line Clock Period(LCP)	452 SCP
Output Bus Width	8bit	CIF Video Output Frequency	SCF * 2 = 8Mhz
Programmable Window	OFF	Half Window Width / Height	
Y First / Cb First	ON / ON	Integration Time	160,000

LCP = (99 + 353)*SCP = 0.113ms

Core Frame Time = 289*LCP = 32.657ms, Hold Slot = 160,000*SCP – 289*LCP = 7.343ms

Real Frame Time = 160,000*SCP + 5*LCP = 40.565ms



6. **SIF/QCIF/QSIF Timing**

SIF/QCIF/QSIF timing is the same as the CIF timing except video width and height

7. Sub-Sample QCIF Timing

Sub-sample QSIF timing is the same as the sub-sample CIF timing except video width and height

Following Figures show the timing of above 5 examples.

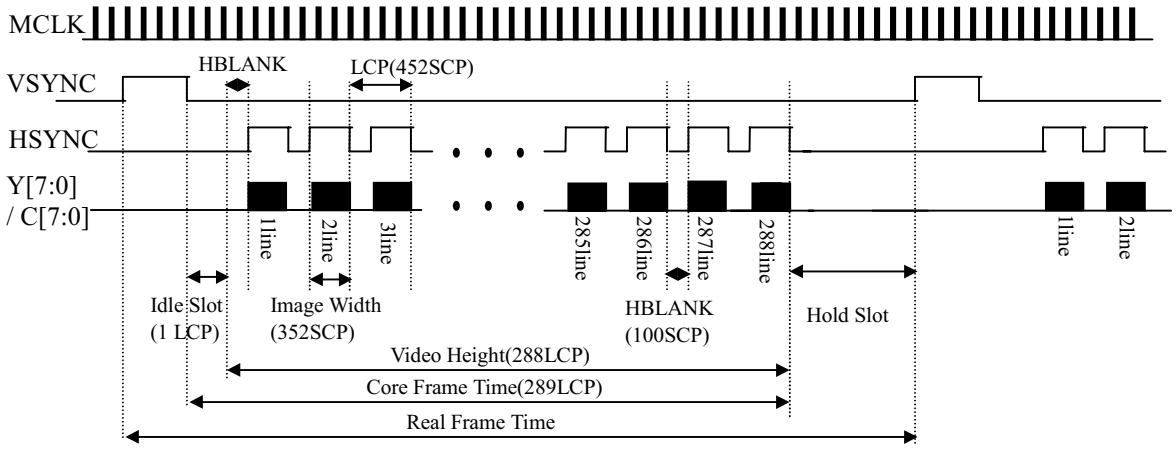


Figure 1. CIF Timing when Programmable Window is disabled

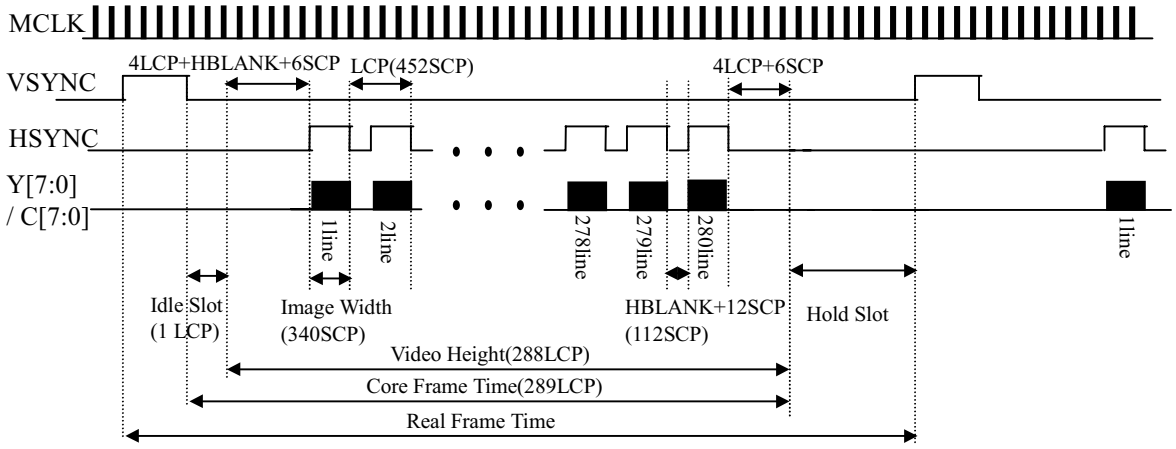


Figure 2. CIF Timing when Programmable Window is enabled

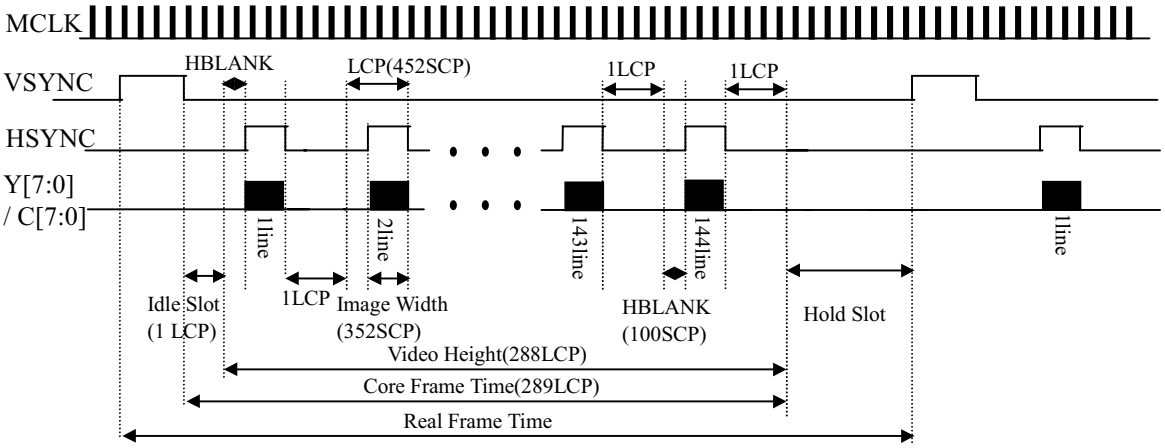


Figure 3. Sub-Sample CIF Timing when Programmable Window is disabled

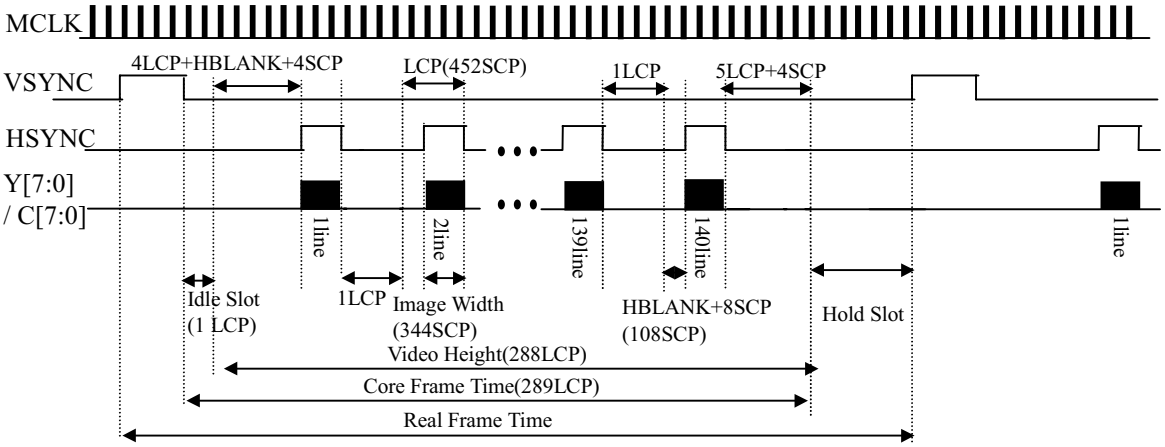


Figure 4. Sub-Sample CIF Timing when Programmable Window is enabled

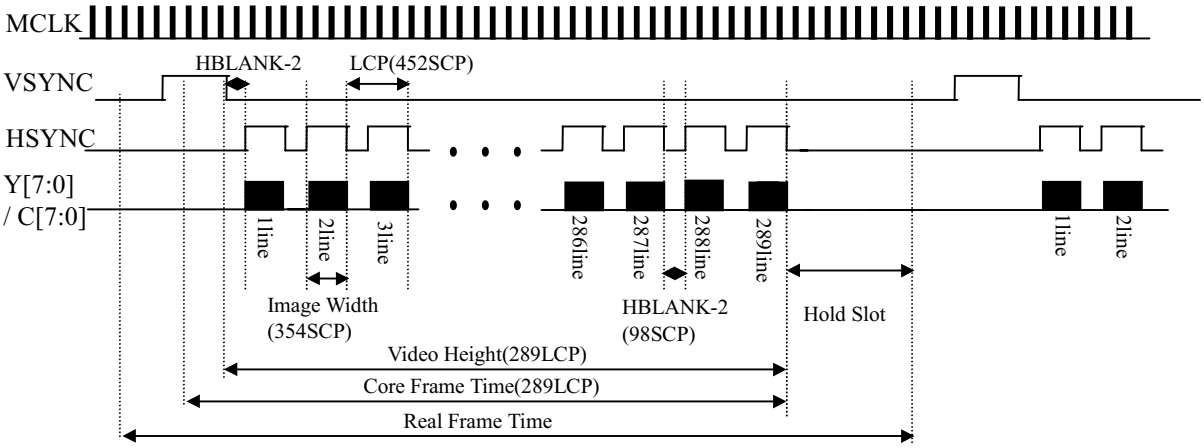


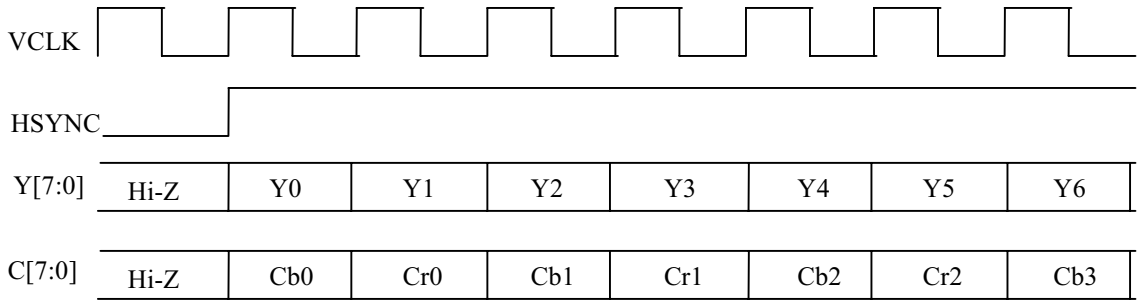
Figure 5. Bayer Output Timing

Output Data Format

Output timings for general configurations are described below. Slot named as “X” means that it is has no meaningful value and should be discarded.

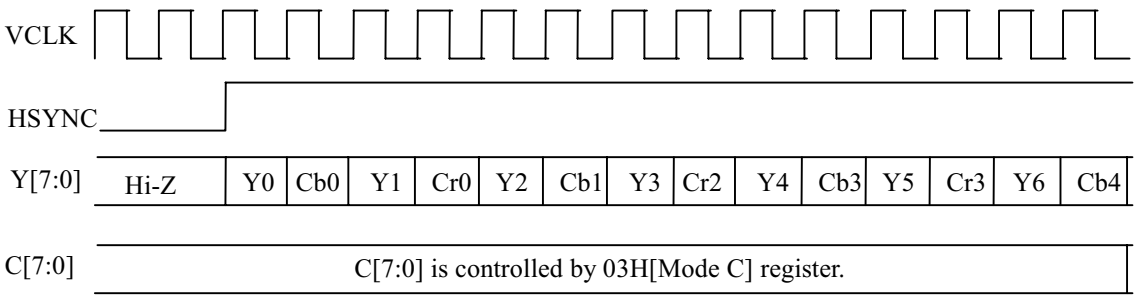
1. YCbCr 4:2:2 with 16bit output

Register bit configurations: 16bit output, Cb First, YCbCr 4:2:2 and Color space conversion enabled



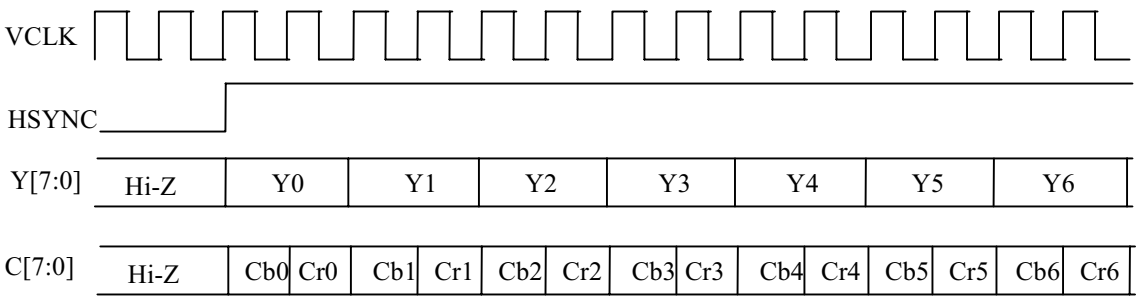
2. YCbCr 4:2:2 with 8bit output

Register bit configurations: 8bit output, Y First, Cb First, YCbCr 4:2:2 and Color space conversion enabled



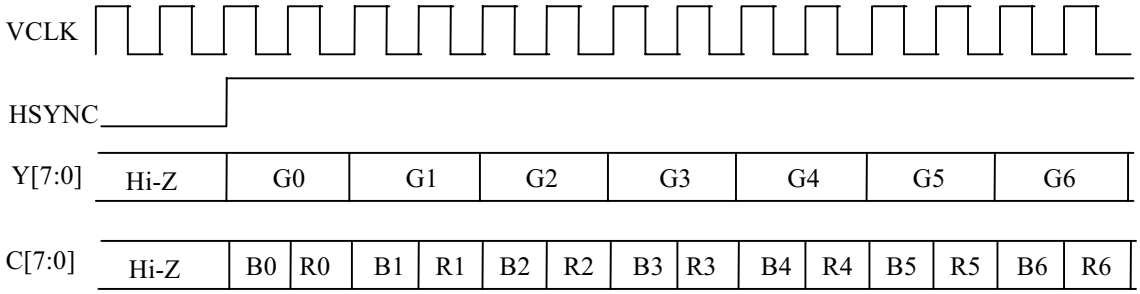
3. 24bit YCbCr 4:4:4 output

Register bit configurations : 16bit output, Y First, Cb First, YCbCr 4:4:4 and Color space conversion enabled



4. 24bit RGB 4:4:4 output

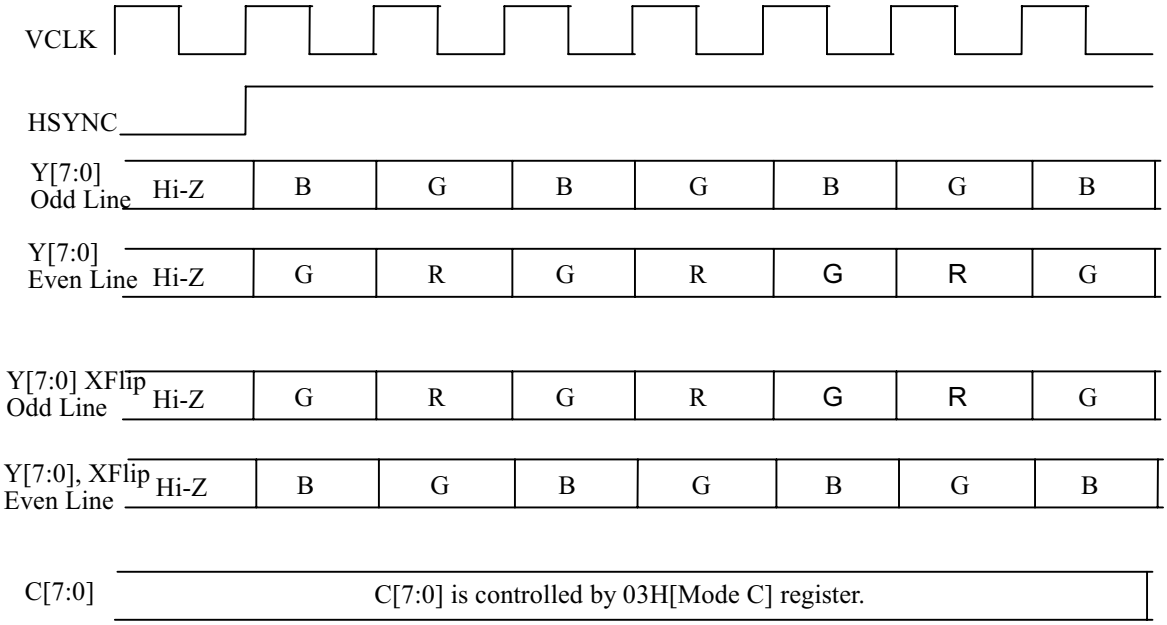
Register bit configurations : 16bit output, Y First, Cb First, YCbCr 4:4:4 and Color space conversion disabled



5. Bayer output

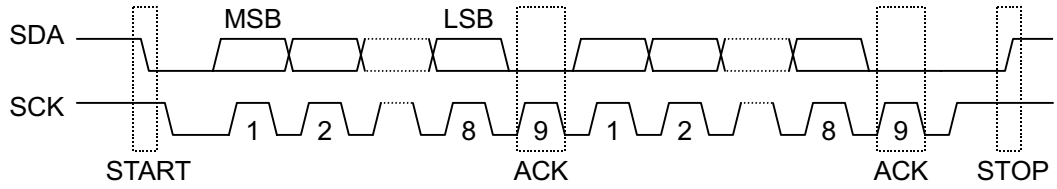
This mode is for test operation. Output data size is 354 X 289.

Register bit configurations: Bayer Output, 8bit output, and Color space conversion disabled.



I2C Chip Interface

The serial bus interface consists of the SDA(serial data) and SCK(serial clock) pins. HV7121GP sensor can operate only as a slave. The SCK only controls the serial interface. However, MCLK should be supplied and RESET should be high signal during controlling the serial interface. The Start condition is that logic transition (High to Low) on the SDA pin while the SCK pin is at high. The Stop condition is that logic transition (Low to High) on the SDA pin while the SCK pin is at high. To generate Acknowledge signal, the Sensor drives the SDA low when the SCK is high. Every byte consists of 8 bits. Each byte transferred on the bus must be followed by an Acknowledge. The most significant bit of the byte should always be transmitted first.



Register Write Sequences

One Byte Write

S	22H	A	01H	A	03H	A	P
*1	*2	*3	*4	*5	*6	*7	*8

Set "Sensor Control A" register into Window mode

*1. Drive: I2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit]

*3. Read: acknowledge from sensor

*4. Drive: 01H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: 03H [Video Mode : CIF]

*7. Read: acknowledge from sensor

*8. Drive: I2C stop condition

Multiple Byte Write using Auto Address Increment

S	22H	A	10H	A	00H	A	64H	A	P
*1	*2	*3	*4	*5	*6	*7	*8	*9	*10

Set "HSYNC Blanking High/Low" register as 0064H with auto address increment

*1. Drive: I2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit]

*3. Read: acknowledge from sensor

*4. Drive: 10H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: 00H [HSYNC Blanking High]

*7. Read: acknowledge from sensor

*8. Drive: 64H [HSYNC Blanking Low]

*9. Read: acknowledge from sensor

*10. Drive: I2C stop condition

Register Read Sequence

S	22H	A	01H	A	S	23H	A	13H	A	P
*1	*2	*3	*4	*5	*6	*7	*8	*9	*10	*11

Read "Sensor Control A" register from HV7121GP

*1. Drive: I2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit(be careful. R/W=0)]

*3. Read: acknowledge from sensor

*4. Drive: 01H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: I^2C start condition

*7. Drive: 23H(001_0001 + 1) [device address + R/W bit(be careful. R/W=1)]

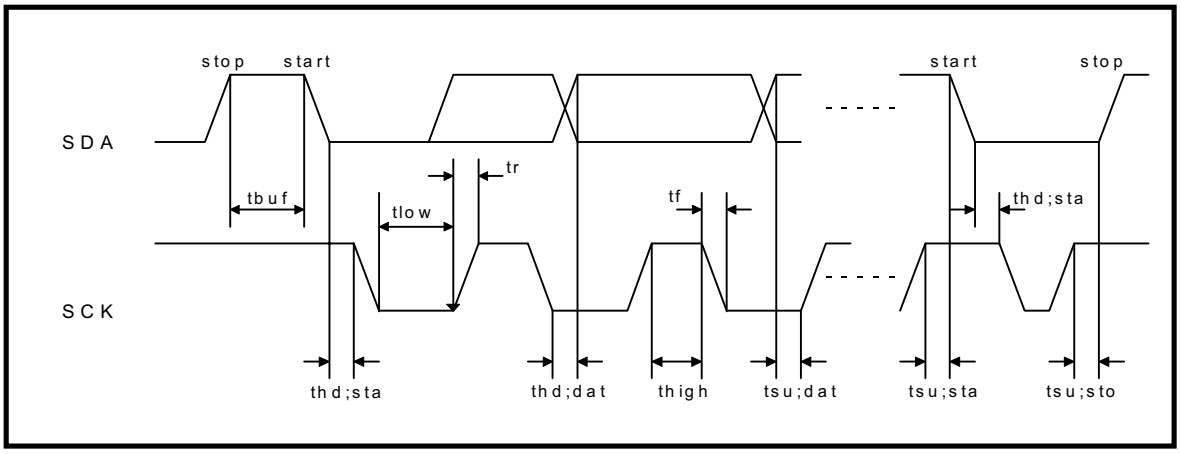
*8. Read: acknowledge from sensor

*9. Read: Read “13H(Value of Sensor Control A) ” from sensor

*10. Drive: acknowledge to sensor. If there is more data bytes to read, SDA should be driven to low and data read states(*9, *10) is repeated. Otherwise SDA should be driven to high to prepare for the read transaction end.

*11. Drive: I2C stop condition

I2C Bus Timing



Parameter	Symbol	Min.	Max.	Unit
SCK clock frequency	f_{sck}	0	400	KHz
Time that I^2C bus must be free before a new transmission can start	t_{buf}	1.2	-	us
Hold time for a START	$t_{hd};s_{ta}$	1.0	-	us
LOW period of SCK	t_{low}	1.2	-	us
HIGH period of SCK	t_{high}	1.0	-	us
Setup time for START	$t_{su};s_{ta}$	1.2	-	us
Data hold time	$t_{hd};d_{at}$	1.3	-	us
Data setup time	$t_{su};d_{at}$	250	-	ns
Rise time of both SDA and SCK	t_r	-	250	ns
Fall time of both SDA and SCK	t_f	-	300	ns
Setup time for STOP	$t_{su};s_{to}$	1.2	-	us
Capacitive load of SCK/SDA	C_b	-	-	pF

AC/DC Characteristics

Absolute Maximum Ratings

Supply Voltage(Analog, Digital) : 2.6 V ~ 3.0 V

Operating Temperature(Centigrade) : -10 ~ 50

Storage Temperature(Centigrade) : -30 ~ 80

Stresses exceeding the absolute maximum ratings may induce failure.

DC Operating Conditions

Symbol	Parameter	Units	Min.	Max.	Load[pF]	Notes
V_{dd}	Internal operation supply voltage	Volt	2.6	3.0		
V_{ih}	Input voltage logic "1"	Volt	2.0	3.0	6.5	
V_{il}	Input voltage logic "0"	Volt	0	0.8	6.5	
V_{oh}	Output voltage logic "1"	Volt	2.15	3.0	60	
V_{ol}	Output voltage logic "0"	Volt	0.4	0.4	60	
T_a	Ambient operating temperature	Celsius	0	40		

AC Operating Conditions

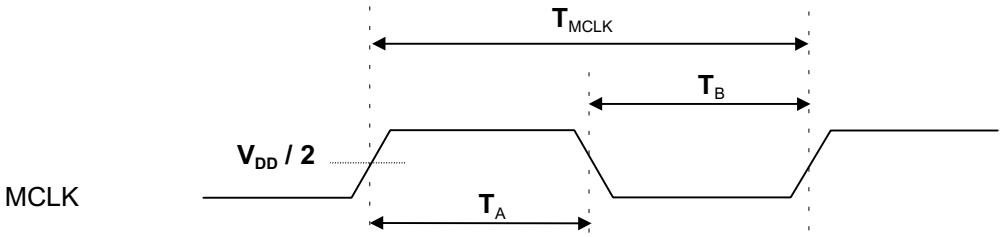
Symbol	Parameter	Max Operation Frequency	Units	Notes
MCLK	Main clock frequency	24	MHz	1
SCK	I^2C clock frequency	400	KHz	2
I_{Normal}	Power Consumption in Normal mode	TBD	mA	
I_{Sleep}	Power Consumption in Sleep mode	TBD	uA	
I_{Down}	Power Consumption in External Power Down mode	TBD	uA	

1. MCLK may be divided by internal clock division logic for easy integration with high-speed video codec.

2. SCK is driven by host processor. For the detail serial bus timing, refer to I2C chip interface section

Input AC Characteristics

MCLK Duty Cycle

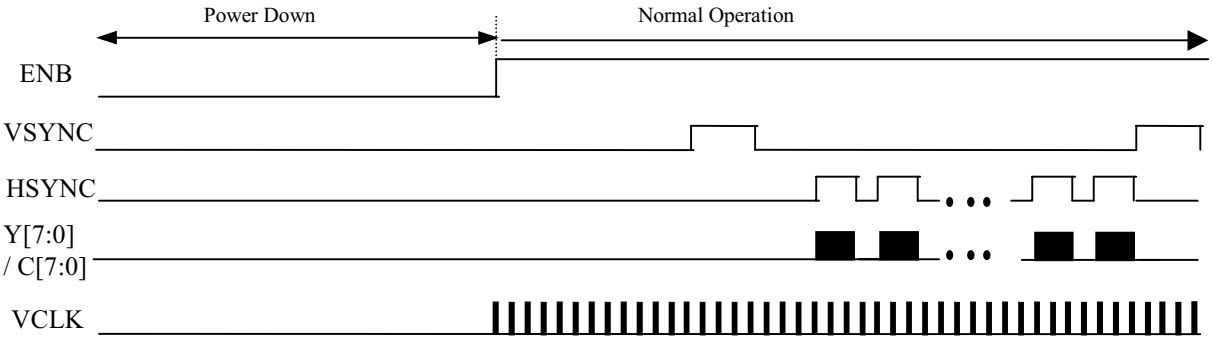


T_A = 40% ~ 60% of T_{MCLK}, T_B = 40% ~ 60% of T_{MCLK} , $T_A + T_B = T_{MCLK}$

Power Down (ENB) Timing

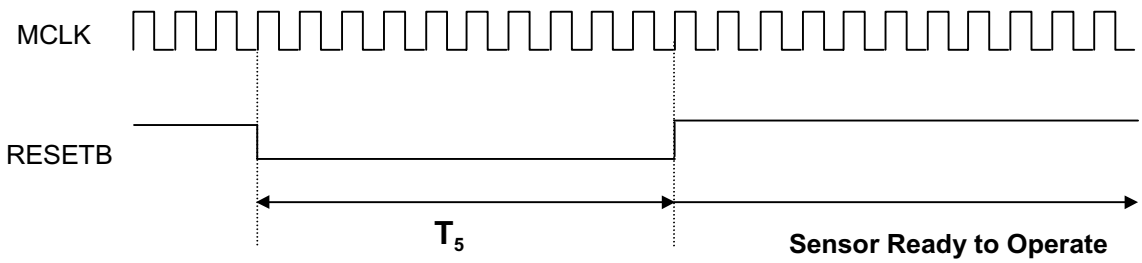
ENB pin enables sensor. When ENB pin is low, sensor goes to power down. All register values are set to initial values when ENB go to high. Power down current is under 50uA.

If you want software power sleep with ENB pin high, set sleep mode in SCTRA(01H)register. Then, all register values are preserved and power sleep current is under 1mA on power sleep mode.



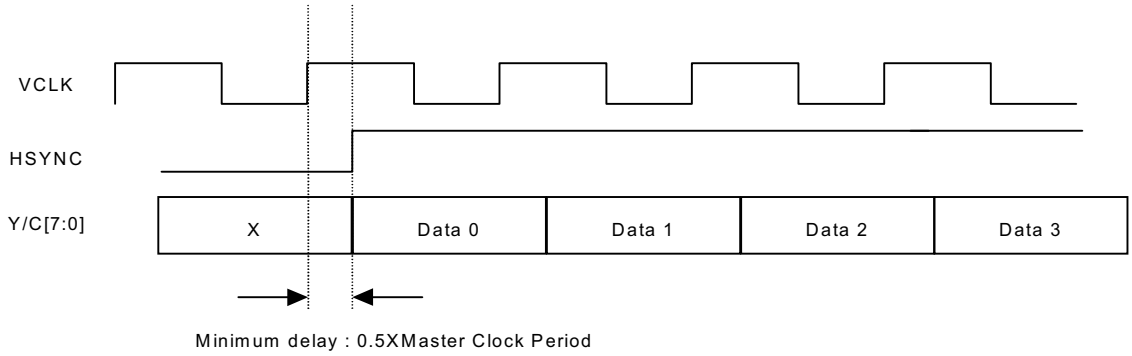
RESETB Timing

RESETB pin initializes the registers to default value. When RESETB pin is low, initialization is done. We recommend to initialize the registers by using RESETB pin before operating sensor. T_5: RESETB valid minimum time: 10 MCLK periods.



Output AC Characteristics

All output timing delays are measured with output load 60[pF]. Output delay includes the internal clock path delay and output driving delay that changes in respect to the output load, the operating environment, and a board design. Due to the variable valid time delay of the output, video output signals Y[7:0], C[7:0], HSYNC, and VSYNC may be latched in the negative edge of VCLK for the stable data transfer between the image sensor and video codec.



Electro-Optical Characteristics

Parameter	Units	Min.	Typical	Max.	Note
Sensitivity	mV / lux·sec		1500		For G
Dark Signal	mV/lux·sec		200		
Dark Shading	mV/sec		TBD		
Output Signal Shading	%		60		
Output Saturation Signal	mV		1000		
Power Consumption (Normal Mode)	mW				

Soldering

Infrared(IR) / Convection solder reflow condition

Parameter	Units	Min.	Typical	Max.	Note
Peak Temperature Range	Celsius	-	230	240	1)

Note: 1) Time within 5 Celsius of actual peak temperature, 10sec

Pad Coordination & Information

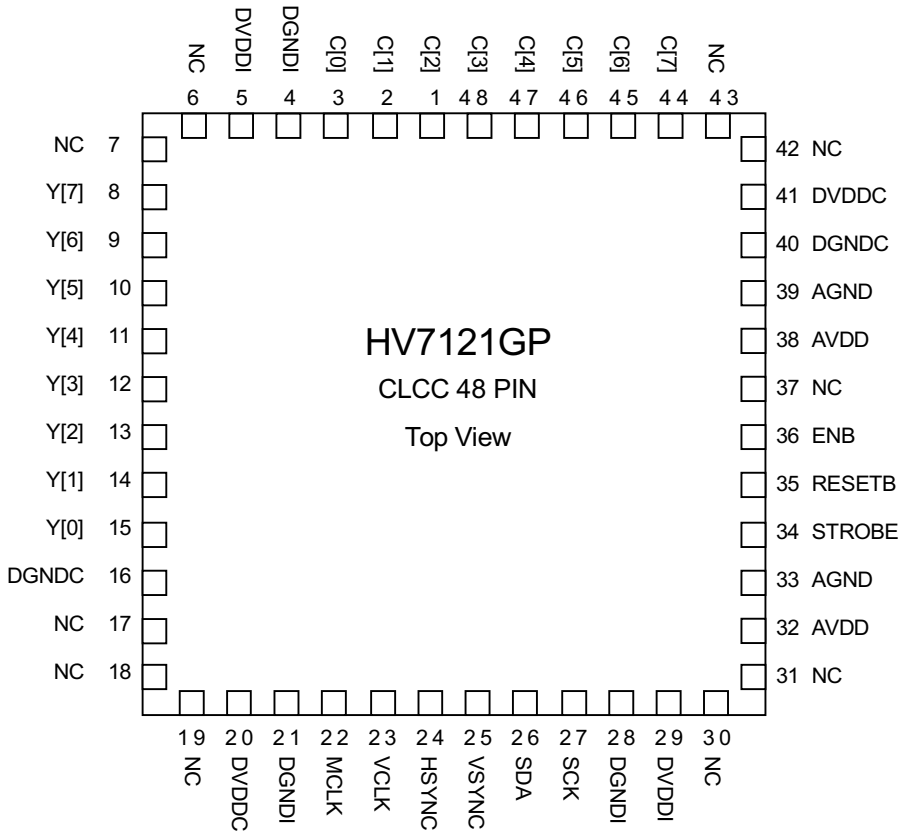
Origin :	Left-Bottom of Chip
Chip Size (Scribe Line Included) :	5730.00 x 4355.00
Pixel Array Center :	2859.7 , 2162.75
Left-Bottom Point of Pixel Array:	1846.1 , 1328.35
Right-Top Point of Pixel Array:	3873.3 , 2997.15

Pin No	Name	Center_X	Center_Y
@Left Lower			
1	Y[7]	225.65	3705.1
2	Y[6]	225.65	3292.1
3	Y[5]	225.65	2879.1
4	Y[4]	225.65	2466.1
5	Y[3]	225.65	2053.1
6	Y[2]	225.65	1640.1
7	Y[1]	225.65	1227.1
8	Y[0]	225.65	814.1
9	DGND	305.35	513.55
@Bottom Righter			
10	DVDD	748.85	307.35
11	GND:IO	1195.15	224.25
12	GND:IO	1320.95	224.25
13	MCLK	1673.8	227.75
14	VCLK	2133.6	227.75
15	HSYNC	2593.1	227.75
16	VSYNC	3052.6	227.75
17	SDA	3520.15	227.75
18	SCK	4048.25	227.7
19	GND:IO	4414.95	224.25
20	VDD:IO	4840.75	252
@Right Upper			
21	AVDD	5401.85	536
22	AGND	5401.85	940.4
23	AGND	5401.85	1078.45
24	STROBE	5503.15	1539.85
25	RESETB	5503.15	1975
26	ENV	5503.15	2410.15
27	AVDD	5401.5	2838.6
28	AVDD	5401.5	2989.45
29	AGND	5401.5	3393.85
30	DGND	5423.55	3623.7
31	DVDD	5423.55	3823.6
@Top Lefter			
32	C[7]	5014.35	4129
33	C[6]	4510.95	4129
34	C[5]	4007.55	4129
35	C[4]	3504.15	4129
36	C[3]	3000.75	4129
37	C[2]	2497.35	4129
38	C[1]	1993.95	4129
39	C[0]	1490.55	4129
40	GND:IO	1154.45	4132.5
41	VDD:IO	728.65	4104.75

Left Pad Count :	9
Bottom Pad Count :	11
Right Pad Count :	11
Top Pad Count :	10
Total Pad Count :	41

note) Pin number 11&12, 22&23, 27&28 are double-bonding pads respectively

CLCC 48Pin Diagram

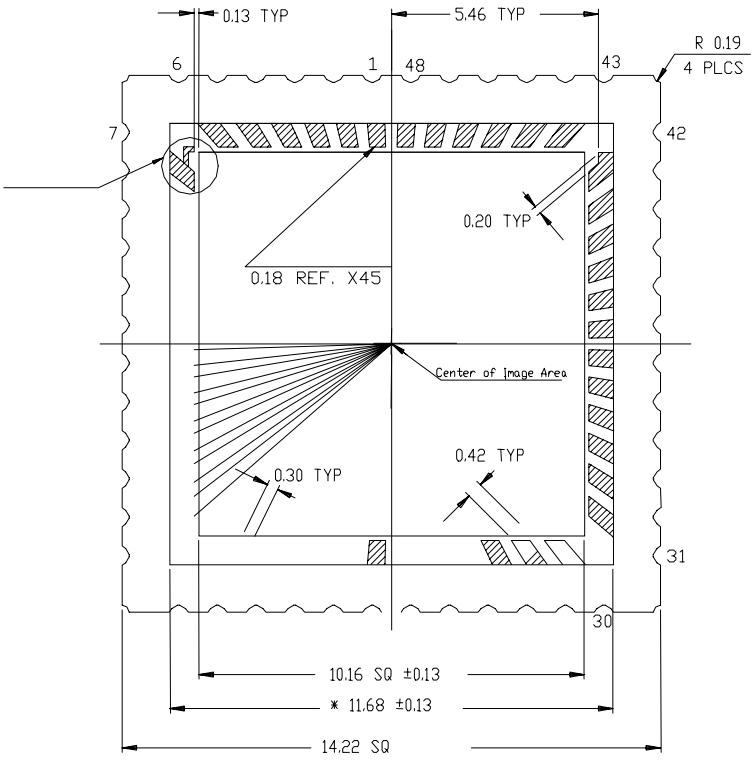


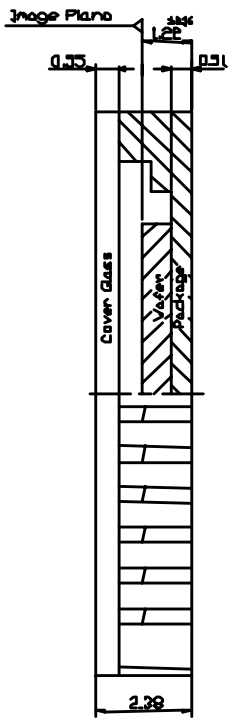
CLCC 48Pin Description

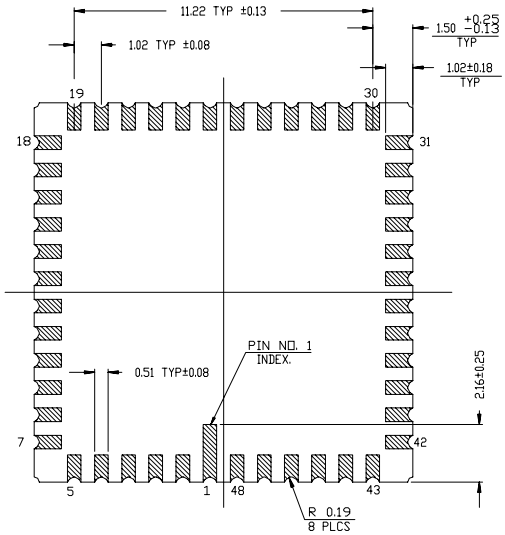
The input mode of C[7:0] is used to test internal image processing function in mass production so that it should be not used as input pin for normal operation. And we recommend C[7:0] pin as pull-up /down when user selects 8bit mode.

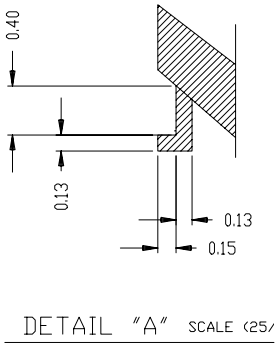
Pin	Type	Symbol	Description
1	B	C[2]	Video Chrominance Data[2].
2	B	C[1]	Video Chrominance Data[1].
3	B	C[0]	Video Chrominance Data[0].
4	G	DGNDI	Digital Ground for I/O Buffer.
5	P	DVDDI	Digital Power for I/O Buffer.
6,7	N	NC	No Connection.
8	O	Y[7]	Video Luminance Data[7].
9	O	Y[6]	Video Luminance Data[6].
10	O	Y[5]	Video Luminance Data[5].
11	O	Y[4]	Video Luminance Data[4].
12	O	Y[3]	Video Luminance Data[3].
13	O	Y[2]	Video Luminance Data[2].
14	O	Y[1]	Video Luminance Data[1].
15	O	Y[0]	Video Luminance Data[0].
16	G	DGNDC	Ground for Internal Digital Block.
17,18,19	N	NC	No Connection.
20	P	DVDDC	Power for Internal Digital Block.
21	G	DGNDI	Digital Ground for I/O Buffer.
22	I	MCLK	Master Input Clock.
23	O	VCLK	Video Output Clock.
24	O	HSYNC	Video Horizontal Line Synchronization signal. / Data is valid, when HSYNC is active.
25	O	VSYNC	Video Frame Synchronization signal. / Frame Start output VSYNC is active at start of image data frame.
26	B	SDA	I2C Standard data I/O port
27	I	SCK	I2C Clock Input.
28	G	DGNDI	Digital Ground for I/O Buffer.
29	P	DVDDI	Digital Power for I/O Buffer.
30,31	N	NC	No Connection.
32	P	AVDD	Power for Analog Block.
33	G	AGND	Ground for Analog Block.
34	O	STROBE	Strobe Signal Output.
35	I	RESETB	Sensor Reset, Low Active.
36	I	ENB	ENB signal enables Sensor : High(Sensor Enabled), Low(Sensor Disabled, External Power Down)
37	N	NC	No Connection.
38	P	AVDD	Power for Analog Block.
39	G	AGND	Ground for Analog Block.
40	G	DGNDC	Ground for Internal Digital Block.
41	P	DVDDC	Power for Internal Digital Block.
42,43	N	NC	No Connection.
44	B	C[7]	Video Chrominance Data[7].
45	B	C[6]	Video Chrominance Data[6].
46	B	C[5]	Video Chrominance Data[5].
47	B	C[4]	Video Chrominance Data[4].
48	B	C[3]	Video Chrominance Data[3].

CLCC 48Pin Package Specification









DETAIL "A" SCALE (25/

MEMO

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