

DESCRIPTION

The HY514170 is the new generation and fast dynamic RAM organized 262,144 x 16-bit configuration employing advanced submicron CMOS process technology and advanced circuit design technique to achieve fast access time. Independent write of upper and lower byte is controlled by 2 separate WE inputs. Refresh control is provided through RAS-only, CAS-before-RAS, hidden refresh and self refresh modes. The HY514170 conforms to JEDEC pinpoint standards and is available in industry standard 400mil 40pin SOJ and 40/44pin TSOP-II and reverse TSOP-II packages.

FEATURES

- Low power dissipation
 - Max. battery back-up 1.65mW (SL-part)
 - Max. CMOS standby 1.1mW (SL-part)
 - 5.5mW

Max. TTL standby 11.0mW

Max. Self refresh 1.65mW (SL-part)

Max. operating

Speed	Power
60	715.0mW
70	605.0mW
80	522.5mW

- Single power supply of $5V \pm 10\%$
- TTL compatible inputs and outputs
- Fast access time

Speed	t _{TRC}	t _{CAS}	t _{PC}
60	60ns	20ns	40ns
70	70ns	20ns	45ns
80	80ns	20ns	50ns

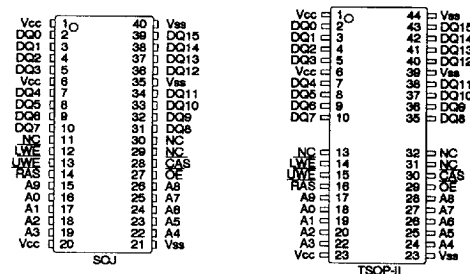
- Fast page mode operation
- 2 WE inputs for upper and lower byte write control
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden refresh and Self refresh
- 1024 refresh cycles / 128ms (SL-part)
- 1024 refresh cycles / 16ms

PIN DESCRIPTION

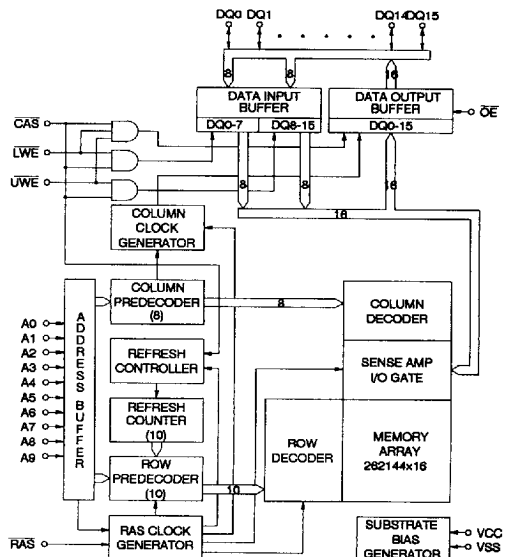
RAS	Row Address Strobe
CAS	Column Address Strobe
LWE, UWE	Write Enable
OE	Output Enable
A0-A9*	Address Input
DQ0-DQ15	Data Input/Output
VCC	Power (+5V)
VSS	Ground

* A8 and A9 are applied to row address input only.

PIN CONNECTION



BLOCK DIAGRAM



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1AC09-00-APR93

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to Vss	-1.0 to 7.0	V
IOS	Short Circuit Output Current	50	mA
Pd	Power Dissipation	1.0	W
TSOLDER	Soldering Temperature•Time	260•10	°C•sec

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC+1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to Vss.

DC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I _{IL}	Input Leakage Current (Any Input Pins)	VSS ≤ V _{IN} ≤ 6.5V, All other pins not under test = VSS		-10	10	μA	
I _{LO}	Output Leakage Current (High Impedance State)	VSS ≤ V _{OUT} ≤ 5.5V, RAS & CAS at V _{IH}		-10	10	μA	
ICC1	VCC Supply Current, Operating	t _{RC} = t _{RC} (min.)	60 70 80	- - -	130 110 95	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at V _{IH} , other inputs ≥ VSS		-	2	mA	
ICC3	VCC Supply Current, RAS-only refresh	t _{RC} = t _{RC} (min.)	60 70 80	- - -	130 110 95	mA	1,3
ICC4	VCC Supply Current, Fast Page mode	t _{PC} = t _{PC} (min.)	60 70 80	- - -	60 50 45	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC - 0.2V	SL-part	-	1 0.2	mA	5
ICC6	VCC Supply Current, CAS-before-RAS refresh	t _{RC} = t _{RC} (min.)	60 70 80	- - -	130 110 95	mA	1,3
ICC7	VCC Supply Current, Battery Back Up (SL-part only)	t _{RC} = 125μs, t _{RAS} ≤ 1μs CAS = CBR cycling or 0.2V OE & WE = VCC - 0.2V, A0-A9 = VCC - 0.2V or 0.2V DQ0-DQ15 = 0.2V, VCC - 0.2V or open		-	300	μA	1,4,5
ICC8	VCC Supply Current, Self refresh (SL-part only)	RAS & CAS ≤ 0.2V other pins same as ICC7		-	300	μA	5
VOL	Output Low Voltage	I _{OL} = 4.2mA		-	0.4	V	
VOH	Output High Voltage	I _{OH} = -5mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rate.
2. ICC1 and ICC4 depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while RAS = V_{IL} and CAS = V_{IH}.
4. Only t_{RAS}(max.) = 1μs is applied to refresh of battery backup but t_{RAS}(max.) = 10μs is applied to normal functional operation.
5. ICC5(max.) = 0.2mA, ICC7 and ICC8 are applied to SL-parts only (HY514170SLJC, HY514170SLTC and HY514170SLRC).

AC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted.) NOTE : 1, 2, 3, 13

#	SYMBOL	PARAMETER	HYS14170JC/TC/RC/SLJC/SLTC/SLRC						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	120	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	175	-	180	-	200	-	ns	
3	tPC	Fast Page Mode Cycle Time	45	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	95	-	95	-	100	-	ns	
5	tRAC	Access Time from RAS	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from CAS	-	20	-	20	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from Column Precharge	-	40	-	40	-	45	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	RAS Precharge Time	50	-	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	RAS Hold Time	20	-	20	-	20	-	ns	
16	tCSH	CAS Hold Time	60	-	70	-	80	-	ns	
17	tCAS	CAS Pulse Width	20	10K	20	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	20	40	20	50	20	55	ns	9
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	50	-	55	-	60	-	ns	
27	tRAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	17
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6,14
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6,14
31	tWCH	Write Command Hold Time	15	-	15	-	15	-	ns	16
32	tWCR	Write Command Hold Time from RAS	50	-	55	-	60	-	ns	16
33	tWP	Write Command Pulse Width	10	-	10	-	10	-	ns	15,16
34	tRWL	Write Command to RAS Lead Time	20	-	20	-	20	-	ns	15
35	tCWL	Write Command to CAS Lead Time	20	-	20	-	20	-	ns	15,18
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7,14
37	tDH	Data-In Hold Time	15	-	15	-	15	-	ns	7,15
38	tDHR	Data-In Hold Time Referenced to RAS	50	-	55	-	60	-	ns	
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	-	16	ms	
		SL-part	-	128	-	128	-	128		11
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8,15

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY514170JC/TC/RC/SLJC/SLTC/SLRC						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	45	-	45	-	45	-	ns	8,14
42	tRWD	RAS to WE Delay Time	85	-	95	-	105	-	ns	8,14
43	tAWD	Column Address to WE Delay Time	55	-	60	-	65	-	ns	8,14
44	tCSR	CAS Set-up Time (CBR Cycle)	10	-	10	-	10	-	ns	
45	tCHR	CAS Hold Time (CBR Cycle)	15	-	15	-	15	-	ns	
46	tRPC	RAS to CAS Precharge Time	10	-	10	-	10	-	ns	
47	tCPT	CAS Precharge Time (CBR Counter Test)	20	-	20	-	20	-	ns	
48	tROH	RAS Hold Time Reference to OE	10	-	10	-	10	-	ns	
49	tOEA	OE Access Time	0	20	0	20	0	20	ns	
50	tOED	OE to Data Delay	20	-	20	-	20	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from OE	0	15	0	15	0	15	ns	5
52	tOEH	OE Command Hold Time	20	-	20	-	20	-	ns	15
53	tCPWD	WE Delay Time from CAS Precharge	60	-	65	-	70	-	ns	8
54	tRHCP	RAS Hold Time from CAS Precharge	30	-	35	-	35	-	ns	
55	tRASS	RAS Pulse Width (Self Refresh)	100	-	100	-	100	-	μs	
56	tRPS	RAS Precharge Time (Self Refresh)	120	-	130	-	150	-	ns	
57	tCHS	CAS Hold Time from RAS (Self Refresh)	-50	-	-50	-	-50	-	ns	

NOTE :

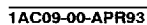
1. An initial pause of 200 μ s is required after power-up followed by 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode during initialization.
2. AC measurements assume $t_T = 5$ ns.
3. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
4. Measured at $V_{OH} = 2.4$ V and $V_{OL} = 0.4$ V with a load equivalent to 2 TTL loads and 100pF.
5. $t_{OFF}(\text{max.})$ and t_{OEZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles and to LWE or UWE leading edge in Read-Modify-Write cycles.
8. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$, $t_{AWD} \geq t_{AWD}(\text{min.})$, and $t_{CPWD} \geq t_{CPWD}(\text{min.})$, the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
10. Operation within the $t_{RAD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
11. $t_{REF}(\text{max.}) = 128$ ms is applied to SL-parts only (HY514170SLJC, HY514170SLTC and HY514170SLRC).
12. A burst of 1024 CAS-before-RAS refresh cycles must be executed within 16ms (128ms for SL-part) after exiting Self refresh.
13. When both LWE and UWE go low at the same time, all 16-bits data are written into the device. LWE and UWE must be transitioned simultaneously within a same read or write cycle.
14. These parameters are determined by the earlier falling edge of LWE or UWE.
15. These parameters are determined by the later falling edge of LWE or UWE.
16. These parameters are determined by the earlier rising edge of LWE or UWE.
17. These parameters are determined by the later rising edge of LWE or UWE.
18. t_{CWL} must be satisfied by both LWE and UWE for 16-bits access cycles.

CAPACITANCE

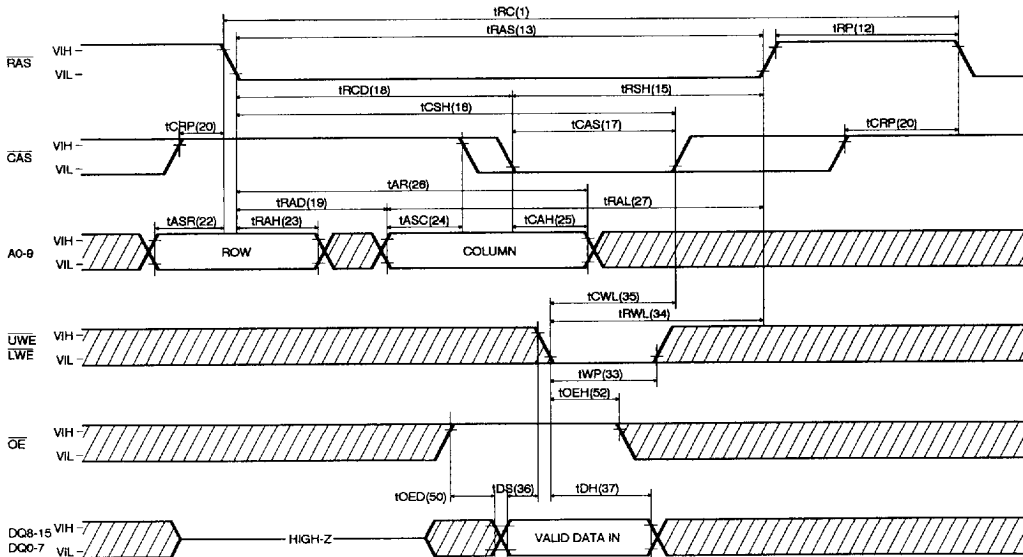
($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, $f = 1\text{MHz}$, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A9)	-	5	pF
CIN2	Input Capacitance (RAS, CAS, WE, OE)	-	7	pF
CDQ	Data Input/Output Capacitance (DQ0-DQ15)	-	7	pF

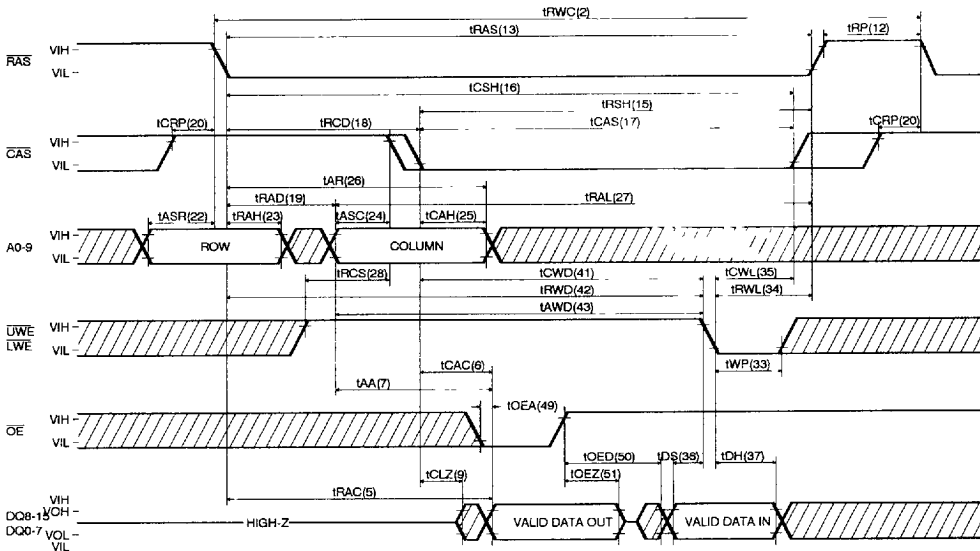
READ CYCLE



WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



READ-MODIFY-WRITE CYCLE



The timing diagram illustrates the sequence of signals for three memory accesses. The signals shown are:

- RAS**: Row Address Strobe, active low.
- CAS**: Column Address Strobe, active low.
- A0-A9**: Address bus, where bits 0-8 indicate ROW and bit 9 indicates COLUMN.
- LWE**: Low Enable, active low.
- OE**: Output Enable, active low.
- DQ0-15**: Data bus, which goes into HIGH-Z during valid data output periods.

Key timing parameters labeled include:

- $t_{RASP}(14)$, $t_{RP}(12)$
- $t_{CRP}(20)$, $t_{CSH}(16)$, $t_{ICSH}(17)$, $t_{ICD}(18)$, $t_{CAS}(17)$, $t_{CP}(21)$, $t_{PC}(3)$, $t_{RHCP}(54)$, $t_{RSH}(15)$, $t_{CAS}(17)$
- $t_{AR}(26)$, $t_{RAD}(19)$, $t_{ASC}(24)$, $t_{CAH}(25)$, $t_{ASC}(24)$, $t_{CAH}(25)$, $t_{ASC}(24)$, $t_{CAH}(25)$, $t_{RAL}(27)$
- $t_{ASR}(22)$, $t_{RAS}(28)$, $t_{ACH}(29)$, $t_{AA}(7)$, $t_{RCH}(29)$, $t_{RCS}(28)$, $t_{IRCH}(29)$, $t_{RRH}(30)$, $t_{FCH}(29)$
- $t_{FAC}(5)$, $t_{CAC}(6)$, $t_{IOEA}(49)$, $t_{CPA}(8)$, $t_{OFF}(10)$, $t_{OEZ}(51)$, $t_{CLZ}(9)$

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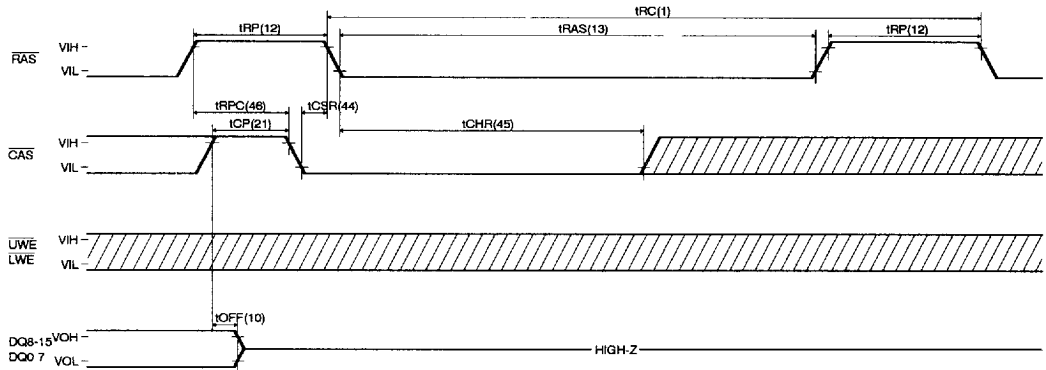
[illegible]

The diagram illustrates the timing relationships for RAS, CAS, and AO-B signals. The signals are shown as active-low waveforms. The timing parameters are defined as follows:

- $t_{RC}(1)$: RAS to CAS delay
- $t_{RAS}(13)$: RAS to CAS delay
- $t_{RP}(12)$: RAS to CAS delay
- $t_{CRP}(20)$: RAS to CAS delay
- $t_{RPC}(48)$: RAS to CAS delay
- $t_{ASR}(22)$: RAS to CAS delay
- $t_{RAH}(23)$: RAS to CAS delay

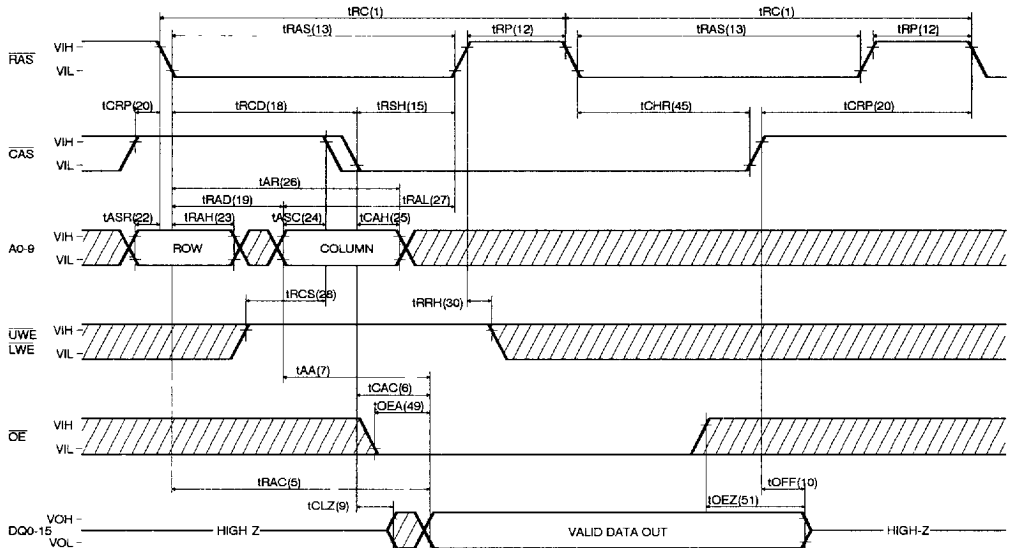
NOTE , OE and WE = "H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE

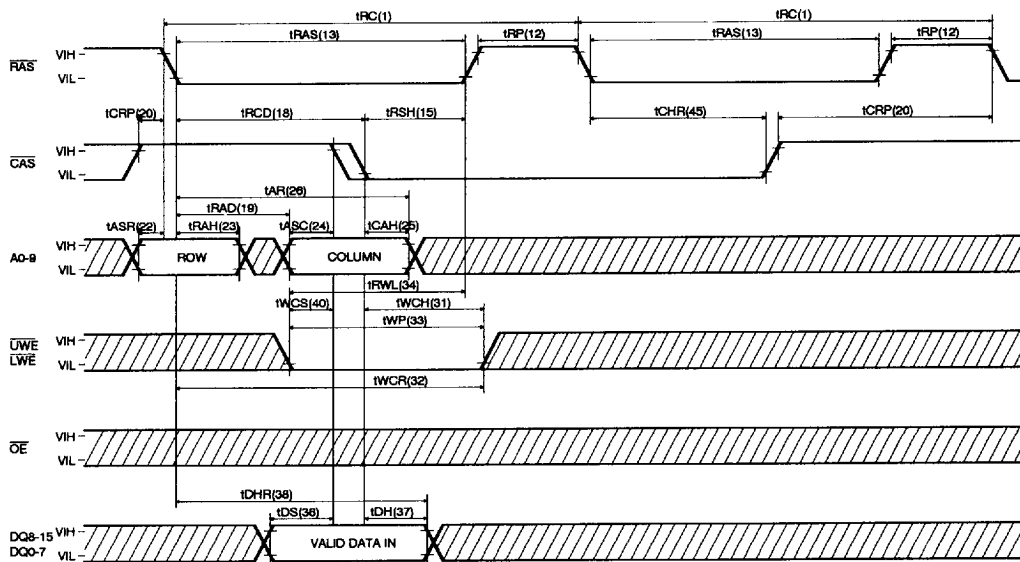


NOTE : A0-9 and OE = "H" or "L"

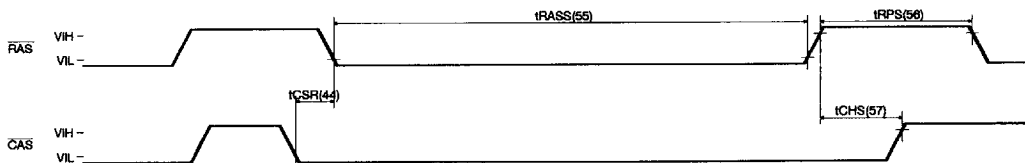
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

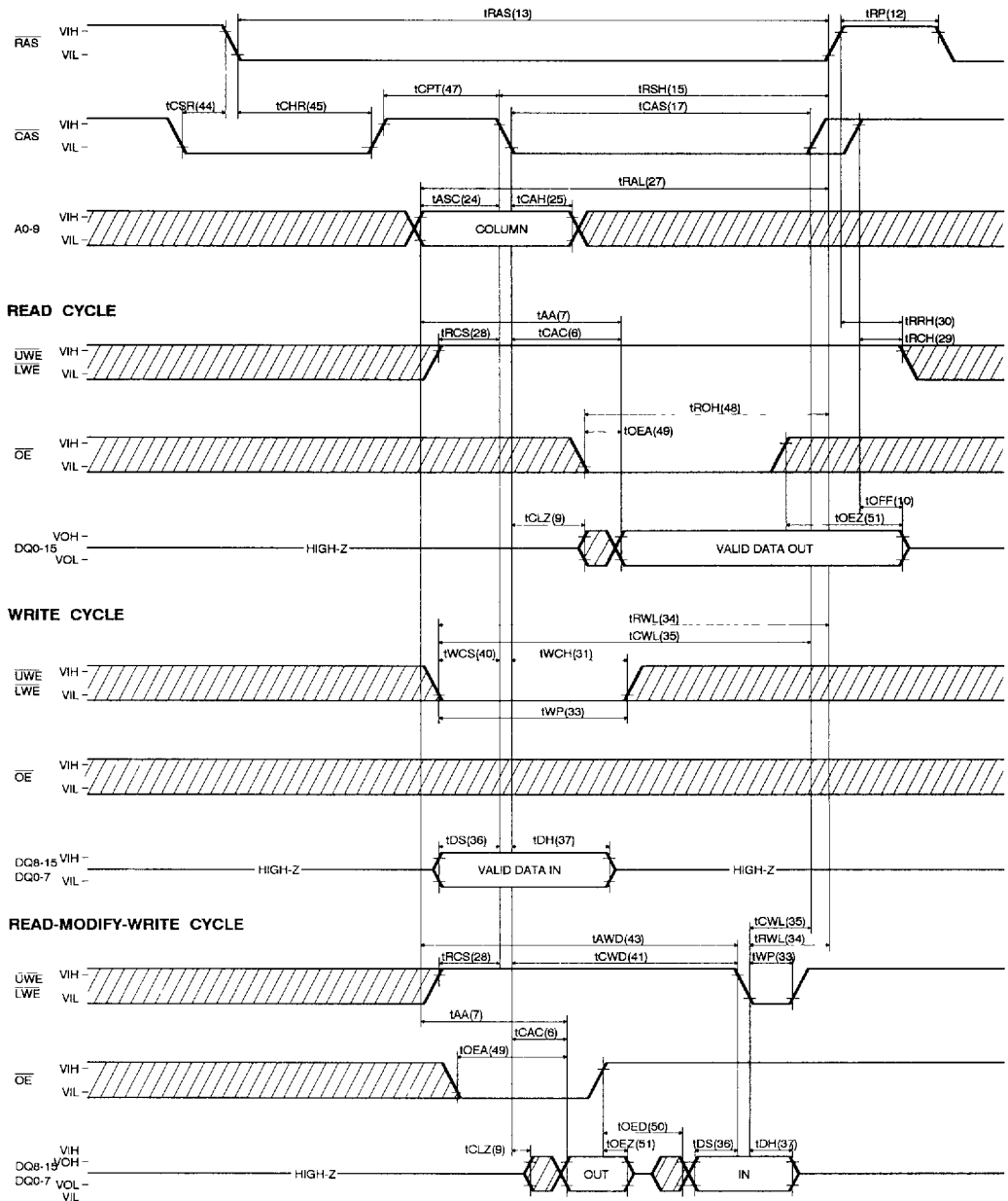


CAS-BEFORE-RAS SELF REFRESH CYCLE



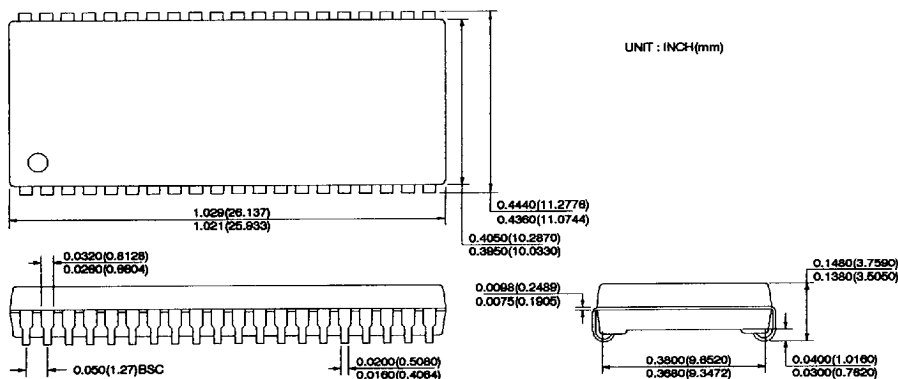
NOTE : A0-9, WE and OE = "H" or "L"

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

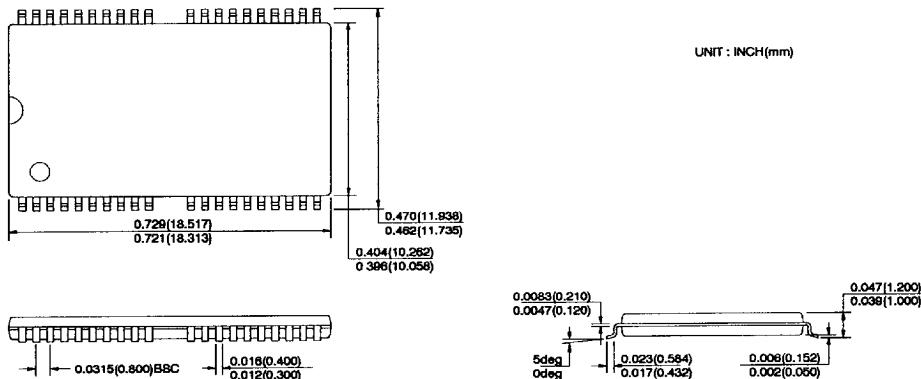


PACKAGE INFORMATION

400 mil 40 pin Small Outline J-form Package (JC)



400 mil 40/44 pin Thin Small Outline Package (TC) (RC)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE
HY514170JC	60/70/80		SOJ
HY514170SLJC	60/70/80	SL-part	SOJ
HY514170TC	60/70/80		TSOP-II
HY514170SLTC	60/70/80	SL-part	TSOP-II
HY514170RC	60/70/80		TSOP-II(R)
HY514170SLRC	60/70/80	SL-part	TSOP-II(R)