

384-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 256-GRAY SCALES)

The μ PD16742 is a source driver for TFT-LCDs capable of dealing with displays with 256 gray scales. Data input is based on digital input configured as 8 bits by 6 dots (2 pixels), which can realize a full-color display of 16,777,216 colors by output of 256 values γ -corrected by an internal D/A converter and 11 external power modules. Because the output dynamic range is as large as $V_{SS2} + 0.1$ V to $V_{DD2} - 0.1$ V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 8-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. The D/A converter, which incorporates a digital offset circuit, is suitable for an LCD panel in which liquid crystal transmittance in positive and negative polarities is different. Assuring a maximum clock frequency of 65 MHz when driving at 3.0 V, this driver is applicable to SXGA and XGA-standard TFT-LCD panels.

FEATURES

- CMOS level input
- 384-output channel
- Input of 8 bits (gradation data) by 6 dots
- Capable of outputting 256 values by means of 11 external power modules and a D/A converter (C-DAC)
- Output dynamic range $V_{SS2} + 0.1$ V to $V_{DD2} - 0.1$ V
- High-speed data transfer: $f_{MAX.} = 65$ MHz (internal data transfer speed when operating at $V_{DD1} = 3.0$ V)
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output voltage polarity reverse is possible (POLA)
- Input data reverse function is incorporated (POLB (O/E))
- Output offset for different eight values can be controlled by offset signals (three signals)
- Logic Part Power Supply Voltage (V_{DD1}) : 3.3 ± 0.3 V
- Driver Part Power Supply Voltage (V_{DD2}) : 9.0 ± 0.5 V

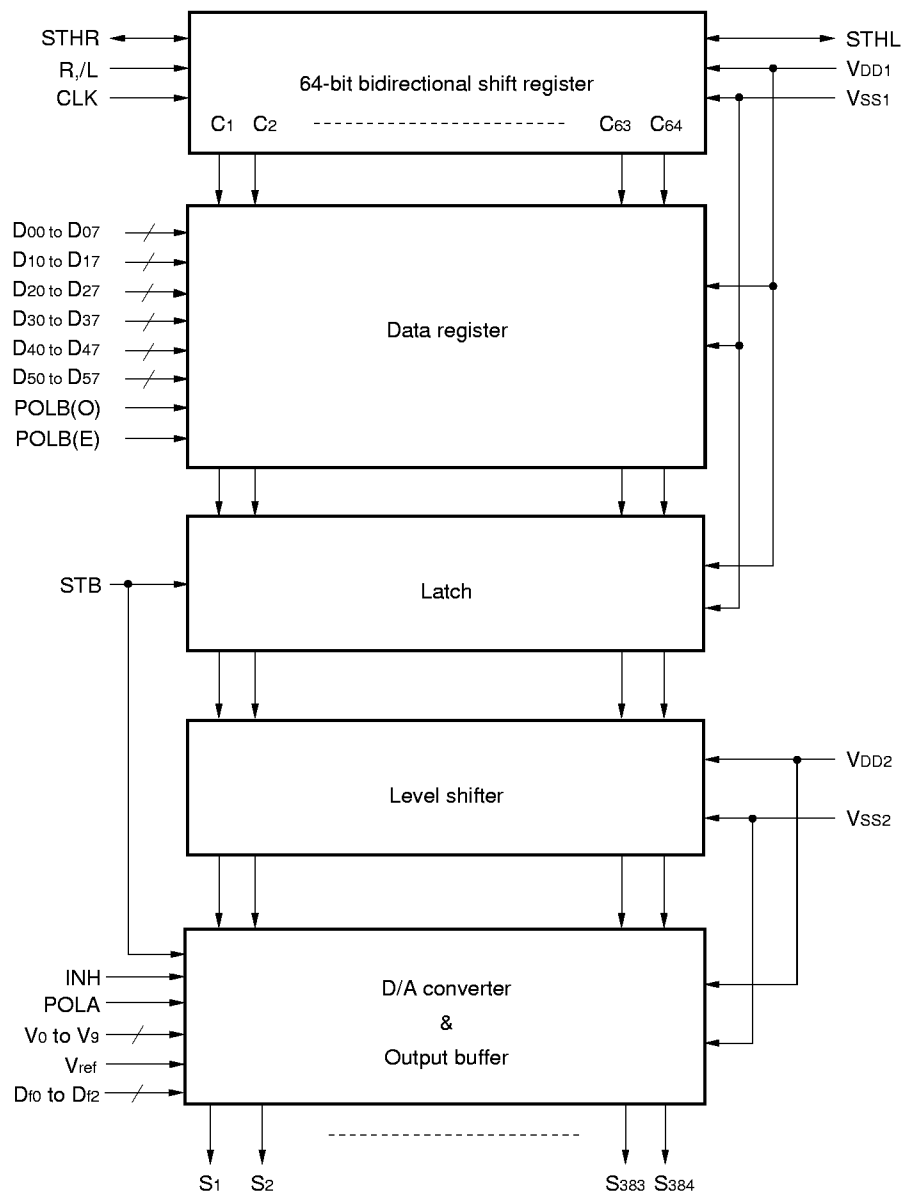
ORDERING INFORMATION

Part Number	Package
μ PD16742N-xxx	TCP (TAB package)

Remark The TCP's external shape is custom-order item. Users are requested to consult with a NEC sales representative.

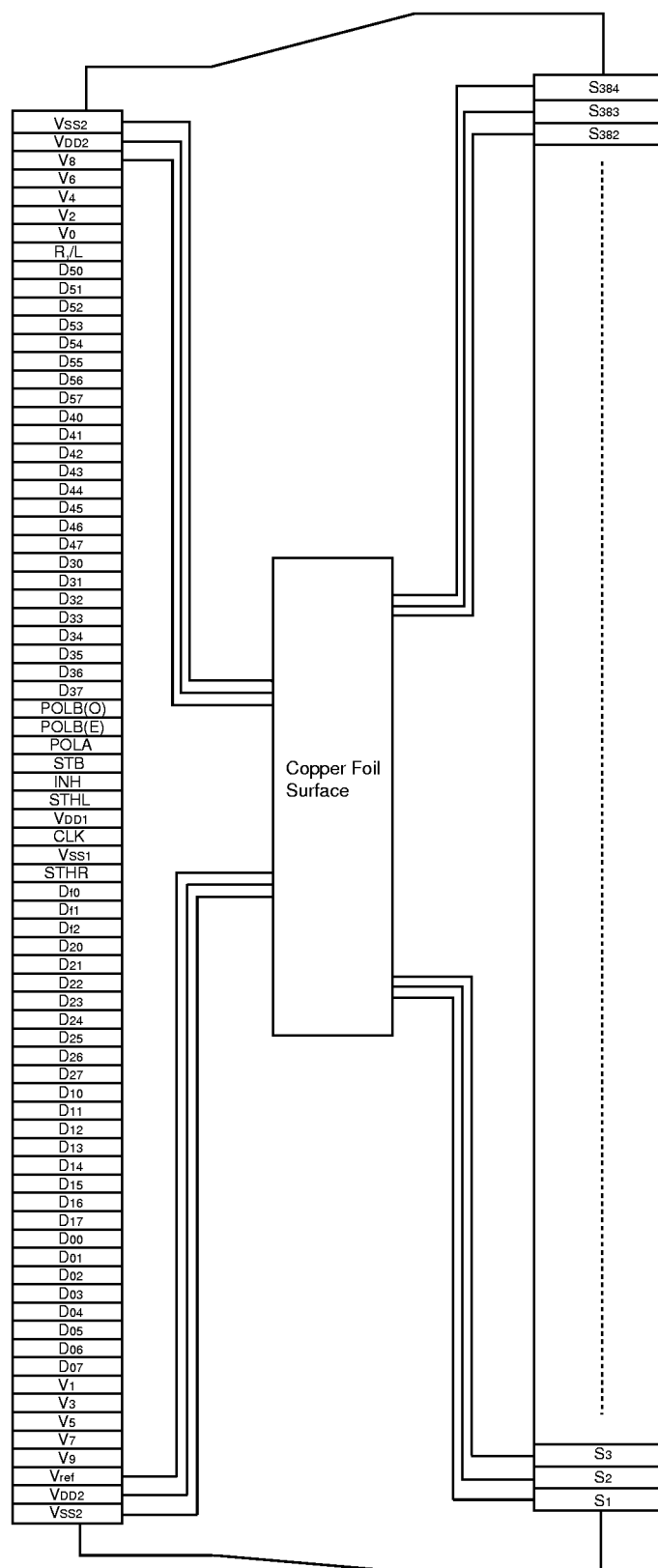
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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

1. BLOCK DIAGRAM



Remark /xxx indicates active low signal.

2. PIN CONFIGURATION (μ PD16742N-xxx)



Remark This figure does not specify the TCP package.

3. PIN FUNCTIONS

Pin Symbol	Pin Name	Description
S ₁ to S ₃₈₄	Driver output	The D/A converted 256-gray-scale analog voltage is output.
D ₀₀ to D ₀₇	Display data input	The display data is input with a width of 48 bits, viz., the gray scale data (8 bits) by 6 dots (2 pixels). 8-bit input : D _{x0} : LSB, D _{x7} : MSB
D ₁₀ to D ₁₇		
D ₂₀ to D ₂₇		
D ₃₀ to D ₃₇		
D ₄₀ to D ₄₇		
D ₅₀ to D ₅₇		
R _i /L	Shift direction control input	These refer to the start pulse input/output pins when driver ICs are connected in cascade. The shift directions of the shift registers are as follows. R _i /L = H (Right shift) : STHR (input) → S ₁ → S ₃₈₄ → STHL (output) R _i /L = L (Left shift) : STHL (input) → S ₃₈₄ → S ₁ → STHR (output)
STHR	Right shift start pulse input/output	Start pulse I/O pin at cascade connection. The display data is acquired when the high level is read at the rising edge of CLK. Right shift : STHR is input. STHL is output. Left shift : STHL is input. STHR is output.
STHL	Left shift start pulse input/output	
CLK	Shift clock input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 64th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. Start pulse high level is read at rising edge of CLK, start to load the display data from next rising edge of CLK. Also, after start pulse input and CLK input 66 pulses, it stops to load the display data and it makes contents of shift register clear at rising edge of STB.
STB	Latch input	After the contents of data register is transferred to a latch at a rising edge and is cleared, operation of analog output voltage for output voltage is started.
INH	Inhibit input	At the falling edge complete calculation of analog output voltage, and output the voltage appointed by display data.
POLA	Polarity input	This signal is read at the rising edge of latch signal and determines the output voltage polarity to reference voltage of each output pin. POLA = L : Pins with even number are negative output. Pins with odd number are positive output. POLA = H : Pins with even number are positive output. Pins with odd number are negative output.
POLB(O) POLB(E)	Data inversion	By inputting a switching signal to this pin, this pin enables the data whose polarity is reversed to be read. POLB(O) and POLB(E) are a data reverse control pin for D _{0x} to D _{2x} and D _{3x} to D _{5x} , respectively. POLB(O/E) = H : Acquires with displayed data reversed POLB(O/E) = L : Acquires raw displayed data
V _{ref}	Reference power supply	This terminal is the input reference power supply need to calculation output. Please refer to 4. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE.
V ₀ to V ₉	γ-corrected power supplies	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. $V_{ref} - 0.1\text{ V} \geq V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_6 \geq V_7 \geq V_8 \geq V_9 \geq V_{SS2} + 0.1\text{ V}$ $V_{ref} - 0.1\text{ V} \geq V_9 \geq V_8 \geq V_7 \geq V_6 \geq V_5 \geq V_4 \geq V_3 \geq V_2 \geq V_1 \geq V_0 \geq V_{SS2} + 0.1\text{ V}$ During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level.
D ₁₀ to D ₁₂	Offset control	This pin determines offset voltage. For the offset voltage for each input data, refer to 8. OFFSET VOLTAGE.
V _{DD1}	Logic power supply	3.3 V ± 0.3 V
V _{DD2}	Driver power supply	9.0 V ± 0.5 V
V _{SS1}	Logic ground	Grounding
V _{SS2}	Driver ground	Grounding

- Cautions**
1. The power start sequence must be $V_{DD1} \rightarrow$ logic input (High or Low) $\rightarrow V_{DD2} \rightarrow V_{ref} \rightarrow V_0$ to V_9 in that order. Reverse this sequence to shut down. Be sure to observe this power sequence even during a transition period.
 2. To stabilize the supply voltage, please be sure to insert each $0.1 \mu F$, $0.47 \mu F$ bypass capacitor between $V_{DD1}-V_{SS1}$ and $V_{DD2}-V_{SS2}$. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about $0.01 \mu F$ is also advised between the γ -corrected power supply terminals (V_0 to V_9) and V_{SS2} .
 3. We recommend to use Operational Amplifier to lower input impedance of “ γ -corrected voltage” and “ γ -corrected reference power supply ” input terminal. Please input this terminal stabilized voltage . In case of input high impedance switching signals, applied voltage to this terminal is getting to instability, and may not be correctly displayed.

4. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

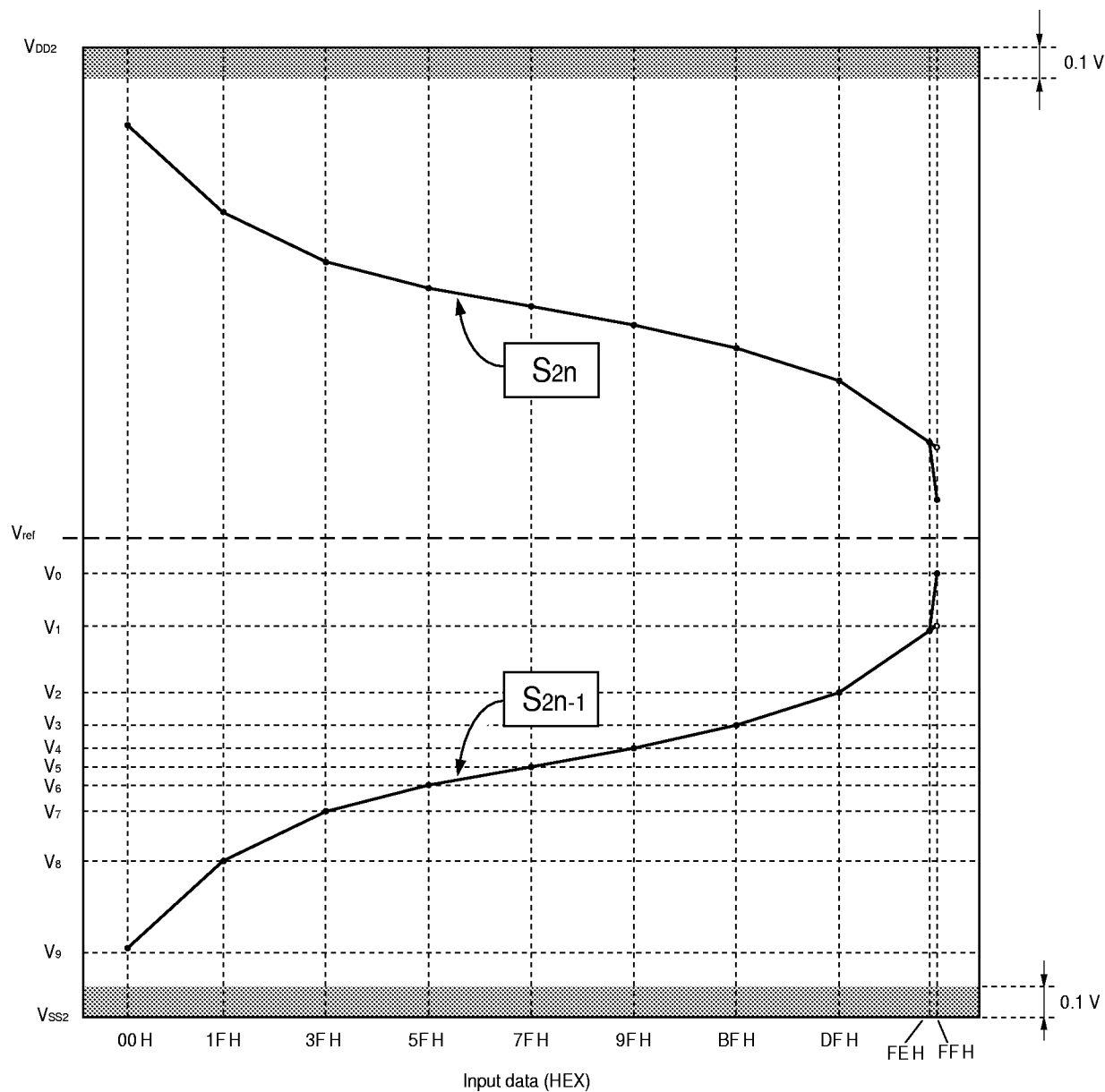
4.1 Calculation of output voltage in 8-bit input

$$(V_{\text{ref}} - 0.1 \text{ V} \geq V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_6 \geq V_7 \geq V_8 \geq V_{\text{SS2}} + 0.1 \text{ V})$$

Gray Scale	Binary	Input Data								Output Voltage	
		D _{X7}	D _{X6}	D _{X5}	D _{X4}	D _{X3}	D _{X2}	D _{X1}	D _{X0}	S _{2n} (POLA=H), S _{2n-1} (POLA=L)	S _{2n-1} (POLA=H), S _{2n} (POLA=L)
0	00H	0	0	0	0	0	0	0	0	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_8 + (V_9 - V_8) \times 31/32\}$	$V_8 + (V_9 - V_8) \times 31/32$
1	01H	0	0	0	0	0	0	1	1	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_8 + (V_9 - V_8) \times 30/32\}$	$V_8 + (V_9 - V_8) \times 30/32$
⋮	⋮				⋮					⋮	⋮
30	1EH	0	0	0	1	1	1	1	0	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_8 + (V_9 - V_8) \times 1/32\}$	$V_8 + (V_9 - V_8) \times 1/32$
31	1FH	0	0	0	1	1	1	1	1	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times V_8$	V_8
32	20H	0	0	1	0	0	0	0	0	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_7 + (V_8 - V_7) \times 31/32\}$	$V_7 + (V_8 - V_7) \times 31/32$
33	21H	0	0	1	0	0	0	1	1	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_7 + (V_8 - V_7) \times 30/32\}$	$V_7 + (V_8 - V_7) \times 30/32$
⋮	⋮				⋮					⋮	⋮
62	3EH	0	0	1	1	1	1	1	0	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_7 + (V_8 - V_7) \times 1/32\}$	$V_7 + (V_8 - V_7) \times 1/32$
63	3FH	0	0	1	1	1	1	1	1	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times V_7$	V_7
64	40H	0	1	0	0	0	0	0	0	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_6 + (V_7 - V_6) \times 31/32\}$	$V_6 + (V_7 - V_6) \times 31/32$
65	41H	0	1	0	0	0	0	1	1	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_6 + (V_7 - V_6) \times 30/32\}$	$V_6 + (V_7 - V_6) \times 30/32$
⋮	⋮				⋮					⋮	⋮
94	5EH	0	1	0	1	1	1	1	0	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_6 + (V_7 - V_6) \times 1/32\}$	$V_6 + (V_7 - V_6) \times 1/32$
95	5FH	0	1	0	1	1	1	1	1	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times V_6$	V_6
96	60H	0	1	1	0	0	0	0	0	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_5 + (V_6 - V_5) \times 31/32\}$	$V_5 + (V_6 - V_5) \times 31/32$
97	61H	0	1	1	0	0	0	1	1	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_5 + (V_6 - V_5) \times 30/32\}$	$V_5 + (V_6 - V_5) \times 30/32$
⋮	⋮				⋮					⋮	⋮
126	7EH	0	1	1	1	1	1	1	0	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_5 + (V_6 - V_5) \times 1/32\}$	$V_5 + (V_6 - V_5) \times 1/32$
127	7FH	0	1	1	1	1	1	1	1	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times V_5$	V_5
128	80H	1	0	0	0	0	0	0	0	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_4 + (V_5 - V_4) \times 31/32\}$	$V_4 + (V_5 - V_4) \times 31/32$
129	81H	1	0	0	0	0	0	1	1	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_4 + (V_5 - V_4) \times 30/32\}$	$V_4 + (V_5 - V_4) \times 30/32$
⋮	⋮				⋮					⋮	⋮
158	9EH	1	0	0	1	1	1	1	0	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_4 + (V_5 - V_4) \times 1/32\}$	$V_4 + (V_5 - V_4) \times 1/32$
159	9FH	1	0	0	1	1	1	1	1	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times V_4$	V_4
160	A0H	1	0	1	0	0	0	0	0	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_3 + (V_4 - V_3) \times 31/32\}$	$V_3 + (V_4 - V_3) \times 31/32$
161	A1H	1	0	1	0	0	0	1	1	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_3 + (V_4 - V_3) \times 30/32\}$	$V_3 + (V_4 - V_3) \times 30/32$
⋮	⋮				⋮					⋮	⋮
190	BEH	1	0	1	1	1	1	1	0	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_3 + (V_4 - V_3) \times 1/32\}$	$V_3 + (V_4 - V_3) \times 1/32$
191	BFH	1	0	1	1	1	1	1	1	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times V_3$	V_3
192	C0H	1	1	0	0	0	0	0	0	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_2 + (V_3 - V_2) \times 31/32\}$	$V_2 + (V_3 - V_2) \times 31/32$
193	C1H	1	1	0	0	0	0	1	1	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_2 + (V_3 - V_2) \times 30/32\}$	$V_2 + (V_3 - V_2) \times 30/32$
⋮	⋮				⋮					⋮	⋮
222	DEH	1	1	0	1	1	1	1	0	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_2 + (V_3 - V_2) \times 1/32\}$	$V_2 + (V_3 - V_2) \times 1/32$
223	DFH	1	1	0	1	1	1	1	1	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times V_2$	V_2
224	E0H	1	1	1	0	0	0	0	0	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_1 + (V_2 - V_1) \times 31/32\}$	$V_1 + (V_2 - V_1) \times 31/32$
225	E1H	1	1	1	0	0	0	1	1	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_1 + (V_2 - V_1) \times 30/32\}$	$V_1 + (V_2 - V_1) \times 30/32$
⋮	⋮				⋮					⋮	⋮
254	FEH	1	1	1	1	1	1	1	0	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times \{V_1 + (V_2 - V_1) \times 1/32\}$	$V_1 + (V_2 - V_1) \times 1/32$
255	FFH	1	1	1	1	1	1	1	1	$(4+\alpha)/\alpha \times V_{\text{ref}} - 4/\alpha \times V_0$	V_0

4.2 Curved line of output voltage

(POLA = H, $\alpha = 4$, $V_{ref} - 0.1 \text{ V} \geq V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_6 \geq V_7 \geq V_8 \geq V_9 \geq V_{SS2} + 0.1 \text{ V}$)



5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

The reference power supply of the D/A converter is made up of a capacitance ladder circuit, which minimizes current flow into the γ - corrected power supply pins. However, in the LCD driver of previous R-DAC systems the resistance ratio between the γ - corrected power supply pins was set to be identical to the γ - corrected voltage ratio used for an actual LCD panel. Such a function is not available in this product. Therefore, γ - corrected voltage directly becomes D/A converter reference power voltage in the IC. Determine γ - corrected voltage based on the data of γ characteristics of a LCD panel described in 4. **RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE.**

6. INPUT FORMAT OF DISPLAY DATA

Data format : 8 bits $\times$ 2 RGBs (6 dots)
Input width : 48 bits (2-pixel data)

(1) R/L = H (Right shift)

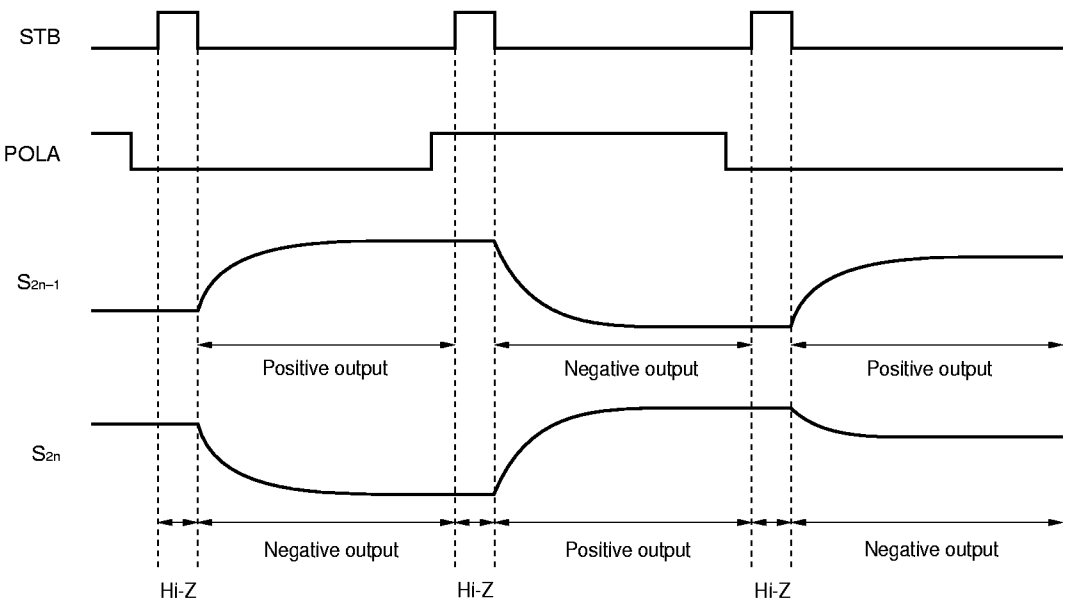
Output	S ₁	S ₂	S ₃	S ₄	...	S ₃₈₃	S ₃₈₄
Data	D ₀₀ to D ₀₇	D ₁₀ to D ₁₇	D ₂₀ to D ₂₇	D ₃₀ to D ₃₇	...	D ₄₀ to D ₄₇	D ₅₀ to D ₅₇

(2) R/L = L (Left shift)

Output	S ₁	S ₂	S ₃	S ₄	...	S ₃₈₃	S ₃₈₄
Data	D ₀₀ to D ₀₇	D ₁₀ to D ₁₇	D ₂₀ to D ₂₇	D ₃₀ to D ₃₇	...	D ₄₀ to D ₄₇	D ₅₀ to D ₅₇

7. RELATIONSHIP BETWEEN STB, POL, AND OUTPUT WAVEFORM

The output buffer consists of an operational amplifier circuit that does not perform recharge operation. Therefore, driver output current I_{VOH} is the charging current to the LCD, and I_{VOL} is the discharging current.



8. OFFSET VOLTAGE

Determine the coefficient α of V_{OUT} based on the offset control pins (D_{i0} to D_{i2}). Relationship between input data and α are listed as follows.

D_{i0}	D_{i1}	D_{i2}	α
0	0	0	4.0
1	0	0	4.4
0	1	0	4.6
1	1	0	4.8
0	0	1	5.0
1	0	1	5.2
0	1	1	5.4
1	1	1	5.6

Remark $V_{OUT} = (4 + \alpha) / \alpha \times V_{ref} - 4 / \alpha \times \{V_m + (V_{m+1} - V_m) \times n / 32\}$

9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings ($T_A = +25^\circ\text{C}$, $V_{SS1} = V_{SS2} = 0\text{ V}$)

Parameter	Symbol	Ratings	Unit
Logic Part Power Supply Voltage	V_{DD1}	-0.5 to + 6.0	V
Driver Part power Supply Voltage	V_{DD2}	-0.5 to + 10.0	V
Logic Part Input Voltage	V_{I1}	-0.5 to $V_{DD1} + 0.5$	V
Driver Part Input Voltage	V_{I2}	-0.5 to $V_{DD2} + 0.5$	V
Logic Part Output Voltage	V_{O1}	-0.5 to $V_{DD1} + 0.5$	V
Driver Part Output Voltage	V_{O2}	-0.5 to $V_{DD2} + 0.5$	V
Operating Temperature Range	T_A	-10 to +75	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +125	$^\circ\text{C}$

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range ($T_A = -10$ to $+75^\circ\text{C}$, $V_{SS1} = V_{SS2} = 0\text{ V}$)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}	3.0	3.3	3.6	V
Driver Part Supply Voltage	V_{DD2}	8.5	9.0	9.5	V
Driver Part Output Voltage Range	V_O	$V_{SS2} + 0.1$		$V_{DD2} - 0.1$	V
γ -Corrected Voltage	V_0 to V_9	$V_{SS2} + 0.1$		$V_{ref} - 0.1$	V
γ -Corrected Reference Power Supply	V_{ref}		$0.5 V_{DD2}$	5.5	V
Maximum Clock Frequency	$f_{MAX.}$	65			MHz

Electrical Characteristics ($T_A = -10$ to $+75^\circ\text{C}$, $V_{DD1} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DD2} = 9.0\text{ V} \pm 0.5\text{ V}$, $V_{SS1} = V_{SS2} = 0\text{ V}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V_{IH}	CLK, STB, R, /L, INH, POLA, POLB,	$0.7 V_{DD1}$		V_{DD1}	V
Low-level Input Voltage	V_{IL}	D ₀₀ to D ₀₇ , D ₁₀ to D ₁₇ , D ₂₀ to D ₂₇ ,	0		$0.3 V_{DD1}$	V
Input Leak Current	I_{IL}	D ₃₀ to D ₃₇ , D ₄₀ to D ₄₇ , D ₅₀ to D ₅₇ , D ₁₀ to D ₁₂	-1.0		+1.0	μA
High-Level Output Voltage	V_{OH}	STHR (STHL), $I_{OH} = -1.0\text{ mA}$	$V_{DD1} - 0.5$			V
Low-level Output Voltage	V_{OL}	STHR (STHL), $I_{OL} = +1.0\text{ mA}$			$V_{SS1} + 0.5$	V
Driver Output Current ($V_{DD2} = 9.0\text{ V}$)	I_{VOH}	$V_{DD1} = 3.3\text{ V}$, $INH = 0\text{ V}$, $V_{OUT} = 8.4\text{ V}$, $V_O = 8.9\text{ V}^{\text{Note}}$		-0.18	-0.1	mA
	I_{VOL}	$V_{DD1} = 3.3\text{ V}$, $INH = 0\text{ V}$, $V_{OUT} = 0.6\text{ V}$, $V_O = 0.1\text{ V}^{\text{Note}}$	0.06	0.13		mA
Output Voltage Deviation	ΔV_O	$V_{DD1} = 3.3\text{ V}$, $V_{DD2} = 9.0\text{ V}$, $V_{OUT} = 0.5 / 3.0 / 5.0 / 8.0\text{ V}^{\text{Note}}$		± 10	± 20	mV
Logic Part Dynamic Current Consumption	I_{DD1}	$V_{DD1} = 3.3\text{ V}$, with no load		7	20	mA
Driver Part Dynamic Current Consumption	I_{DD2}	$V_{DD2} = 9.0\text{ V}$, with no load		8	16	mA

Note V_{OUT} indicates application voltage to output pins. V_O indicates output voltage to output pins.

Caution For logic part dynamic current consumption, the **TYP.** value is based on the condition while the screen is displayed in entirely dark or entirely light and the **MAX.** value is based on the condition while the screen is displayed in chess board pattern.

Switching Characteristics ($T_A = -10$ to $+75^\circ\text{C}$, $V_{DD1} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DD2} = 9.0\text{ V} \pm 0.5\text{ V}$, $V_{SS1} = V_{SS2} = 0\text{ V}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	$C_L = 10\text{ pF}$, CLK $\rightarrow$ STHL (STHR)	2		15	ns
★ Driver Output Delay Time	t_{PLH2}	$V_{DD2} = 9.0\text{ V}$, $R_L = 5.0\text{ k}\Omega$,	$V_O = 0.1\text{ V} \rightarrow 8.9\text{ V}$	3.0	6.0	μs
	t_{PLH3}			7.0	12.0	μs
	t_{PHL2}	$C_L = 70\text{ pF}$,	$V_O = 8.9\text{ V} \rightarrow 0.1\text{ V}$	3.0	6.0	μs
	t_{PHL3}			7.0	12.0	μs
★ Input Capacitance	C_{I1}	$T_A = +25^\circ\text{C}$, STHR (STHL), V_6 to V_9, V_{ref}		10	15	pF
	C_{I2}	$T_A = +25^\circ\text{C}$, STHR(STHL), V_6 to V_9 , Except V_{ref}		5	10	pF

★ Timing Requirement ($T_A = -10$ to $+75^\circ\text{C}$, $V_{DD1} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS1} = 0\text{ V}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		15			ns
Clock Pulse High Period	$PW_{CLK(H)}$		3			ns
Clock Pulse Low Period	$PW_{CLK(L)}$		3			ns
STB Pulse Width	PW_{STB}		1			CLK
INH Pulse Width	PW_{INH}		1			CLK
Data Setup Time	t_{SETUP1}		2			ns
Data Hold Time	t_{HOLD1}		2			ns
Start Pulse Setup Time	t_{SETUP2}		2			ns
Start Pulse Hold Time	t_{HOLD2}		2			ns
POLB Setup Time	t_{SETUP3}		2			ns
POLB Hold Time	t_{HOLD3}		2			ns
STB Pulse Rise Timing	t_{SRT1}		1			CLK
Start Pulse Rise Timing	t_{SRT2}		1			CLK
INH Rise Timing	t_{IRT}		1			μs
CLK-INH Time	$t_{CLK-INH}$	CLK $\uparrow \rightarrow$ INH $\downarrow$	4			ns
INH-CLK Time	$t_{INH-CLK}$	INH $\uparrow \rightarrow$ CLK $\uparrow$	4			ns
POLA-STB Time	$t_{POLA-STB}$	POLA $\uparrow$ or $\downarrow \rightarrow$ STB $\uparrow$	4			ns
CLK-STB Time	$t_{CLK-STB}$	CLK $\uparrow \rightarrow$ STB $\uparrow$	4			ns
STB-CLK Time	$t_{STB-CLK}$	STB $\uparrow \rightarrow$ CLK $\uparrow$	4			ns

11. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the μ PD16742.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

μ PD16742N-xxx : TCP (TAB package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C: heating for 2 to 3 seconds: pressure 100 g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm ² : time 3 to 5 secs. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm ² : time 30 to 40 secs. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.