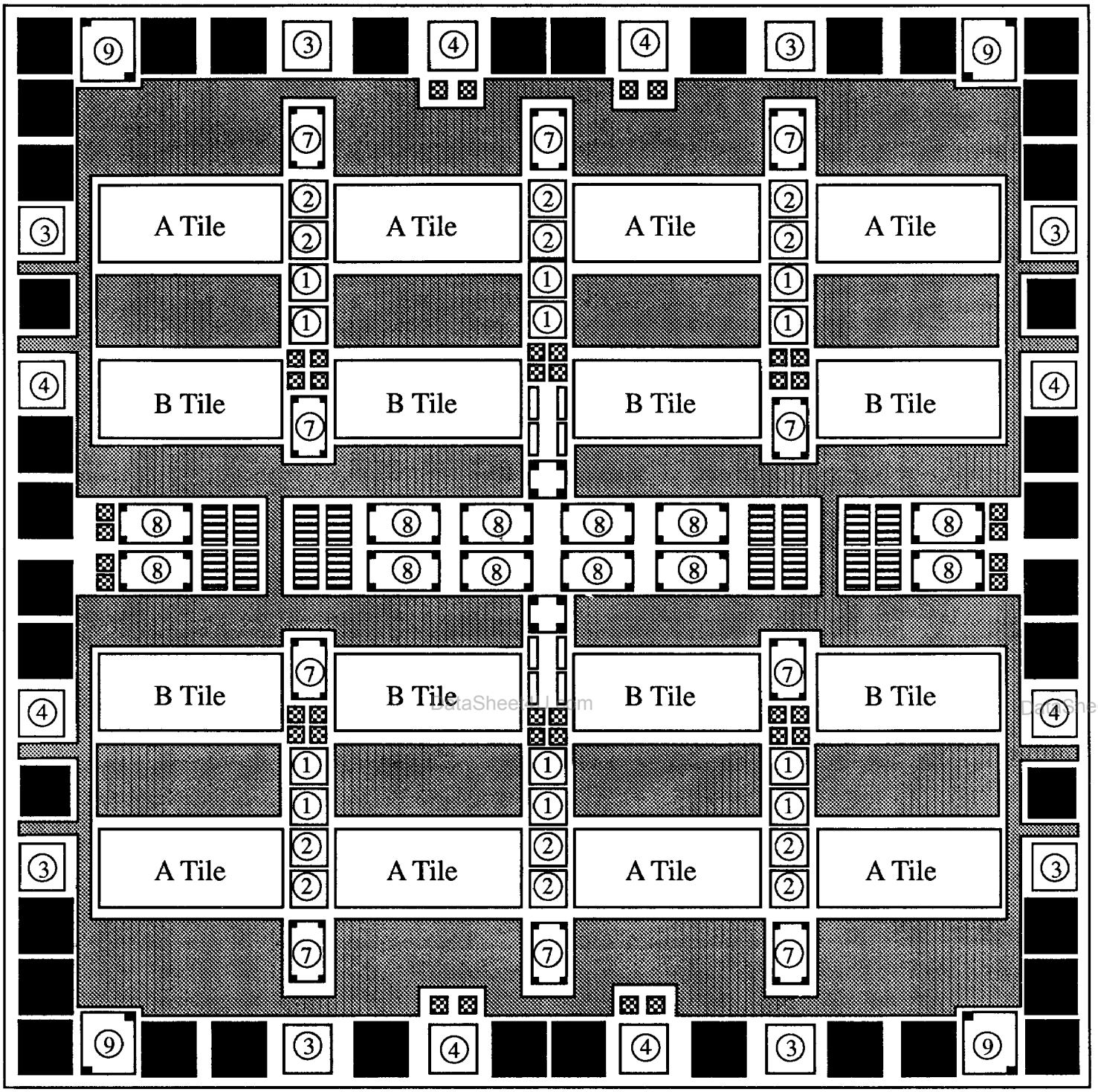
SP - 1204



Bond Pad

Buried Zener

Nichrome Clear Field Area

N+ /P+ Diode

P-JFET

Pinch Resistor

1 DBNPN

2 DBPNP

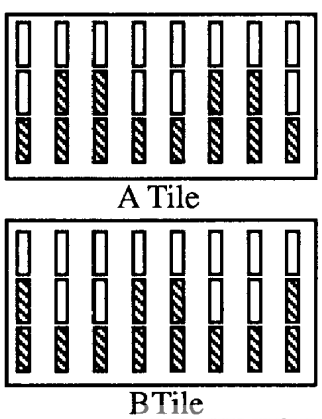
3 MNPN

4 MPNP

7 4.5pF Capacitor

8 6pF Capacitor

9 7pF Capacitor



SP1204 COMPONENT COUNT SUMMARY

DESCRIPTION	COUNT
Tiles:	
A Type	8
B Type	8
Transistors:	
SNPN	192
SPNP	192
DBNPN	16
DBPNP	16
MNPN	8
MPNP	8
HNPN	0
HPNP	0
P-JFET	16
Thin Film Resistors:	
Clear Field Area	5700 sq. mil (Total 800 KΩ Possible)
Pinch Resistors	8
Capacitors:	
4.5 pF (max)	10
6 pF (max)	12
7 pF (max)	4
Diodes:	
Buried Zener	2
N+/P+ Diodes	40
Bond Pads	40
Die Dimensions	146 mils x 140 mils

ARCHITECTURE & ORGANIZATION

The organization and complexity of the SP1204 array makes it ideally suited for integrating complete analog system functions on a single silicon chip. The SP1204 employs a tile based architecture where each tile has been configured (sized) so that it can contain a complete analog function. Pre-defined macro functions which fit these tiles are available and can be used to implement analog systems thus eliminating the tedious task of transistor level design. Using this approach also reduces both the manpower and elapsed time required to complete a design, while increasing the probability of first time success.

Each tile on the SP1204 consists of 12 SNPN & 12 SPNP transistors arranged in a 3 x 8 matrix. There are both A type & B type tiles. The only difference between the two tile types is that the locations of the SNPN & SPNP transistors in the middle row of the tile are reversed. As a result, A type tiles have two NPN Quads & one PNP Quad while the B type tiles have two PNP Quads and one NPN Quad. This feature simplifies many types of layouts.

The SP1204 is organized as a 4 x 4 matrix of tiles. The top and bottom rows have A type tiles while the two middle rows contain the B type tiles. Sixteen P-JFETs, arranged in quads, lie across the center of the die. The P-JFETs are only available with the 35 Volt process. (These areas are inactive when using the 20 Volt process).

Above and below each tile is a clear field area which is reserved for user defined thin film resistors. Interspersed between the tiles and around the periphery of the array are the various components available on the array.

To accommodate rapid layout, all SP1204 components are positioned on a 15µ grid. Within the clear field area there is a 5µ sub grid for thin-film resistor layout. The SP1204 is symmetric about the two perpendicular center lines of the array. There are additional symmetries within the tiles themselves as well as between adjacent tiles.

The dimensions of the SP1204 are 140 mils x 146 mils.

PROCESS OPTIONS

Maximum operating voltage is usually a key requirement in most applications. For an analog ASIC application the maximum possible voltage is ultimately limited by the breakdown voltage of the transistors. The lowest breakdown voltage is usually V_{CEO} and process application capability is specified by this parameter. The V_{CEO} is determined by a combination of starting silicon resistivity and transistor geometries (i.e. spacings). Higher starting silicon resistivity gives higher V_{CEO}, but at the expense of slightly higher transistor parasitics (mainly R_C) which will ultimately limit circuit performance.

The SP1204 array is available in two process options: 20 Volt and 35 Volt processes. By controlling substrate resistivity, V_{CEO}'s of 35 Volts & 20 Volts are achieved. The 20 Volt V_{CEO} process offers somewhat lower parasitics, and therefore, higher speed. This is the preferred process for high speed applications, if maximum voltages can be held below 20 Volts.

MACRO CELLS

Design time, cost and risk can be reduced significantly by designing with proven macro cells rather than at the transistor device level. A library of macro cells has been developed to support SP1204 user designs. Additional macros will be added to the library as they become available. Before starting your design, consult your local SIPEX sales office or the factory to obtain the latest update on available macro cells.

SP1204 MACRO CELL LIBRARY

CELL NAME	DESCRIPTION	# OF TILES
MXRB01	1.5V Voltage Reference	0.5
MXRB02	2.5V Voltage Reference	1
MXRB03	2.5V Voltage Reference a ±0.5 mA Current Reference	1
MXRB05	5.0V Voltage Reference	1
MXRB10	10.0V Voltage Reference	1
MXOP01	General Purpose Wideband Op Amp	1
MXOP02	Wideband, Medium Drive Op Amp	2
MXOP03	Precision High Bandwidth Op Amp	2
MXCM01	General Purpose Comparator	1

SUPPORT PRODUCTS & SERVICES

- Commercially Available P-SPICE or Equivalent Simulators (Purchased Directly From the Vendor)
- Design Manual (DESMAN 1100)
- Mylar Layout Worksheets
- GDS II Database Tape for Workstations Based Layouts
- A Family of Proven Macro Cells (Circuit Schematics and Net Lists are Available in the Design Manual)
- Transistor Level and Macro Cell Kit Parts to Support Evaluation and Breadboarding (If Required)
- Application Assistance and Training by Sipex Personnel

Sipex Corporation

SIGNAL PROCESSING EXCELLENCE

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Please Call
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Raytheon

R29000 Series Standard Performance PROMs and Power-Switched SPROMs

Applications

- Microprogram control store
- Microprocessor program store
- Programmable logic
- Custom look-up tables
- Security encoding/decoding
- Code converter
- Character generator
- Use in redundant systems

Description

Raytheon's R29000 Series of Bipolar Field Programmable Real-Only Memories include both standard and power-switched versions. Chip select inputs provide logic flexibility and ease of memory expansion decoding.

The power-switched devices (SPROMs) were originated by Raytheon to reduce overall power dissipation in PROM arrays. This technique takes advantage of the non-volatile nature of PROMs by removing power when a particular device is not being used in the system. Unlike previous power-switching schemes, which employed external transistors and resistors, the SPROM includes all power-switching circuitry on the same chip as the memory. Moreover, the power switch state is activated by the same Chip Select (Power Select) input scheme that is used to address a standard performance PROM; thus, in most cases, SPROMs can be directly substituted for standard devices without system redesign.

All Raytheon R29000 Series PROMs and SPROMs are manufactured with nichrome

Features/Benefits

- All devices are available in both commercial (0°C to +75°C) and military (-55°C to +125°C) temperature range
- All standard performance PROMs are offered in power-switched SPROM versions
- Very high tolerance to total dose radiation
- Typically, 75% power savings achieved on deselected SPROMs
- Device pinouts conform to JEDEC standards
- All devices programmed on standard PROM programmers
- Reliable nichrome fuses
- Three-state outputs
- Available in surface mount and through-hole packaging
- 4096 x 8 standard performance PROMs and power-switched SPROMs are offered in 24-pin, 0.3" wide DIPs

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Semiconductor Division

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