mosaic

Mosaic Semiconductor Inc.

PUMA 2U4000

PUMA 2U4000-17/20/25

Issue 2.0 : July 1989

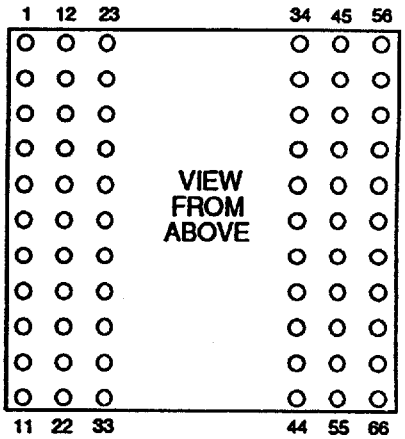
PRELIMINARY

4,194,304 bit CMOS High Speed UV EPROM

Features

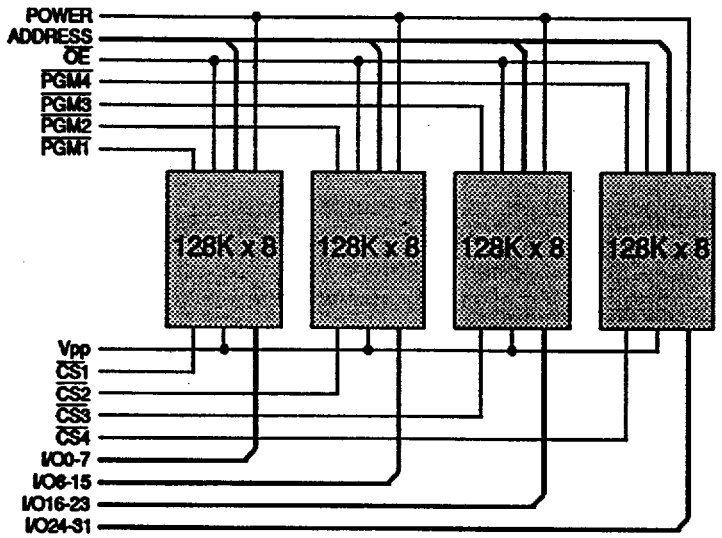
User Configurable as 8,16 or 32 bit wide.
Fast access times of 170/200/250 nS.
Low Power Operation 200mW (typ), 32 bit mode.
100mW (typ), 16 bit mode.
50mW (typ), 8 bit mode.
Low Power Standby 20µW (typ).
Vpp Program Voltage of 12.5V.
High Performance Programming available.
Pin grid array gives 2:1 improvement over DIL.
Package Suitable for Thermal Ladder Applications.
On board decoupling capacitors.
May be screened in accordance with BS9400 and MIL-STD-883C (suffix MB)

Pin Definition



For pinout see page 7

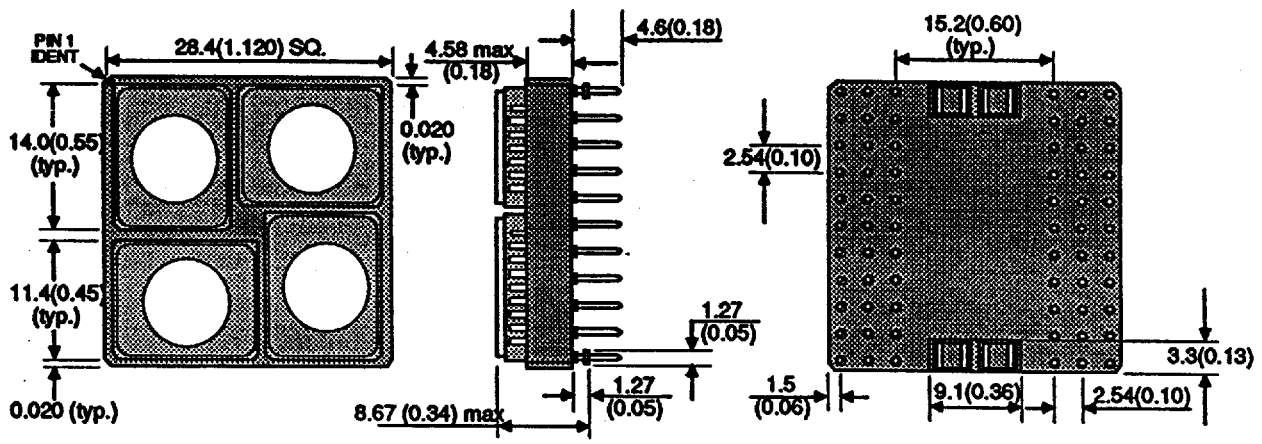
Block Diagram



Pin Functions

A0-16	Address Inputs
I/O0-31	Data Inputs/Outputs
CS1-4	Chip Select
OE	Output Enable
PGM1-4	Program Enable
NC	No Connect
Vcc	Power (+5V)
Vpp	Programming Voltage
GND	Ground

Package Details Dimensions in mm (inches).



Absolute Maximum Ratings (1)

Supply Voltage (2)	V_{CC}	-0.6 to +7	V
Programming Voltage	V_{PP}	-0.6 to +13	V
Input Voltage (2),(3)	V_{in}	-0.6 to +7	V
Operating Temperature	T_{opr}	-60 to +140	°C
Storage Temperature	T_{stg}	-65 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of The deviceat those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
(2) Pulse Width:-1 v for 50ns
(3) With Respect to GND

Recommended Operating Conditions

		min	*typ*	*max*	
DC Logic Supply Voltage	V_{CC}	4.75	5.0	6.3	V
DC EPROM Program Voltage	V_{PP}	12.2	-	12.5	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+1	V
Input Low Voltage	V_{IL}	0.3	-	0.8	V
Operating Temperature(1)	T_a	0	-	70	°C
	T_{ai}	-40	-	85	°C (4000I)
	T_{am}	-55	-	125	°C (4000M,4000MB)

Note:(1) Programming would normally take place at 25°C

Operating Modes

The Table below show the logic inputs required to control the operating modes of each EPROM on the PUMA2U4000.

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{PGM}$	*Vpp*	*Vcc*	*Outputs*
Read	0	0	1	5V	5V	Data out
Output Disable	0	1	1	5V	5V	Floating
Standby	1	X	X	5V	5V	Floating
Program	0	1	0	12.5V	6V	Data in
Program Verify	0	0	1	12.5V	6V	Data out
Page Data Latch	1	0	1	12.5V	6V	Data in
Page Program	1	1	0	12.5V	6V	Floating
Program Inhibit	0	0	0	12.5V	6V	Floating
	0	1	1	12.5V	6V	
	1	0	0	12.5V	6V	
	1	1	1	12.5V	6V	

1 = V_{ih}
0 = V_{il}
X = Don't Care

Device Identifier Mode

The Identifier Mode allows the reading out of binary codes, which identify manufacturer and type of device, from the outputs of each EPROM. By this mode, the device can be automatically matched to the correct programming algorithm using a suitable EPROM Programmer. The table below shows the outputs of a single EPROM with the PUMA 2U4000 in 8 bit Mode.

PINS / IDENTIFIER	$\overline{PGM1}$	A9	A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX DATA
Manufacturer Code	V_{ih}	12.0V	V_{il}	0	0	0	0	0	1	1	1	07
Device Code			V_{ih}	0	0	1	1	1	0	0	0	38

Notes (1) A1 - A8, A10 - A16, $\overline{CS1}$ and $\overline{OE}$ are all held at V_{il}

READ OPERATION

T-46-13-29

DC Electrical Characteristics (T_a=0 to±70°C,V_{CC}=5V±5%)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{in1}	V_{in}=5.25V, input $\overline{OE}$, Address	-	-	8	µA
	I_{in2}	All other inputs	-	-	2	µA
Output Leakage Current	I_{out}	V_{out}=5.25V/0.45V	-	-	8	µA
V_{PP} Leakage Current	I_{PP}	V_{PP}=5.5V	-	4	80	µA
Standby Power	I_{sb1}	$\overline{CS}$ = V_{ih}	-	-	4	mA
Supply Current	I_{sb1}	$\overline{CS}$=V_{CC} ±0.3V, I_{out}=0mA	-	4	80	µA
Operating Power	I_{cc1}	f=1MHz, I_{out}=0mA (3)	18	32	60	mA
Supply Current	I_{cc2}	f=5MHz, I_{out}=0mA (3)	33	62	120	mA
Input Low Voltage	V_{il}	Note (1)	-0.3	-	0.8	V
Input High Voltage	V_{ih}	Note (2)	2.2	-	V_{CC}+1	V
Output LowVoltage	V_{ol}	I_{ol}=2.1mA	-	-	0.45	V
Output HighVoltage	V_{oh}	I_{oh}=-400µA	2.4	-	-	V

Notes (1) -1.0V for pulse width ≤ 50 ns
(2) Vcc+1.5V for pulse width ≤20 ns. If V_{ih} is over the specified max. value, READ operation cannot be guaranteed.
(3) For these currents min, typ and max values are given for 8, 16 and 32 bit mode operation respectively. Each individual value shown is a maximum.

Capacitance (T_a=25°C,f=1MHz)

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance:	C_{in}	V_{in}=0V	-	40	pF
Output Capacitance:	C_{out}	V_{out}=0V	-	60	pF

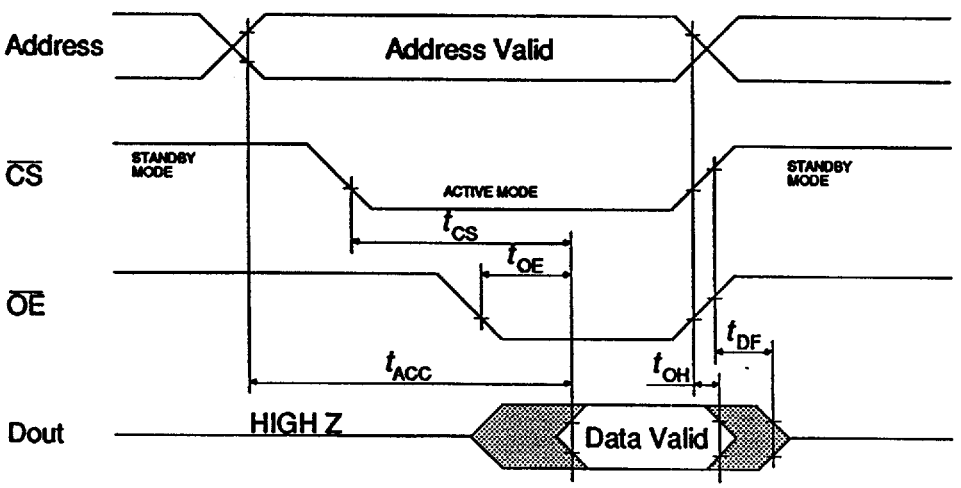
AC Characteristics

		-17		*-20*		*-25*		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Address to Output Delay	t_{ACC}	-	170	-	200	-	250	ns
$\overline{CS}$ to Output Delay	t_{CS}	-	170	-	200	-	250	ns
$\overline{OE}$ to Output Delay	t_{OE}	10	70	10	70	10	100	ns
$\overline{OE}$ or $\overline{CS}$ High to Output Float	t_{DF}	0	50	0	50	0	60	ns
Output Hold from Address, $\overline{CS}$ or $\overline{OE}$ (whichever occurred first)	t_{OH}	0	-	0	-	0	-	ns

AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: ≤ 20ns
* Input and Output timing reference levels: 0.8V and 2.0V
* Output load : 1 TTL gate plus 100pF.

Read Cycle Timing Waveform



PROGRAMMING OPERATION

T-46-13-29

DC Electrical Characteristics (T_a= 25°C ±5°C, V_{CC}= 6V±0.25V, V_{PP} = 12.5V ±0.3V)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Operating Power Supply Current	I_{CC}	Note (7)	33	62	120	mA
V_{PP} Supply Current	I_{PP1}	Single Byte Programming (7)	43	82	160	mA
	I_{PP2}	Page Mode Programming (7)	53	102	200	mA
Input Low Voltage	V_{il}	Note (5)	-0.1	-	0.8	V
Input High Voltage	V_{ih}	Note (6)	2.2	-	V_{CC}+0.5	V
Output LowVoltage (Verify)	V_{ol}	I_{ol}=2.1mA	-	-	0.45	V
Output HighVoltage (Verify)	V_{oh}	I_{oh}=-400µA	2.4	-	-	V

Notes (1) V_{CC} must be applied before V_{PP} and removed after V_{PP}.
(2) V_{PP} must not exceed 13V including overshoot.
(3) Device reliability may be affected if device is installed or removed while V_{PP}= 12.5V
(4) The transitions Vil to 12.5V or 12.5V to V_{il} are not allowed while $\overline{CS}$ = Low.
(5) -0.6V for pulse width ≤ 20 ns.
(6) If V_{ih} is over the specified maximum value, programming operation cannot be guaranteed.
(7) For V_{CC} and V_{PP} Supply Currents, min, typ and max values are given for 8, 16 and 32 bit mode operation respectively. Each individual value shown is a maximum.

AC Characteristics

Parameter		*Symbol*	*min*	*typ*	*max*	*Unit*
Address Setup Time		t_{AS}	2	-	-	µs
$\overline{OE}$ Setup Time		t_{OES}	2	-	-	µs
$\overline{OE}$ Hold Time		t_{OEH}	2	-	-	µs
Data Setup Time		t_{DS}	2	-	-	µs
Address Hold Time		t_{AH}	0	-	-	µs
		t_{AHL}	2	-	-	µs
Data Hold Time		t_{DH}	2	-	-	µs
$\overline{OE}$ High to Output Float Delay	(1)	t_{DF}	0	-	130	ns
Vpp Setup Time		t_{VPS}	2	-	-	µs
Vcc Setup Time		t_{VCS}	2	-	-	µs
$\overline{PGM}$ Initial Program Pulse Width	(2)	t_{PW}	0.19	0.2	0.21	ms
$\overline{PGM}$ Overprogram Pulse Width	(3)	t_{OPW}	0.19	-	5.25	ms
Data Valid from $\overline{OE}$		t_{OE}	0	-	150	ns
$\overline{OE}$ Pulse Rise Time During Programming		t_{PRT}	50	-	-	ns
$\overline{PGM}$ Setup Time		t_{PGMS}	2	-	-	µs
$\overline{CS}$ Setup Time		t_{CES}	2	-	-	µs
$\overline{CS}$ Hold Time		t_{CSH}	2	-	-	µs
$\overline{OE}$ Pulse Width during Data Latch		t_{LW}	1	-	-	µs

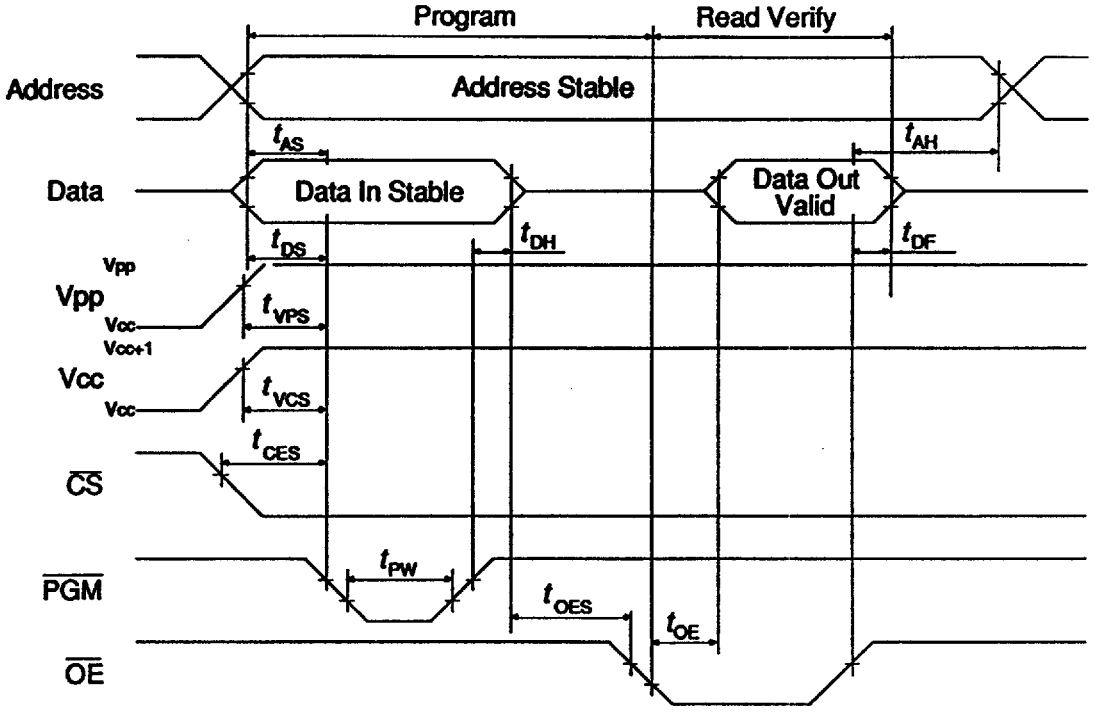
Notes (1) Defines the time at which the output achieves the open circuit condition and is no longer driven.
(2) Initial program pulse width tolerance is 0.2 ms± 5%.
(3) Length of this pulse may vary as a function of the iteration counter value n.

AC Test Conditions

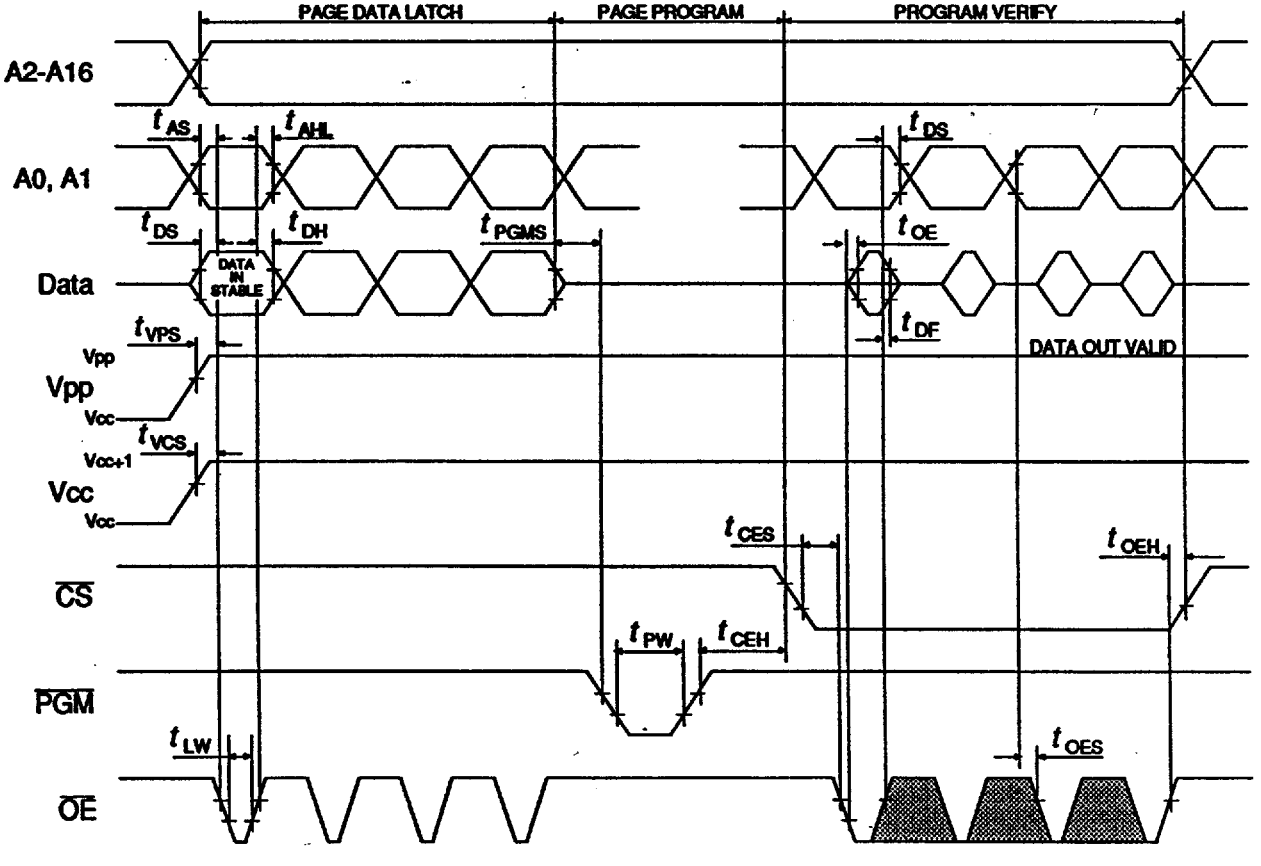
* Input pulse levels: 0V to 3.0V
* Input rise and fall times: ≤ 20ns
* Input and Output timing reference levels: 1.5V

Programming Cycle Timing Waveforms
Single Byte Programming

T-46-13-29



Page Mode Programming



HIGH PERFORMANCE PROGRAMMING ALGORITHMS

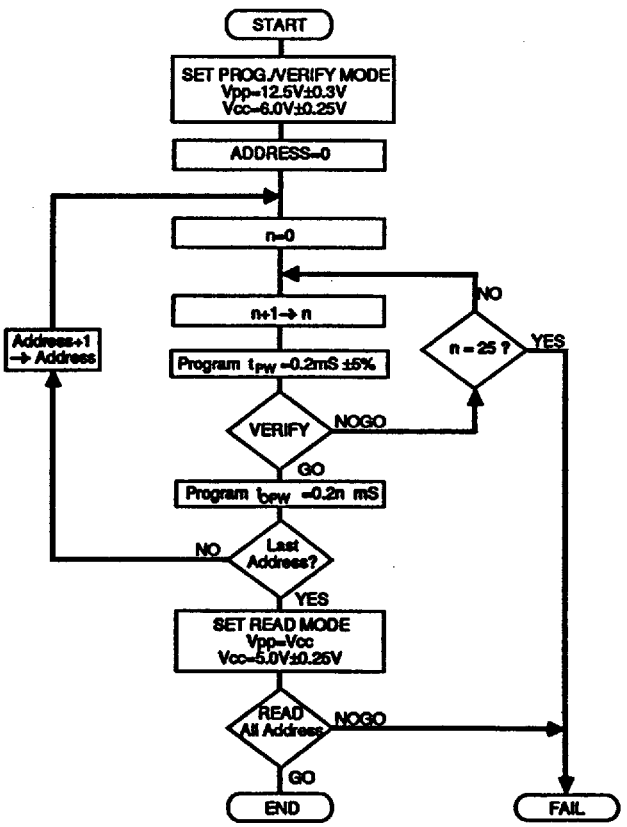
T-46-13-29

The PUMA2U4000 can be programmed using either of the alogorithms shown below. These allow faster programming times without stressing the device or causing deterioration in Data Retention Time. Two methods are described below, Single Byte and Page Mode, the selection of which are shown in the Truth Table on page 2.

Although each flow chart specifically refers to a single EPROM, all four devices on the PUMA tile can be programmed simultaneously in 32 bit mode, in pairs in 16 bit mode or singly in 8 bit mode. Obviously 32 bit mode is potentially the fastest programming time, but this makes greater demands on the Vpp Supply Current.

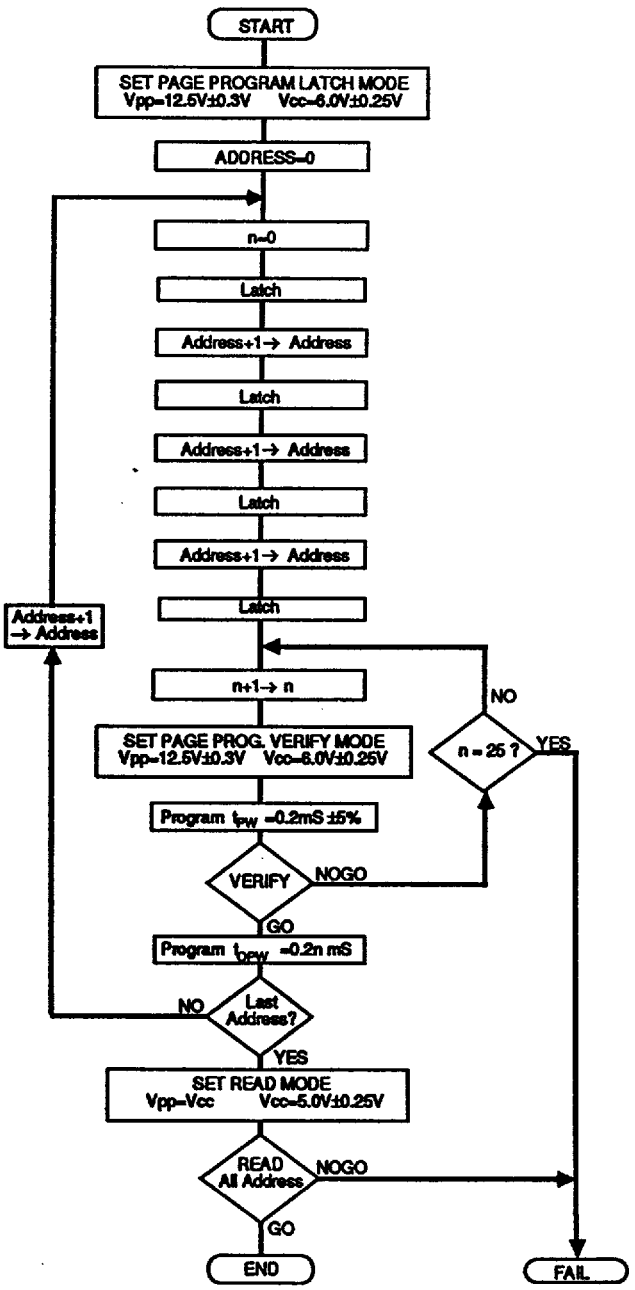
Single Byte

When the Program logic conditions are satisfied, the location is designated by A0 - A16, and the data to be programmed is applied 8 bits in parallel on D0 - D7. In this state, Byte programming is completed when PGM is at a low level.



Page Mode

Page Mode allows 4 bytes of data to be simultaneously programmed. The destination address for a Page Programming operation must reside on the same page i.e. A2 - A16 must not change. When the logic conditions in the Truth Table are satisfied, Page Mode Programming is activated. The four locations in the same page are designated by A0 - A1, and the data is applied in parallel on D0 - D7. In this state the data latch (4 bytes) is completed, and the data is programmed when $\overline{OE}$ is high. Programming is completed when $\overline{PGM}$ is low.



ERASE

Erasure of the PUMA 2U4000 is performed by exposure to ultraviolet light of 2537 Å at a minimum intensity of 15WS/cm², for approximately 15 - 20 minutes.

Note that sunlight and flourescent light may contain sufficient ultraviolet light to erase the programmed information. For this reason, and anyway for any operation in the READ mode, the transparent lids on this device should be covered with an opaque label.

Connection Table

PGA Pin No.	*Signal Name*	*PGA Pin No.*	*Signal Name*	*PGA Pin No.*	*Signal Name*	*PGA Pin No.*	*Signal Name*	*PGA Pin No.*	*Signal Name*
1	D8	2	D9	3	D10	4	A14	5	A16
6	A11	7	A0	8	NC	9	D0	10	D1
11	D2	12	$\overline{PGM2}$	13	$\overline{CS2}$	14	GND	15	D11
16	A10	17	A9	18	A15	19	Vcc	20	$\overline{CS1}$
21	NC	22	D3	23	D15	24	D14	25	D13
26	D12	27	$\overline{OE}$	28	NC	29	$\overline{PGM1}$	30	D7
31	D6	32	D5	33	D4	34	D24	35	D25
36	D26	37	A7	38	A12	39	Vpp	40	A13
41	A8	42	D16	43	D17	44	D18	45	Vcc
46	$\overline{CS4}$	47	$\overline{PGM4}$	48	D27	49	A4	50	A5
51	A6	52	$\overline{PGM3}$	53	$\overline{CS3}$	54	GND	55	D19
56	D31	57	D30	58	D29	59	D28	60	A1
61	A2	62	A3	63	D23	64	D22	65	D21
66	D20								

Ordering Information

PUMA 2U4000MB-17

- Speed
  - 17 = 170 ns
  - 20 = 200 ns
  - 25 = 250 ns
- Temp. range/screening
  - Blank = Commercial Temp.
  - I = Industrial Temp.
  - M = Military Temp.
  - MB = High Reliability MIL STD 883C Screening
- Memory Type
  - U = UV EPROM

Module Screening Flow for high reliability product is in accordance with MIL-STD-883C method 5004 Level B and is detailed below:

MB MODULE SCREENING FLOW		
SCREEN	TEST METHOD	LEVEL
Visual and Mechanical		
External visual	2017 Condition B (or manufacturers equivalent)	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Burn-In		
Pre Burn-in Electrical	Per Applicable device Specifications at Ta = +25°C (optional)	100%
Burn-In	Method 1015, Condition D, Ta=+125°C	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective Allowable (PDA)	Calculated at Post Burn-in at Ta=+25°C	10%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per vendor or customer specification	

mosaic
Mosaic Semiconductor Inc.
7420 Carroll Road
San Diego, CA 92121
Tel: (619) 271 4565
FAX: (619) 271 6058