■ MN102H950F

Туре	MN102H950F
Internal ROM type	External
ROM (byte)	_
RAM (byte)	10K
Package (Lead-free)	LQFP100-P-1414
Minimum Instruction	[With main clock operated]
Execution Time	58 ns (at 3.0 V to 3.6 V, 34 MHz)

■ Interrupts

/RST pin, Watchdog, /NMI pin, Timer counter 0 to 9 underflow, Timer counter 10 to 14 underflow, Timer counter 10 to 14 compare capture A, Timer counter 10 to 14 compare capture B, ATC ch.0 to ch.3 tra nsfer finish, External 0 to 4, Serial ch.0 to ch.4 tra nsmission, Serial ch.0 to ch.4 reception, A/D conversion finish

■ Tim

mer Counter Timer counter 0 : 8-bit × 1 Clock source
Timer counter 1 : 8-bit × 1 Clock source
Timer counter 2 : 8-bit \times 1 Clock source
Timer counter 3: 8-bit \times 1 Clock source
Timer counter 4 : 8-bit × 1 Clock source
Timer counter 5 : 8-bit × 1 Clock source
Timer counter 6 : 8-bit \times 1 Clock source
Timer counter 7 : 8-bit \times 1 Clock source
Timer counter 8 : 8-bit × 1 Clock source
Timer counter 9 : 8-bit × 1 Clock source
Timer counter 10 : 16-bit \times 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)

Clock source......underflow of timer counter 8, 9; TM10IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode

Interrupt source underflow of timer counter 10; timer counter 10 compare capture A; timer counter 10 compare capture B

of TM10IOA pin/TM10IOB pin (1 \times , 4 \times)

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Timer counter 11: 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source......underflow of timer counter 8, 9; TM11IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM11IOA pin/TM11IOB pin $(1 \times, 4 \times)$ Interrupt source underflow of timer counter 11; timer counter 11 compare capture A; timer counter 11 compare capture B Timer counter 12: 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source...... underflow of timer counter 8, 9; TM12IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM12IOA pin/TM12IOB pin $(1 \times, 4 \times)$ Interrupt source underflow of timer counter 12; timer counter 12 compare capture A; timer counter 12 compare capture B Timer counter 13: 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source...... underflow of timer counter 8, 9; TM13IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM13IOA pin/TM13IOB pin $(1 \times, 4 \times)$ Interrupt source underflow of timer counter 13; timer counter 13 compare capture A; timer counter 13 compare capture B Timer counter 14: 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source......underflow of timer counter 8, 9; TM14IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM14IOA pin/TM14IOB pin $(1 \times, 4 \times)$ Interrupt source underflow of timer counter 14; timer counter 14 compare capture A; timer counter 14 compare capture B ■ Serial interface Serial 0, 1:8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Serial 2, 3:8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) UART × 4 (common use with serial 0 to 3) $I^2C \times 2$ (common use with serial 1,3; single master) ■ I/O Pins Common use: 43 (use of full address, address data separate 16-bit mode) Common use: 57 (use of address 16-bit, address data separate 8-bit mode) I/O 63 Common use: 56 (use of full address, address data multiplex 16-bit mode) Common use: 63 (use of address 16-bit, address data multiplex 8-bit mode)

■ A/D converter

10-bit \times 12-ch. (with S/H)

■ D/A converter

8-bit \times 4-ch.

■ PWM

16-bit \times 5-ch. (timer counter 10 to 14)

■ ICR

16-bit \times 5-ch. (timer counter 10 to 14)

OCR

16-bit \times 5-ch. (timer counter 10 to 14)

Notes

Address / data separate bus interface; 8 / 16-bit bus width selectable; SRAM interface Address / data multiplex bus interface support

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■ Electrical Charactreistics (Supply current)

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	Offic
Operating supply current	IDDopr	VI = VDD or VSS, output open			60	mA
		f = 34 MHz, $VDD = 3.3 V$				
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and			70	μΑ
		Hi-Z state input/output pins are simultaneously applied				
Supply current at HALT0	IDDH	VDD or VSS level			30	mA
		f = 34 MHz, VDD = 3.3 V, output open				

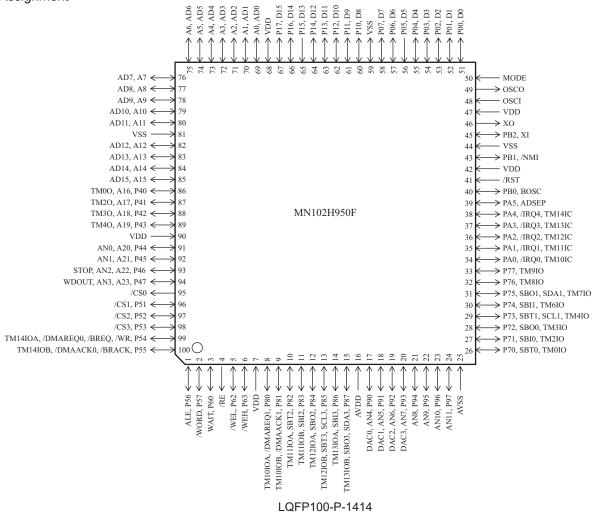
(Ta = -40°C to +85°C, VDD = AVDD = 3.3 V, VSS = AVSS = 0 V)

Development tools

In-circuit Emulator

PX-ICE102H930F-LQFP100-P-1414

■ Pin Assignment



LQFP 100-P-14 14

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