

## Radiation Hardened CMOS Dual SPDT Analog Switch

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The HS-303RH-T analog switch is a monolithic device fabricated using Radiation Hardened CMOS technology and the Intersil dielectric isolation process for latch-up free operation. Improved total dose hardness is obtained by layout (thin oxide tabs extending to a channel stop) and processing (hardened gate oxide). This switch offers low-resistance switching performance for analog voltages up to the supply rails. "ON" resistance is low and stays reasonably constant over the full range of operating voltage and current. "ON" resistance also stays reasonably constant when exposed to radiation, being typically 30Ω pre-rad and 35Ω post 100kRAD(Si). Break-before-make switching is controlled by 5V digital inputs.

### Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed electrical specifications for the HS-303RH-T are contained in SMD 5962-95813. A "hot-link" is provided from our website for downloading.

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is available on our website.

### Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (°C)
5962R9581301TCC	HS1-303RH-T	-55 to 125
5962R9581301TXC	HS9-303RH-T	-55 to 125

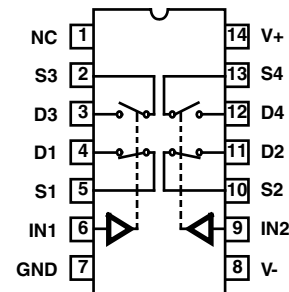
NOTE: Minimum order quantity for -T is 150 units through distribution, or 450 units direct.

### Features

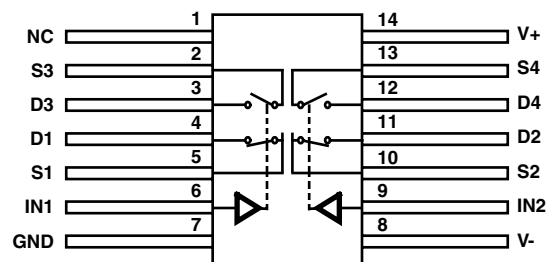
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose ( $\gamma$ ) 1 x 10<sup>5</sup> RAD(Si)
- No Latch-Up, Dielectrically Isolated Device Islands
- Pin for Pin Compatible with Intersil HI-303 Series Analog Switches
- Analog Signal Range 15V
- Low Leakage . . . . . 100nA (Max, Post Rad)
- Low r<sub>ON</sub> . . . . . 60Ω (Max, Post Rad)
- Low Operating Power . . . . . 100μA (Max, Post Rad)

### Pinouts

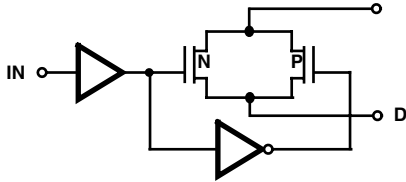
**HS1-303RH-T (SBDIP), CDIP2-T14  
TOP VIEW**



**HS9-303RH-T (FLATPACK) CDFP3-F14  
TOP VIEW**



## Functional Diagram



SBDIP TRUTH TABLE

LOGIC	SW1 AND SW2	SW3 AND SW4
0	OFF	ON
1	ON	OFF

## Die Characteristics

### DIE DIMENSIONS:

(2130 $\mu\text{m}$  x 1930 $\mu\text{m}$  x 279 $\mu\text{m}$   $\pm$ 25.4 $\mu\text{m}$ )

84 x 76 x 11mils  $\pm$ 1mil

### METALLIZATION:

Type: Al

Thickness: 12.5k $\text{\AA}$   $\pm$ 2k $\text{\AA}$

### SUBSTRATE POTENTIAL:

Unbiased (DI)

### BACKSIDE FINISH:

Gold

### PASSIVATION:

Type: Silox ( $\text{SiO}_2$ )

Thickness: 8k $\text{\AA}$   $\pm$ 1k $\text{\AA}$

### WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm<sup>2</sup>

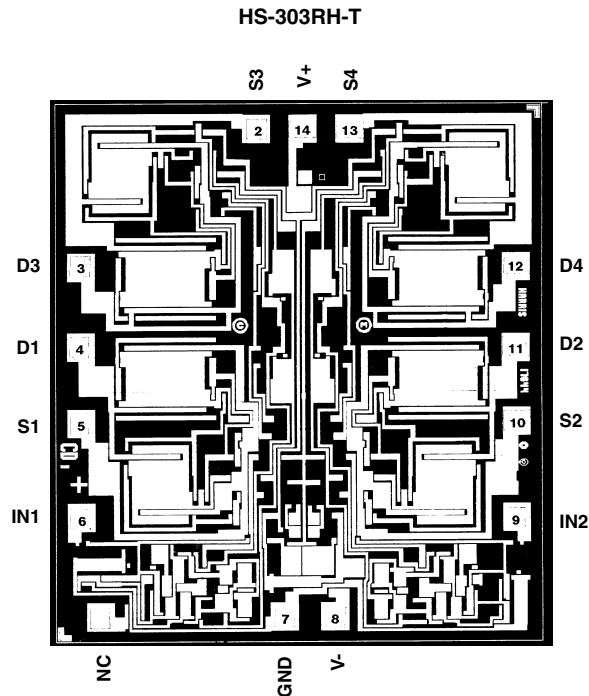
### TRANSISTOR COUNT:

76

### PROCESS:

Metal Gate CMOS, Dielectric Isolation

## Metallization Mask Layout



All Intersil products are manufactured, assembled and tested utilizing ISO9000 quality systems.

Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

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