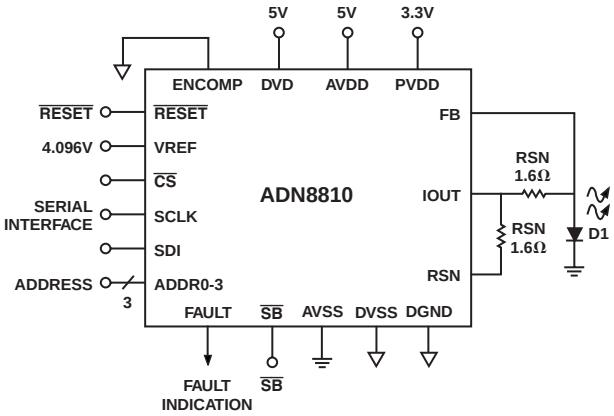
Programmable Precision Current Source for Tunable Laser

Preliminary Technical Data — ADN8810

FEATURES
High Precision 12-Bit Current Source
Low Noise
Long Term Stability
Current Output from 0 mA to 300 mA
Output Fault Indication
Low Drift
Programmable Maximum Current
4 mm × 4 mm Lead Frame Chip Scale Package
3-Wire Serial Interface

APPLICATIONS
Turnable Laser Current Source
Programmable High Output Current Source

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADN8810 is a tunable laser controller that provides high precision, low noise current sources and all other control signals needed for tunable laser devices.

The ADN8810 tunable laser controller can drive the Laser section, the Laser Front Mirror, Back Mirror, Phase, Gain or amplification. It interfaces to the host system over a serial interface. The host controls the operation of the controller.

Resolution and accuracy are 12-bits with ±3 LSB INL and ± LSB DNL. Noise and digital feed through are kept low to ensure low jitter operation. Full scale and scaled output currents are given in Equations 1 and 2, respectively.

$$I_{FS} \approx \frac{V_{REF}}{10 \times R_{SN}} \quad (1)$$

$$I_{OUT} = Code \times \frac{V_{REF}}{4096} \times \frac{1}{R_{SN}} \times \left(\frac{R_{SN}}{15k} + 0.1 \right) \quad (2)$$

*Protected by U.S.Patent No. 5,969,657; other patents pending.

REV. PrC

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

ADN8810–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

(AVDD = DVDD = 5 V, PVDD = 3.3 V, AVSS = DVSS = DGND = 0 V, T_A= 25°C, covering IOUT from 2% IFS to 100% IFS unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DC PERFORMANCE						
Resolution	N			12		Bit
Relative Accuracy	INL				±3	LSB
Differential Nonlinearity	DNL				±0.5	LSB
Offset				4	8	LSB
Offset Drift					15	ppm/°C
Gain Error					1%	FS
REFERENCE INPUT						
Reference Input Voltage	VREF		3.9	4.096	4.3	V
Input Impedance			500			kΩ
Bandwidth	BWref				2	MHz
ANALOG OUTPUT						
Output Current Change vs. Output Voltage Change	$\Delta I_{OUT}/\Delta V_{OUT}$	V_{OUT} = 0.7 V to 2.0 V			250	ppm/V
Max Output Current	I_{MAX}	$R_{SN1} = R_{SN2}$ = 1.6 Ω			250	mA
Capacitive Load	C_{LFB}		100			pF
Output Compliance Voltage	V_{COMP}			2.5		V
AC PERFORMANCE						
Settling Time	τ_S			3		µs
Bandwidth	BW			5		MHz
Current Noise Density @10 KHz	i_N	I_{FS} = 250 mA		7.5		nA/√Hz
		I_{FS} = 100 mA		2.5		nA/√Hz
		I_{FS} = 50 mA		1.25		nA/√Hz
Shutdown Recovery				6		µs
POWER SUPPLY[1]						
Power Supply Voltage	DVDD		3.0	5	5.5	V
	AVDD		4.5	5	5.5	V
	PVDD		3.0	3.3	3.6	V
Power Supply Rejection Ratio	PSRR	AVDD; PVDD	60	80		dB
Supply Current	I_{DVDD}	I_O = 0 mA		1		mA
	I_{AVDD}	I_O = 0 mA		1.5		mA
	I_{PVDD}	I_O = 0 mA		3		mA
FAULT DETECTION						
Load Open Threshold				PVDD–0.6		V
Load Short Threshold				AVSS+0.2		V
FAULT Logic Output	V_{OH}	DVDD = 5.0 V	4.5			V
	V_{OL}	DVDD = 5.0 V			0.5	V
LOGIC INPUTS						
Input Leakage Current	I_{IL}				±1	µA
Input Low Voltage	V_{IL}	DVDD = 3.0 V			0.5	V
		DVDD = 5 V			0.8	V
Input High Voltage	V_{IH}	DVDD = 3.0 V	2.4			V
		DVDD = 5 V	4			V
INTERFACE TIMING[2]						
Clock Frequency	f_{CLK}				25	MHz
$\overline{\text{RESET}}$ Pulse Width	t_{11}		20			ns

NOTES

[1]With respect to AVSS.

[2]See Timing Characteristics section for timing specifications.

TIMING CHARACTERISTICS[1,2]

Parameter	Description	Min	Typ	Max	Unit
f_{CLK}	SCLK Frequency			25	MHz
t_1	SCLK Cycle Time	40			ns
t_2	SCLK Width High	20			ns
t_3	SCLK Width Low	20			ns
t_4	$\overline{CS}$ Low to SCLK High Setup	15			ns
t_5	$\overline{CS}$ High to SCLK High Setup	15			ns
t_6	SCLK High to $\overline{CS}$ Low Hold	35			ns
t_7	SCLK High to $\overline{CS}$ High Hold	20			ns
t_8	Data Setup	15			ns
t_9	Data Hold	2			ns
t_{10}	$\overline{CS}$ High Pulsewidth	30			ns
t_{11}	$\overline{RESET}$ Pulsewidth	20			ns
t_{12}	$\overline{CS}$ High to $\overline{RESET}$ Low Hold	30			ns

NOTES

[1]Guaranteed by design. Not production tested.

[2]Sample tested during initial release and after any redesign or process change that may affect this parameter. All input signals are measured with tr = tf = 5 ns (10% to 90% of DVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

Specifications subject to change without notice.

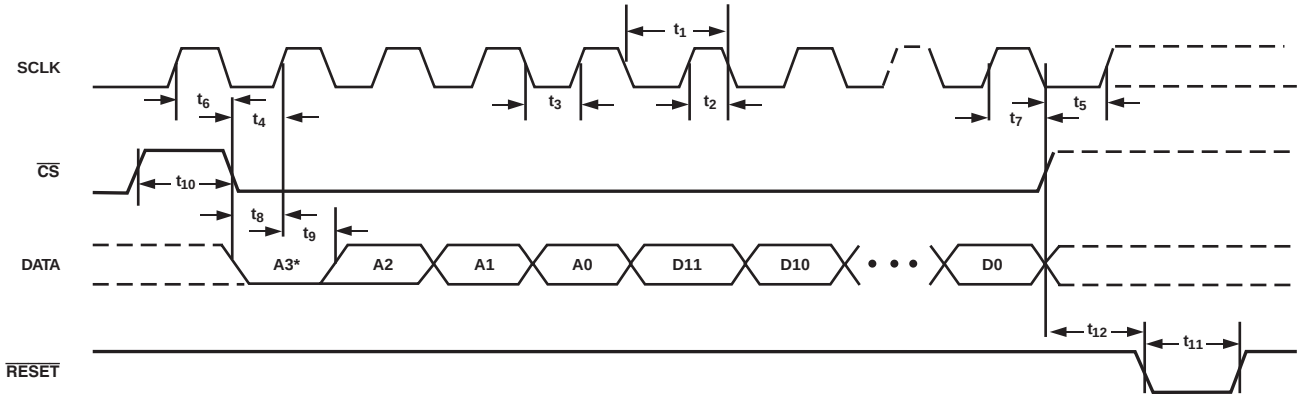
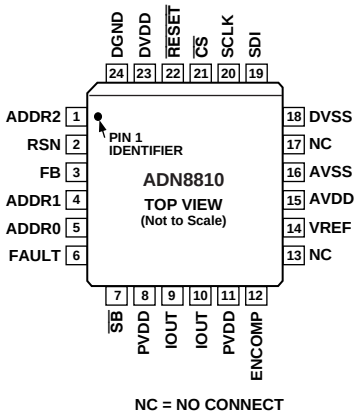


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6V
Input Voltage . . . . . GND to V_S + 0.3V
Output Short-Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . 0°C to +85°C
Junction Temperature Range
CP Packages . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 10 sec) . . . . . TBD

PIN CONFIGURATION



NC = NO CONNECT

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADN8810ACP	0°C to +85°C	24LEAD LFCSP	CP-24

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADN8810 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ADN8810 PIN FUNCTIONS

Pin	Name	Type	Description
1	ADDR2	Digital Input	Chip address, Bit 2
2	RSN	Analog Input	Sense resistor RS2 feedback
3	FB	Analog Input	Sense resistor RS1 feedback
4	ADDR1	Digital Input	Chip address, Bit 1
5	ADDR0	Digital Input	Chip address, Bit 0
6	FAULT	Digital Output	Load open/short indication
7	$\overline{SB}$	Digital Input	Active low deactivates output stage (high output impedance state)
8	PVDD	Power	Power supply for IOUT (3.3V recommended)
9	IOUT	Analog Output	Current output
10	IOUT	Analog Output	Current output
11	PVDD	Power	Power supply for IOUT (3.3V recommended)
12	ENCOMP	Digital Input	Connect to PVDD to enable internal compensation, otherwise connect to AVSS
13	NC		No connection
14	VREF	Analog Input	Input for high accuracy external reference voltage (ADR292ER)
15	AVDD	Power	Power supply for DAC
16	AVSS	Ground	Connect to analog ground or most negative potential in dual supply applications
17	NC		No connection
18	DVSS	Ground	Connect to digital ground or most negative potential in dual supply applciations
19	SDI	Digital Input	Serial data input
20	SCLK	Digital Input	Serial clock input
21	$\overline{CS}$	Digital Input	Chip select; active low
22	$\overline{RESET}$	Digital Input	Asynchronous reset to return DAC output to code zero; active low
23	DVDD	Power	Power supply for digital interface
24	DGND	Ground	Digital ground