MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTE50N45
MTE50N50
MTE60N35
MTE60N40

Designer's Data Sheet

Power Field Effect Transistor

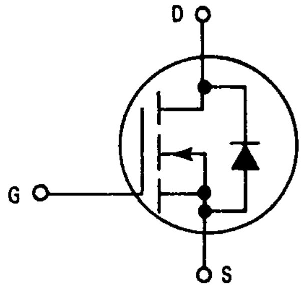
N-Channel Enhancement Mode Silicon Gate TMOS

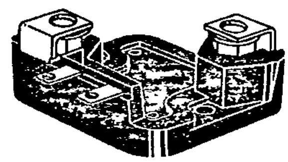
These TMOS Power FETs are designed for high current, high speed power switching applications such as switching regulators, converters, and motor controls.

- I_{DSS}, $V_{DS(on)}$, SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- High di/dt Capability
- Silicon Gate for Fast Switching Speeds
- Multi-chip Construction
- Gates Internally Decoupled

TMOS™

TMOS POWER FETs
50 and 60 AMPERES
$r_{DS(on)}$ = 0.075 OHM
350 and 400 VOLTS
$r_{DS(on)}$ = 0.100 OHM
450 and 500 VOLTS





CASE 346-01
MO-040AA

MAXIMUM RATINGS

Rating	Symbol	MTE 60N35	MTE 60N40	MTE 50N45	MTE 50N50	Unit
Drain-Source Voltage	V_{DSS}	350	400	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	350	400	450	500	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous Pulsed	I_D I_{DM}	60 300		50 240		Adc
Turn-Off Rate of Change	di_D/dt	See Note 4 and Figure 15 in Considerations				A/μs
Gate Current — Pulsed	I_{GM}	2				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	500 4				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150				°C
Mounting Torque (To heat sink with 10−32 screw)(1)	τ(m)	20				in-lb
Lead Torque (Lead to bus with 1/4−20 screw)(2)	τ(l)	20				in-lb
Per Unit Weight	W	120				grams

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Junction to Case	$R_{\theta JC}$	0.25	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

1. A Belleville washer of 0.472″ O.D., 0.205″ I.D., 0.024″ thick and 150 pounds flat is recommended.
2. The maximum penetration of the screw should be limited to 0.75″.

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MOTOROLA

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5 mA)	MTE60N35 MTE60N40 MTE50N45 MTE50N50	$V_{(BR)DSS}$	350 400 450 500	— — — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0) (T_J = 100°C)		I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1 mA, V_{DS} = V_{GS}) (T_J = 100°C)		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 30 Adc) (V_{GS} = 10 Vdc, I_D = 25 Adc)	MTE60N35/40 MTE50N45/50	$r_{DS(on)}$	— —	0.075 0.100	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 60 Adc) (I_D = 30 Adc, T_J = 100°C) (I_D = 50 Adc) (I_D = 25 Adc, T_J = 100°C)	MTE60N35/40 MTE60N35/40 MTE50N45/50 MTE50N45/50	$V_{DS(on)}$	— — — —	4.5 3.5 5.2 5	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 30 A) (V_{DS} = 15 V, I_D = 25 A)	MTE60N35/40 MTE50N45/50	g_{fs}	16 20	— —	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	12,000	pF
Output Capacitance		C_{oss}	—	2,000	
Reverse Transfer Capacitance		C_{rss}	—	800	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Inductive Load, Clamped — MTE60N35 and MTE60N40					
Turn-Off Delay Time	(V_{clamp} = 200 Vdc, I_D = 30 Adc,	t_{dv}	—	1,300	ns
Crossover Time	L = 25 μH, V_{in} = 10 Vdc	t_c	—	325	
Current Fall Time	R_{gen} = 50 Ω) See Figures 13 and 14	t_{fi}	—	200	
Inductive Load, Clamped — MTE50N45 and MTE50N50					
Turn-Off Delay Time	(V_{clamp} = 250 Vdc, I_D = 25, Adc,	t_{dv}	—	1,300	ns
Crossover Time	L = 25 μH, V_{in} = 10 Vdc	t_c	—	300	
Current Fall Time	R_{gen} = 50 Ω) See Figures 13 and 14	t_{fi}	—	200	

SOURCE-DRAIN DIODE CHARACTERISTICS*		Symbol	Typical	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0) See Figures 15 and 16.	V_{SD}	2	Vdc
Forward Turn-On Time		t_{on}	350	ns
Reverse Recovery Time		t_{rr}	2,000	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

ON-REGION CHARACTERISTICS

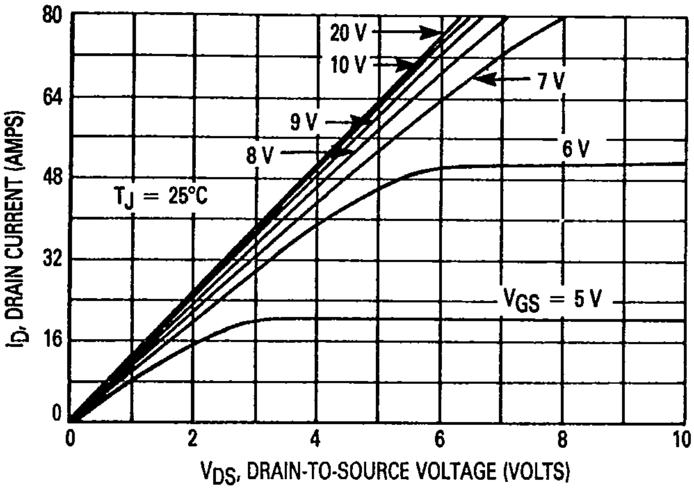


Figure 1. MTE50N45/50

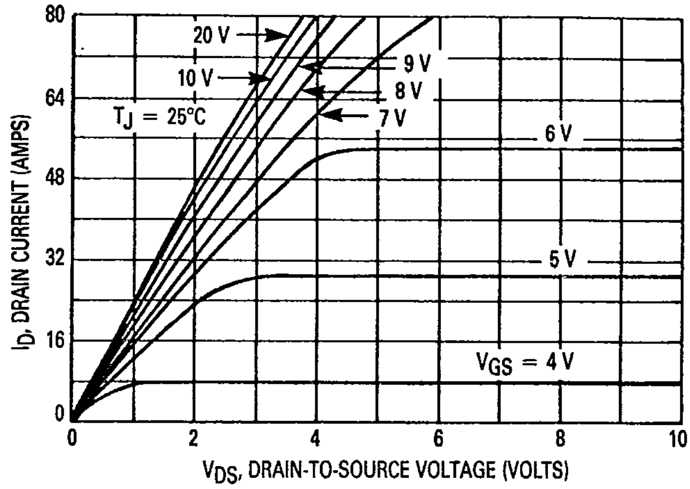


Figure 2. MTE60N35/40

TRANSFER CHARACTERISTICS

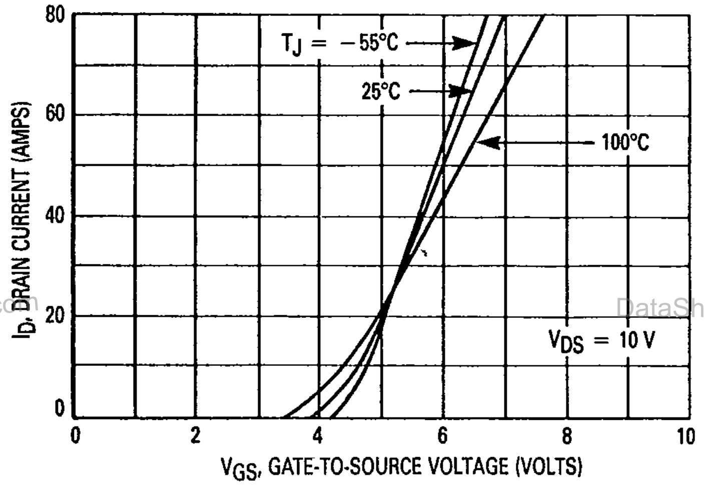


Figure 3. MTE50N45/50

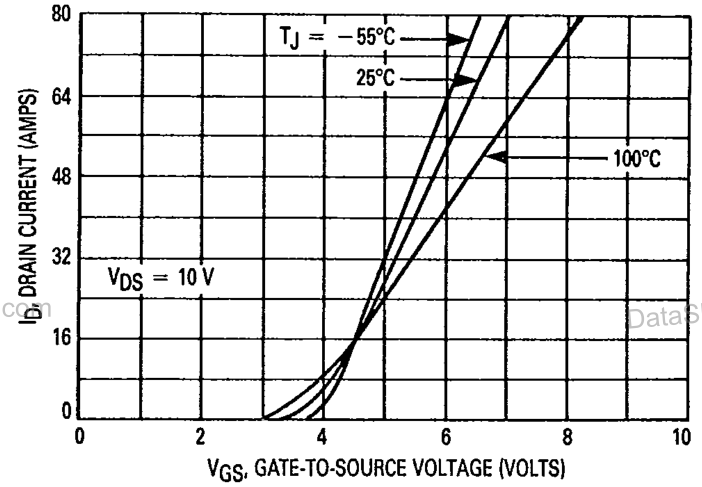


Figure 4. MTE60N35/40

ON-RESISTANCE versus DRAIN CURRENT

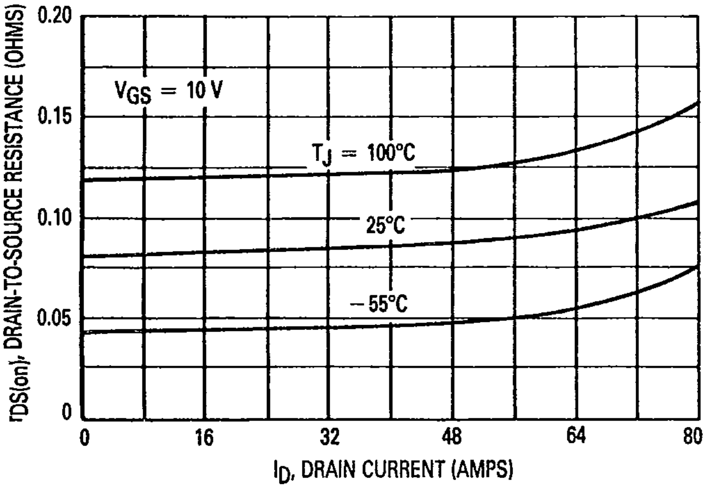


Figure 5. MTE50N45/50

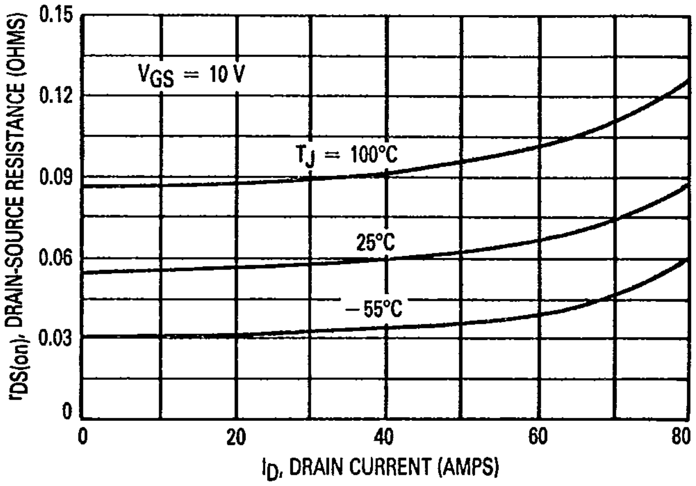


Figure 6. MTE60N35/40

TYPICAL CHARACTERISTICS

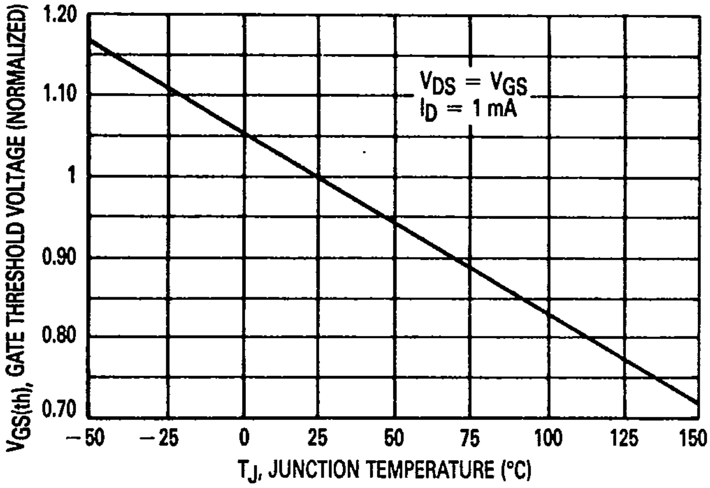


Figure 7. Gate-Threshold Voltage Variation with Temperature

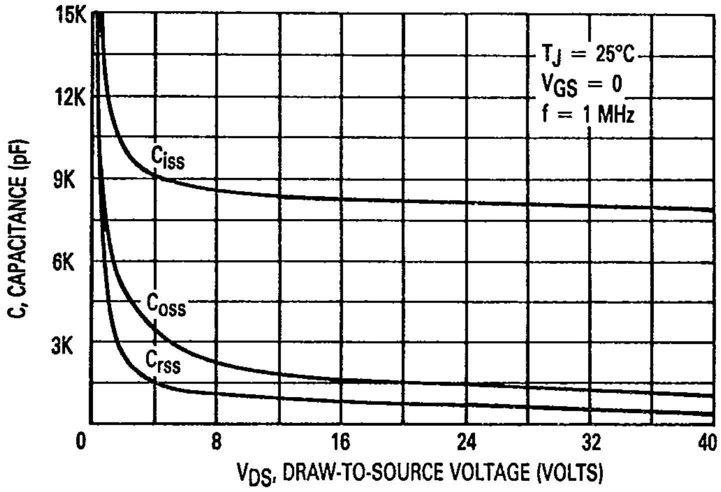


Figure 8. Capacitance Variation

SAFE OPERATING AREA INFORMATION

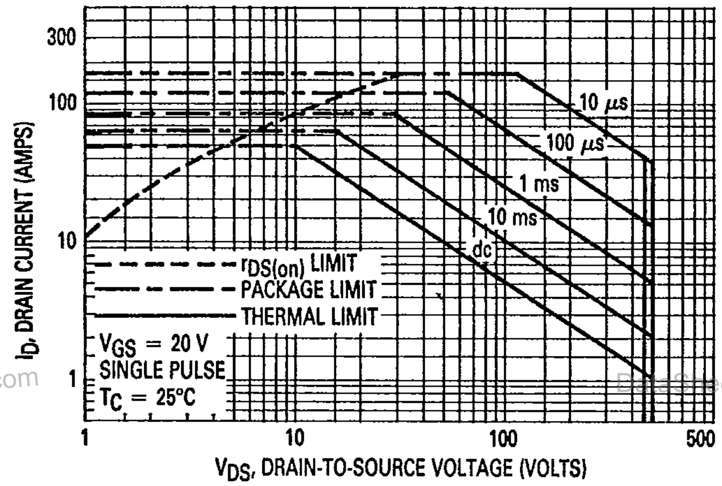


Figure 9. MTE50N45/50 Maximum Rated Forward Biased Safe Operating Area

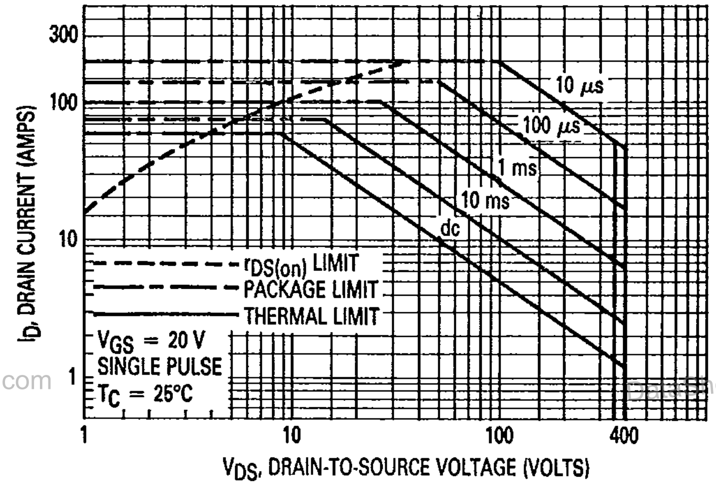


Figure 10. MTE60N35/40 Maximum Rated Forward Biased Safe Operating Area

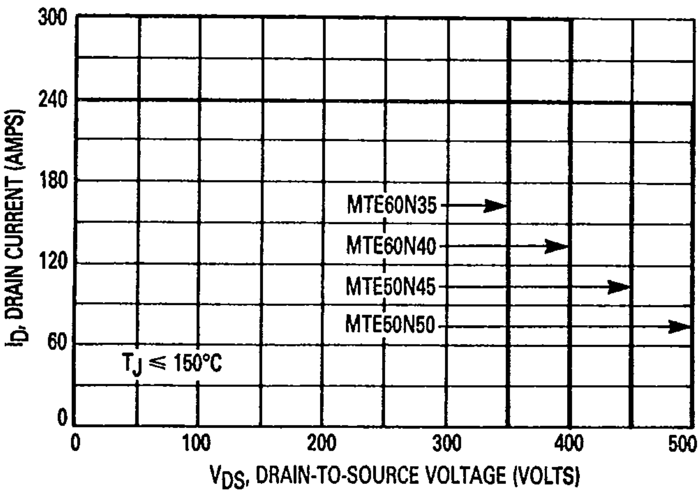


Figure 11. MTE6035/40 AND MTE50N45/50 Maximum Rated Switching Safe Operating Area

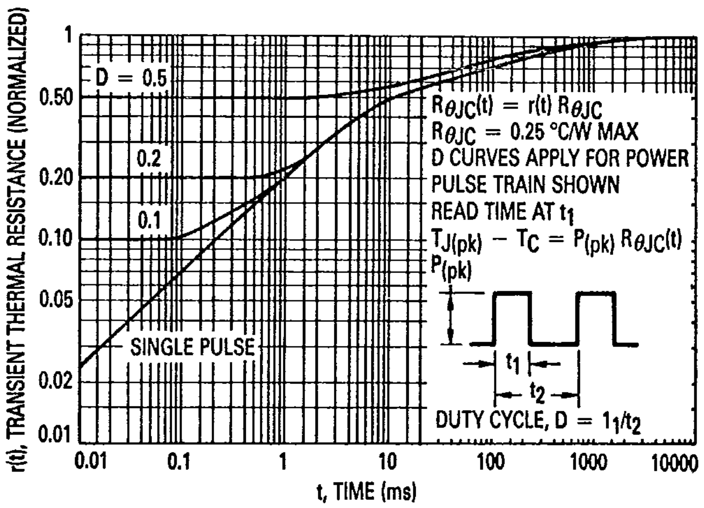


Figure 12. Thermal Response

GUARANTEED SAFE OPERATING AREA

The dc data presented in Figures 9 and 10 is for a single pulse, applied while maintaining the case temperature T_C at 25°C. For multiple pulses and case temperatures other than 25°C, the dc drain current at a case temperature of 25°C should be de-rated as follows:

$$I_D(T) = I_D\,(25°)\left[\frac{150 - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where P_D is the maximum power rating at 25°C, $R_{\theta JC}$ is the junction-to case thermal resistance, and r(t) is the normalized thermal response from Figure 15, corresponding to the appropriate pulse width and duty cycle.

EXAMPLE: Determine the maximum allowable drain current for an MTE50N50 at 25 volts drain voltage, with a pulse width of 10 ms and duty cycle of 50%, at a case temperature of 80°C.

From Figure 9, the dc drain current at V_{DS} = 25 volts is 20 A. For a 10 ms pulse and duty cycle of 50%, Figure 12 gives an r(t) of 0.6; then, with P_D = 500 watts at 25°C and $R_{\theta JC}$ = 0.5°C/W.

$$I_D = 20 \times \frac{150 - 80}{500 \times 0.25 \times 0.6} = 18.6\ A$$

The switching safe operating area in Figure 11 is the boundary that the load line may traverse without incurring damage to the device. The fundamental limits are the maximum rated peak drain current I_{DM}, the minimum drain-to-source breakdown voltage $V_{BR(DSS)}$ and the maximum rated junction temperature. The boundaries are applicable for both turn-on and turn-off of the devices for rise and fall times of less than one microsecond.

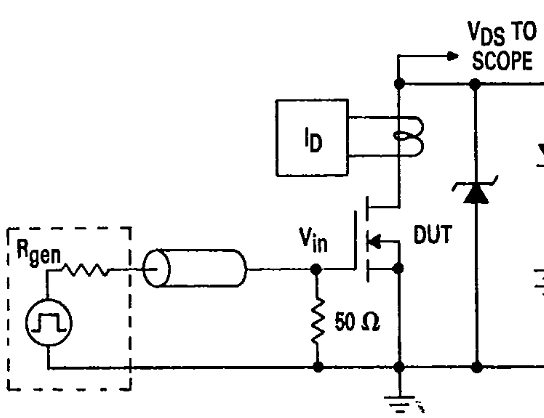


Figure 13. Inductive Load Switching Circuit

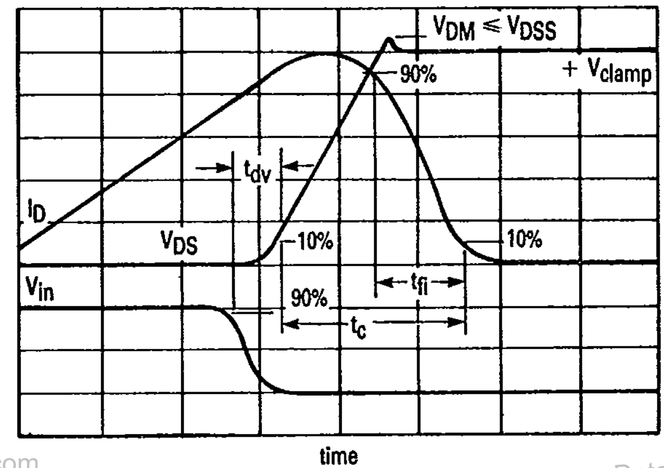
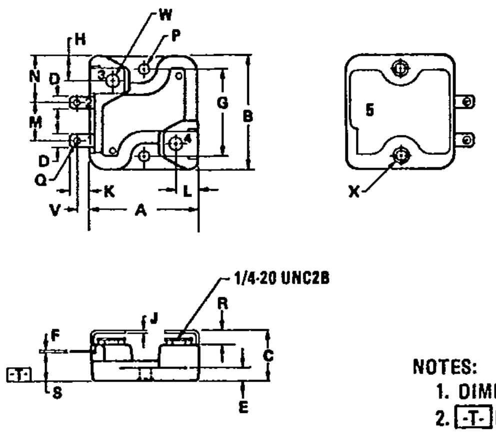


Figure 14. Clamped Inductive Load Switching Waveforms

OUTLINE DIMENSIONS



CASE 346-01
MO-040AA

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	53.09	53.84	2.090	2.120
B	55.37	56.39	2.180	2.220
C	–	26.67	–	1.050
D	6.10	6.60	0.240	0.260
E	6.60	7.11	0.260	0.280
F	0.71	0.81	0.028	0.032
G	43.31 BSC		1.705 BSC	
H	12.57	12.82	0.495	0.505
J	1.52	1.62	0.060	0.064
K	9.50	9.75	0.374	0.384
L	10.21	10.46	0.402	0.412
M	18.92	19.18	0.745	0.755
N	23.67	23.93	0.932	0.942
P	5.08	5.21	0.200	0.205
Q	3.53	3.78	0.139	0.149
R	6.76	7.26	0.266	0.286
S	14.73	15.24	0.580	0.600
V	5.33	5.84	0.210	0.230
W	6.40	6.65	0.252	0.262
X	7.37	7.87	0.290	0.310

STYLE 1:
PIN 1. BASE
2. EMITTER
3. EMITTER
4. COLLECTOR
5. COLLECTOR

NOTES:
1. DIMENSION A AND B ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLES: ⌖ ⌀ 0.36 (0.014) Ⓜ | T | A Ⓜ | B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

CONSIDERATION IN DESIGNING WITH POWER MOSFETS

Depending on the frequency of operation, certain precautions must be taken to insure optimum reliability. When switching near the device maximum frequency, the high current and very fast switching capability of this device necessitates the use of the following protective measures:

Note 1 As in any wideband circuit, good RF layout techniques must be maintained, i.e., short lead lengths, adequate ground planes and decoupled power supplies.

Note 2 All overvoltage protection circuitry — free wheeling diodes, zeners, MOVs, snubber networks — should be placed directly between the drain-source or between the drain and a good, low inductance ac ground.

Note 3 Since most "real world" loads are inductive, the fast turn-off peak flyback voltage ($e = L\ di/dt$) must not exceed the $V_{BR(DSS)}$ rating, an instantaneous voltage limit. The protective circuitry, including parasitics, must have response times commensurate with the Power MOSFET switching speed, e.g., rectifiers must have very short recovery times. The forward recovery time t_{fr}, overshoot voltage $V_{FM(DYN)}$ and reverse recovery time t_{rr} should be low to minimize the switching stress on the transistor.

Note 4 Even with good RF layout and ideal clamping below the maximum $V_{(BR)DSS}$ of the device, significant potentials may be generated across the package drain and source parasitic inductances during rapid turn off of a large magnitude of current. These induced voltages which are internal to the package add to the clamp voltage. Therefore, to protect the chips from excessive voltage, the di_D/dt must be limited in accordance to the peak voltage seen across the terminals of the device. The *MAXIMUM ALLOWABLE* di_D/dt must be limited in accordance to the peak V_{DS} appearing at the device terminals as shown in Figure 15.

For applications requiring slower switching speeds, increasing the gate drive impedance will increase the switching times. This can be accomplished by adding a resistor in series with the gate.

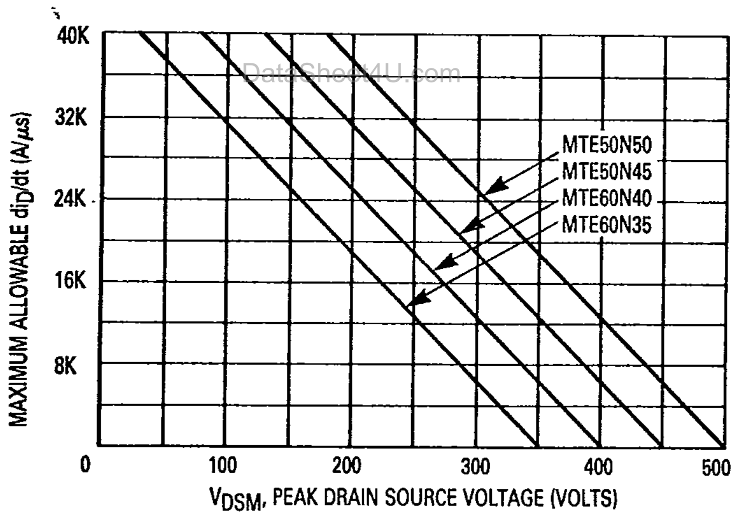


Figure 15. Maximum Allowable di_D/dt versus Drain Source Voltage

TMOS SOURCE-TO-DRAIN CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 16. Reversal of the drain voltage will cause current flow in the reverse direction. This diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turnon and reverse recovery times are given.

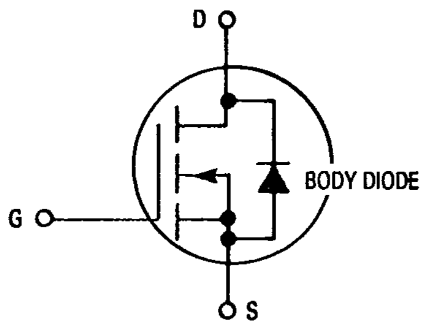


Figure 16. TMOS FET With Source-To-Drain Diode

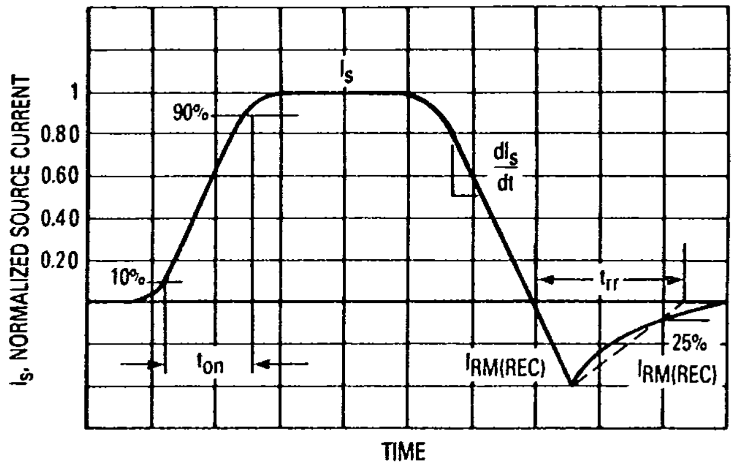
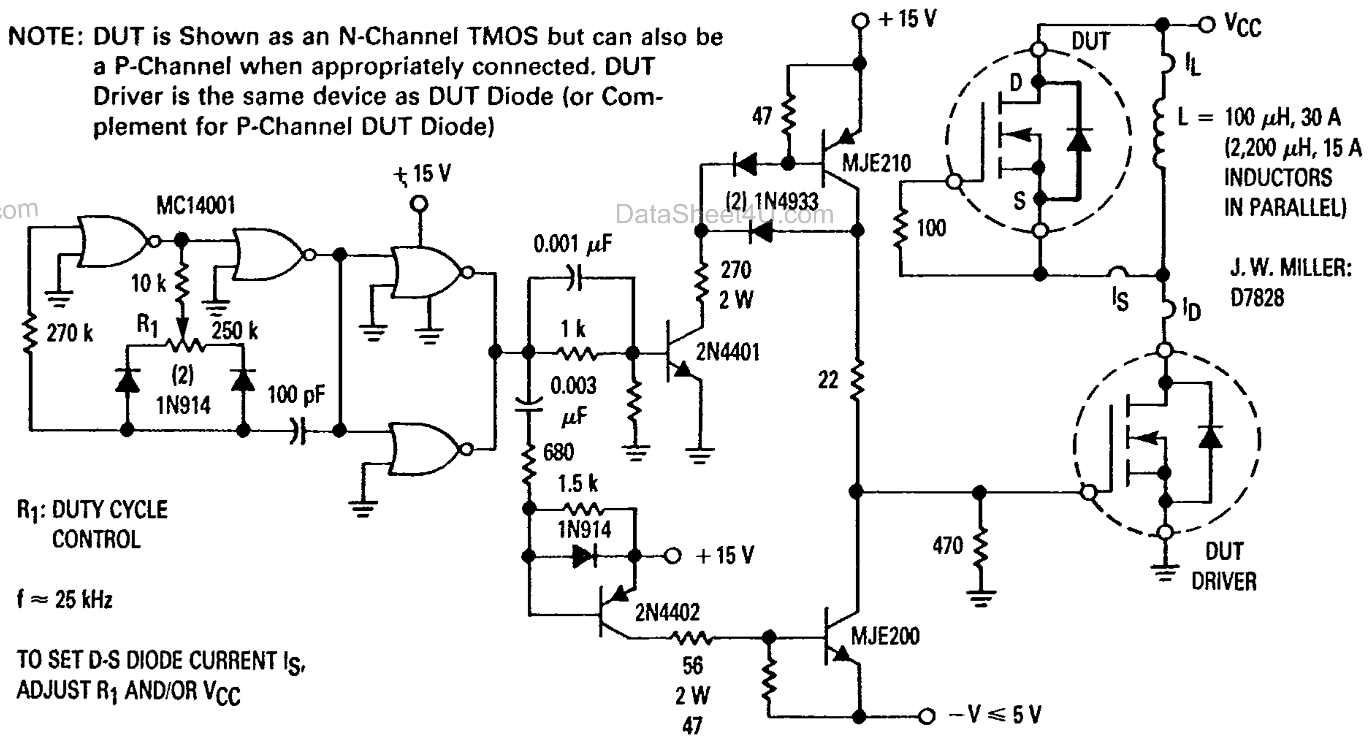


Figure 17. Diode Switching Waveform

NOTE: DUT is Shown as an N-Channel TMOS but can also be a P-Channel when appropriately connected. DUT Driver is the same device as DUT Diode (or Complement for P-Channel DUT Diode)



R1: DUTY CYCLE CONTROL

f ≈ 25 kHz

TO SET D-S DIODE CURRENT I_S, ADJUST R_1 AND/OR V_{CC}

Figure 18. TMOS Diode Switching Test Circuit