

NEC**MOS FIELD EFFECT TRANSISTOR
2SK3713****SWITCHING
N-CHANNEL POWER MOS FET****DESCRIPTION**

The 2SK3713 is N-channel MOS Field Effect Transistor designed for high voltage and high speed switching applications.

FEATURES

- Super high $V_{GS(off)}$: $V_{GS(off)} = 3.8$ to 5.8 V
- Low C_{rss} : $C_{rss} = 6.5$ pF TYP.
- Low Q_G : $Q_G = 25$ nC TYP.
- Low on-state resistance:
 $R_{DS(on)} = 0.83 \Omega$ MAX. ($V_{GS} = 10$ V, $I_D = 5$ A)

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3713-SK	TO-262

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0$ V)	V_{DSS}	600	V
Gate to Source Voltage ($V_{DS} = 0$ V)	V_{GSS}	± 30	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 10	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 35	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	100	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	1.5	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to $+150$	$^\circ\text{C}$
Single Avalanche Current ^{Note2}	I_{AS}	10	A
Single Avalanche Energy ^{Note2}	E_{AS}	6	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 100$ V, $L = 100 \mu\text{H}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0$ V

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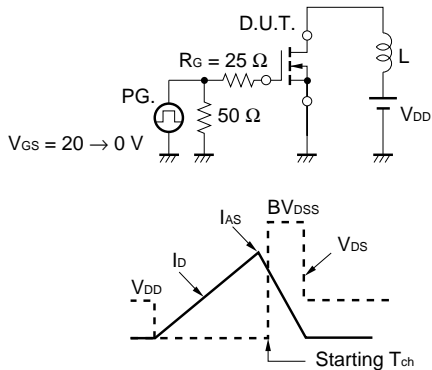
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

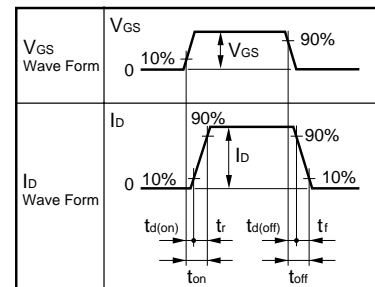
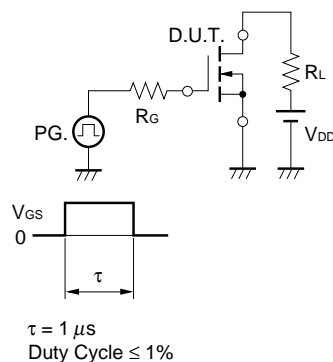
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 600 V, V _{GS} = 0 V			100	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±30 V, V _{DS} = 0 V			±100	nA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	3.8	4.8	5.8	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = 10 V, I _D = 5 A	2.5	4.6		S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)}	V _{GS} = 10 V, I _D = 5 A		0.68	0.83	Ω
Input Capacitance	C _{iss}	V _{DS} = 10 V		1460		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		250		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		6.5		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 150 V, I _D = 5 A		26		ns
Rise Time	t _r	V _{GS} = 10 V		8.5		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		30		ns
Fall Time	t _f			5.2		ns
Total Gate Charge	Q _G	V _{DD} = 450 V		25		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		12		nC
Gate to Drain Charge	Q _{GD}	I _D = 10 A		9		nC
Body Diode Forward Voltage ^{Note}	V _{F(S-D)}	I _F = 10 A, V _{GS} = 0 V		0.9	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 10 A, V _{GS} = 0 V		450		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		4.0		μC

Note Pulsed

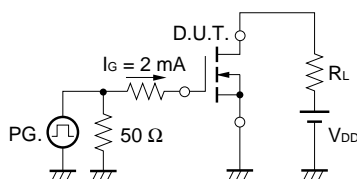
TEST CIRCUIT 1 AVALANCHE CAPABILITY



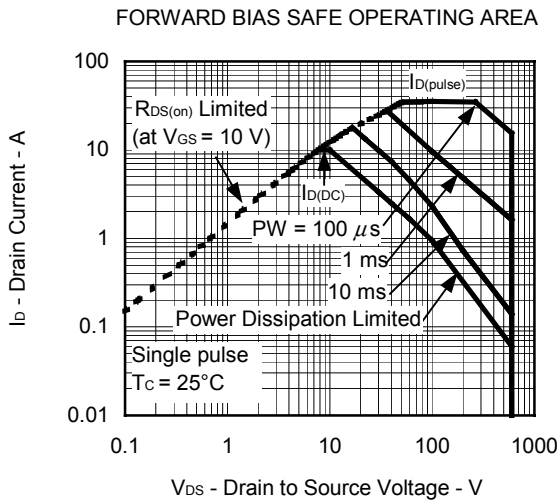
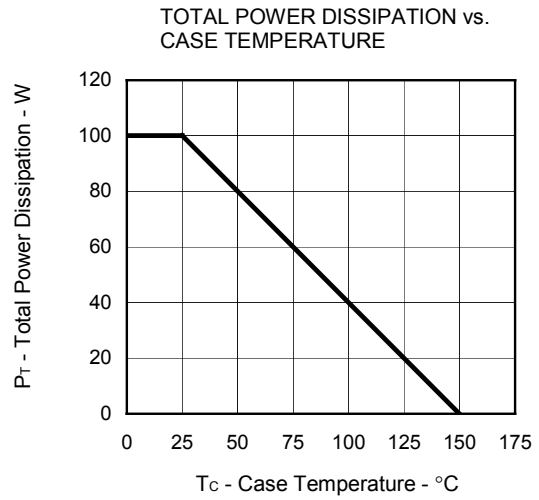
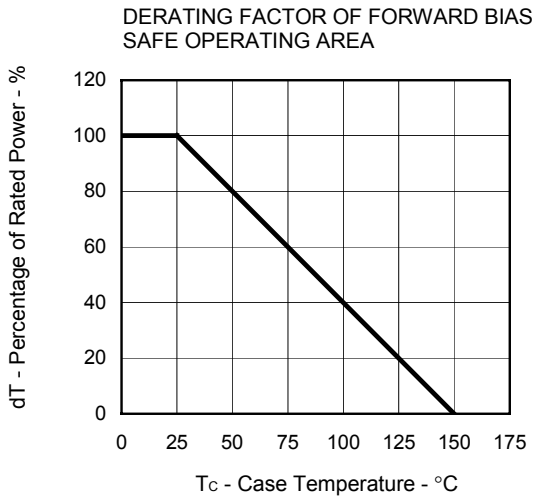
TEST CIRCUIT 2 SWITCHING TIME



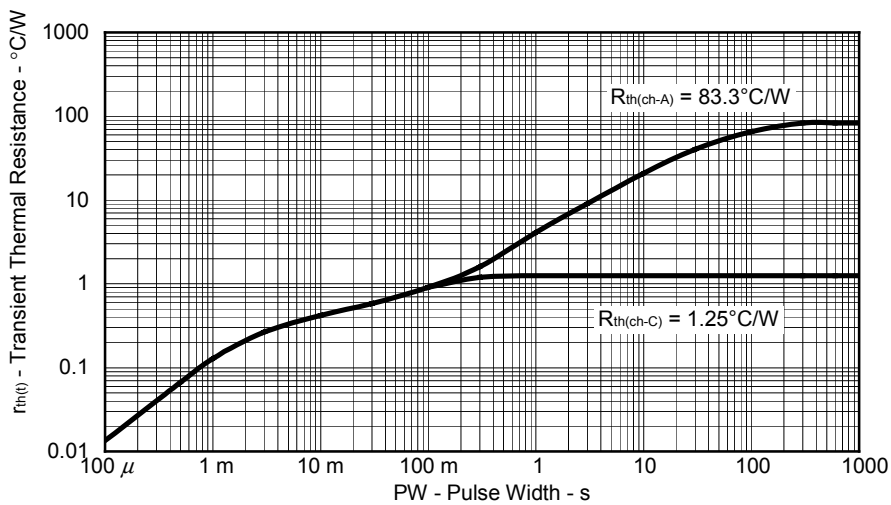
TEST CIRCUIT 3 GATE CHARGE



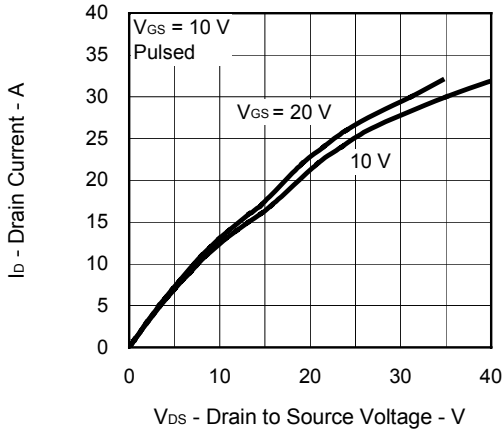
TYPICAL CHARACTERISTICS (T_A = 25°C)



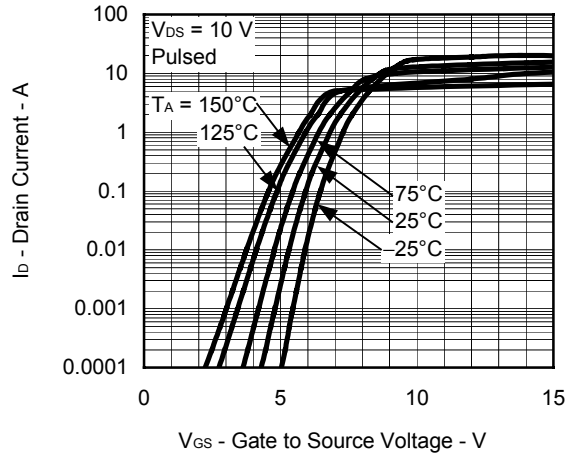
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



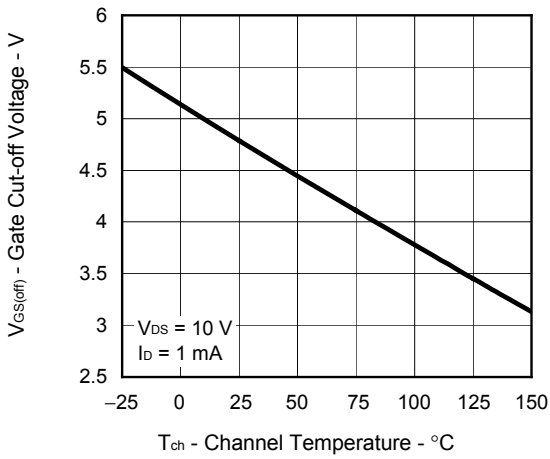
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



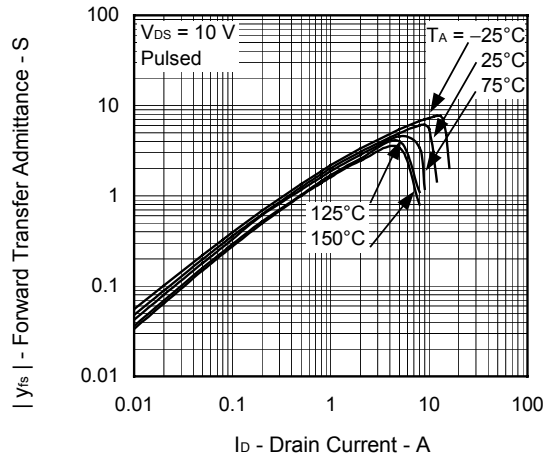
FORWARD TRANSFER CHARACTERISTICS



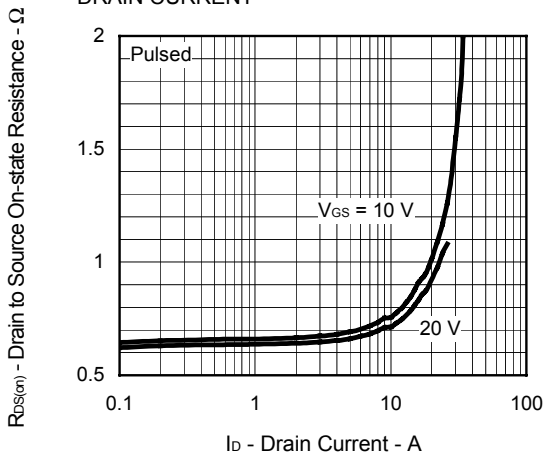
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



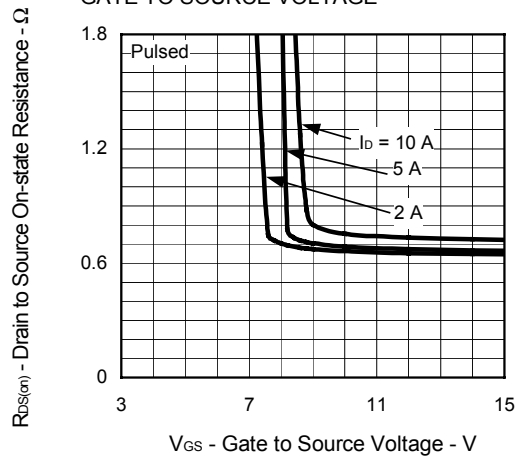
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



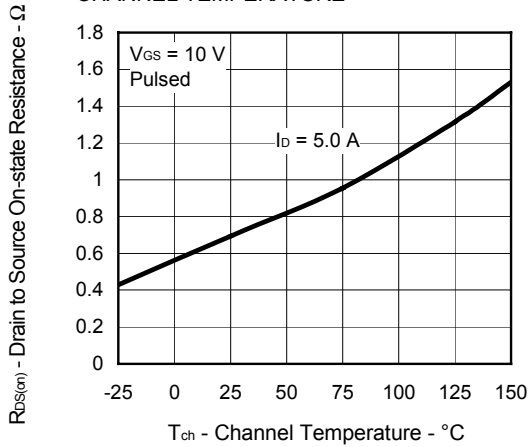
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



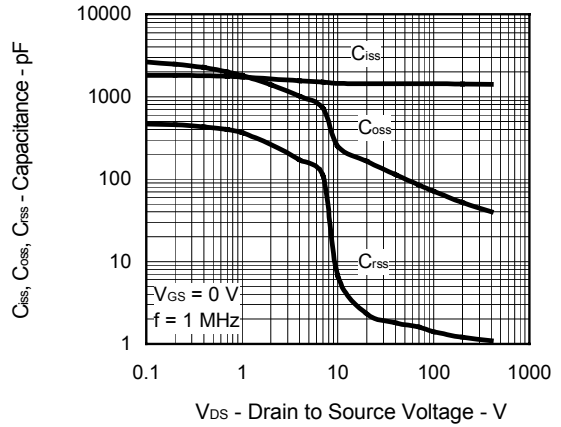
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



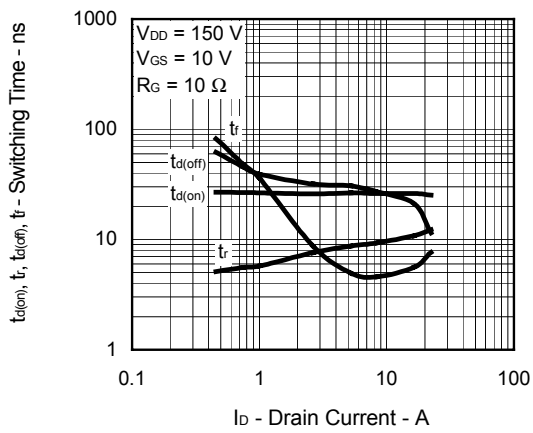
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



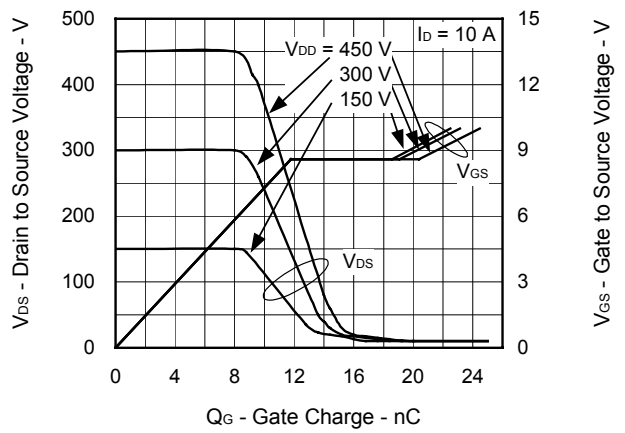
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



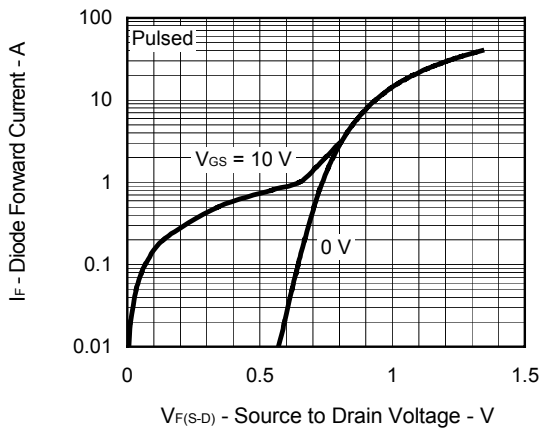
SWITCHING CHARACTERISTICS



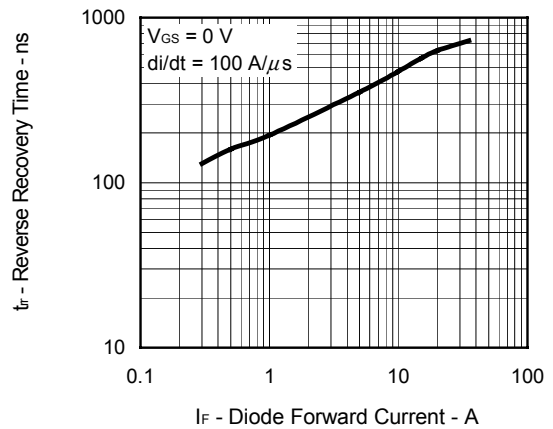
DYNAMIC INPUT/OUTPUT CHARACTERISTICS

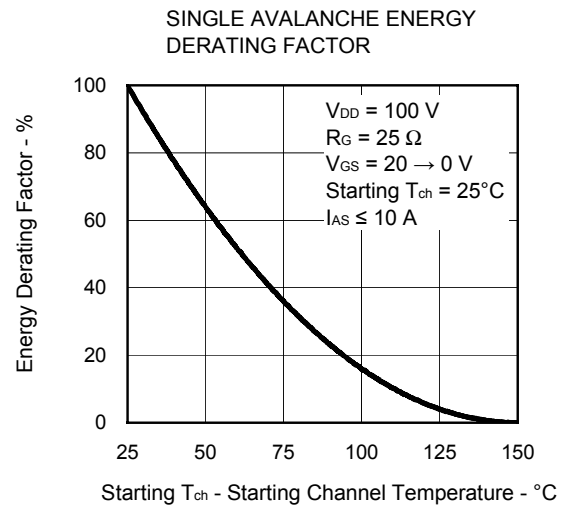
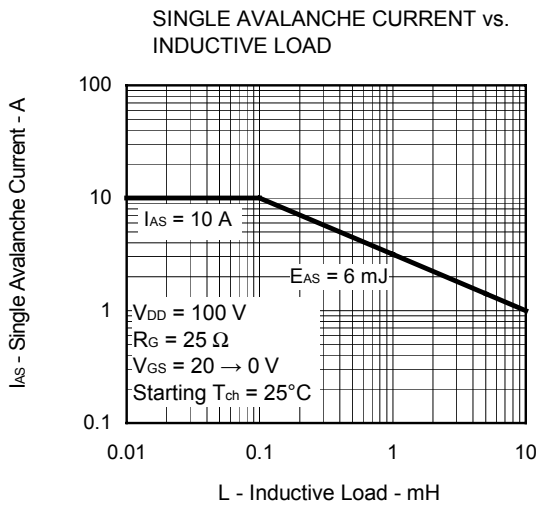


SOURCE TO DRAIN DIODE FORWARD VOLTAGE



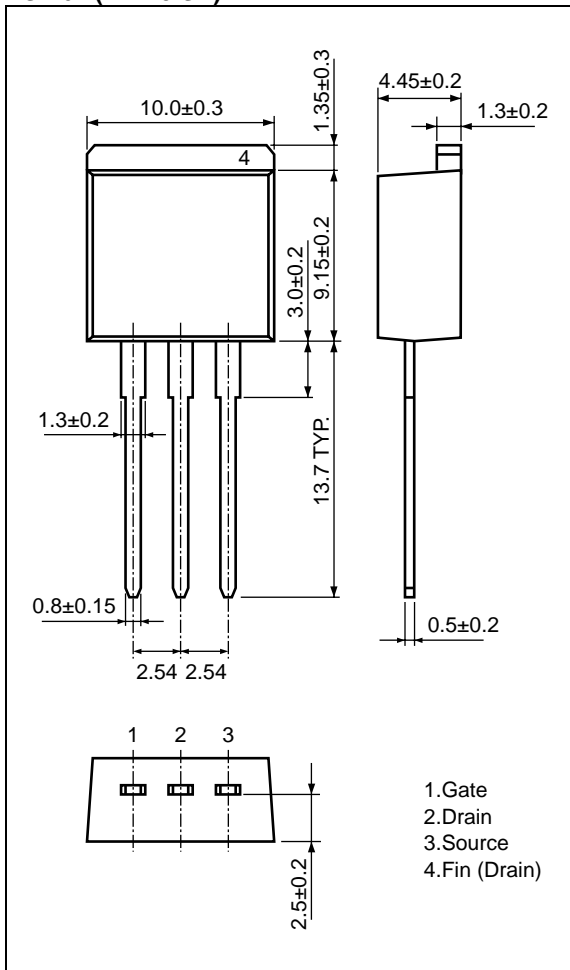
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



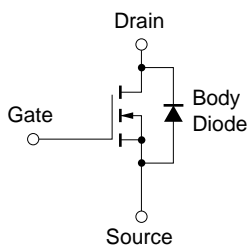


PACKAGE DRAWING (Unit: mm)

TO-262 (MP-25 SK)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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