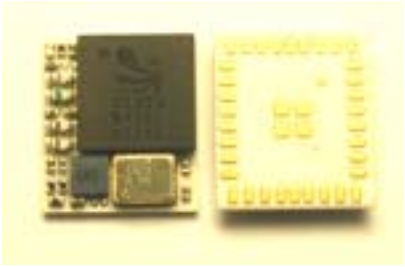
DLBM-CA120 (16Kbit EEPROM)
DLBM-CA121 (64Kbit EEPROM)
Bluetooth™ Module Class 2

A Class 2 Bluetooth module suitable for wireless Audio applications.



1.FEATURES:

- ***Suitable for Headset, MP3… applications.***
- ***Reducing the size and thickness greatly using high-density packaging technology.***
- ***High sensitivity to achieve better performance.***
- ***Compliant to various interfaces: UART, USB, PIO...***
- ***Wide operating temperature range: -30~+80℃.***

2.Device diagram

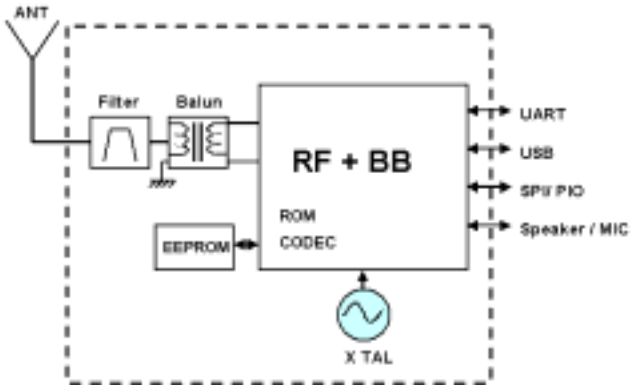


Figure 1. DLBM-CA120/CA121 Block Diagram

3.General Specification

Bluetooth™ Specification	Version 1.1
Frequency	2402~2480MHz
Modulation	FHSS/GFSK
Transmission rate	721kbps
Receive sensitivity	-83dBm
Maximum output power	+4dBm(Class 2)
Operating Voltage	1.8V or 2.2~3.6V
Operating temperature	-30~+80℃
Antenna Impedance	50 ohm
Package size	9.1*7.9*1.5mm
Talk time (Audio application)	*Up to 4.5 hours (120mA Battery)
Stand-by time (Audio application)	*Up to 200 hours (120mA Battery)

* Base on application circuit figure 7*

4.Rating

	Min	Max	Unit
Storage Temperature	-40	+150	℃
VDD_1.8V	-0.4	+1.9	V
VDD_IO	-0.4	+3.6	V
VREG_IN	-0.4	+4.2	V

5.Recommended Operating conditions

	Min	Max	Unit
Guaranteed RF performance range	-10	+70	℃
VDD_1.8V	+1.7	+1.9	V
VDD_IO	+2.7	+3.6	V
VREG_IN	+2.2	+4.2	V

6.Interface

Interface	Description
Antenna	External Antenna 50 ohm
UART Interface	TX,RX,RTS,CTS(9600bps~1.5Mbps)
SPI Interface	Synchronous Serial Interface for firmware download
PIO Interface	9 terminals

7.Power Supply Diagram

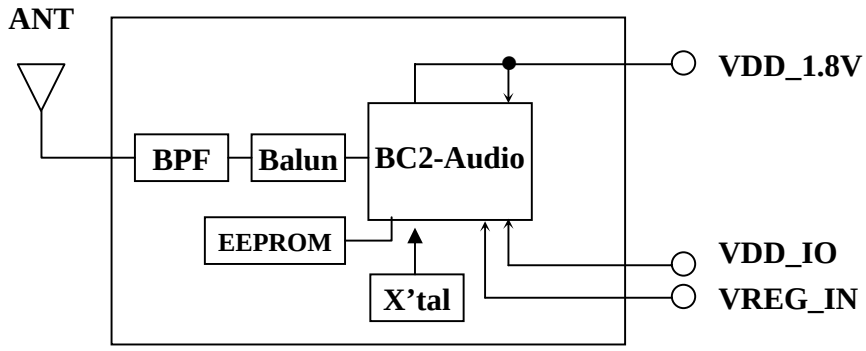


Figure 2. Power Supply Diagram

Terminal	VDD=3.0V	VDD=1.8V
VDD_1.8V	NC	1.7 to 1.9V
VDD_IO	2.7 to 3.6V	2.7 to 3.6V
VREG_IN	2.7 to 3.6V	NC

8.RF Characteristics

Operating Condition: +25℃, VDD=1.8V

RF Characteristics	Min.	Typ.	Max.	Unit
1. Fequency Range		2400 ~ 2483.5		MHz
2. Output Power	-6	1.5	4	dBm
3. Sensitivity at 0.1% BER				
1) 2402MHz	-70	-83		dBm
2) 2441MHz	-70	-83		dBm
3) 2480MHz	-70	-83		dBm
4. Maximum Input Level (BER≦0.1%)	-20	0		dBm

5. Adjacent channel selectivity				
1) C/I F=F0 + 1MHz		-4	0	dB
2) C/I F=F0 - 1MHz		-4	0	dB
3) C/I F=F0 + 2MHz		-35	-30	dB
4) C/I F=F0 - 2MHz		-21	-20	dB
5) C/I F≧F0 + 3MHz		-45		dB
6) C/I F≦F0 - 5MHz		-45		dB
7) C/I F=FImage		-18	-9	dB
6. Adjacent channel transmit power				
1) F=F0 ± 2MHz		-35	-20	dBc
2) F=F0 ± 3MHz		-55	-40	dBc
7. Modulation Characteristics				
1) Modulation Δf1avg	140	165	175	kHz
2) Modulation Δf2max	115	155		kHz
8. Initial Carrier Frequency Tolerance				
1) 2402MHz	-75	-12	75	kHz
2) 2441MHz	-75	-11	75	kHz
3) 2480MHz	-75	-10	75	kHz
9. Carrier Frequency Drift				
1) 1slot	-20	9	20	kHz
2) 5slot	-25	10	25	kHz
4) Drift rate	-20	6.5	20	KHz/50us
10. 20dB Bandwidth for modulated carrier				
1) 2402MHz		879	1000	KHz
2) 2441MHz		816	1000	KHz
3) 2480MHz		819	1000	KHz
11.C/I co - channel		9	11	dB

9.Audio Codec

The DLBM-CA120 CODEC is compatible with the direct speaker drive and microphone input using a minimum number of external components. It is primarily intended for voice applications and it is fully operational from a single 1.8 Volt power supply. A fully differential architecture has been implemented for optimal power supply rejection and low noise performance. The digital format is 15-bit/sample linear PCM with a data rate of 8kHz.

The CODEC has an input stage containing a microphone amplifier, variable gain amplifier and a Σ-Δ ADC. Its output stage contains a DAC, low-pass filter and output amplifier. The CODEC functional diagram is shown below:

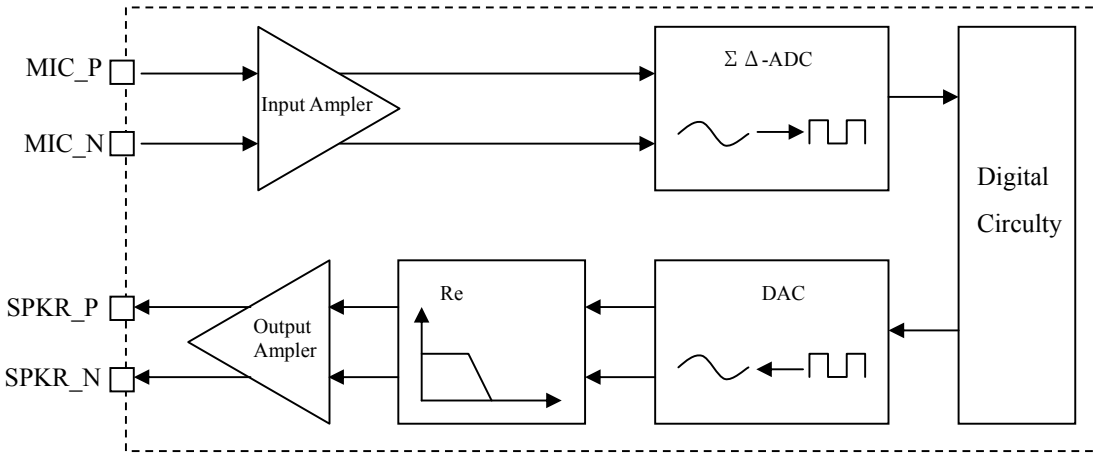


Figure 3. DLBM-CA120 CODEC Diagram

10. Input Stage

A low noise variable gain amplifier amplifies the signal difference between inputs MIC_N and MIC_P. The input may be from either a microphone or line. The amplified signal is then digitised by a Σ-Δ ADC. The high frequency single bit output from the ADC is converted to 15-bit 8kHz linear PCM data.

The gain is programmable via a PSKEY and has a 42dB range with 3dB resolution. At maximum gain the full scale input level is 3mV rms. A bias network is required for operation

with a microphone whereas the line input may be simply a.c. coupled. The following sections explain each of these modes. Single ended signals are supported by DLBM-CA120: a single ended signal may be driven into either MIC_N or MIC_P with the undriven input coupled to ground by a capacitor.

At the maximum gain the signal to noise ratio is better than 60dB and distortion is better than –75dB relative to a full-scale sine wave. At lower gain settings (such as used for line input) the signal to noise ratio improves to better than –75dB.

11. Microphone Input

The DLBM-CA120 CODEC has been designed for use with microphones that have sensitivities between –60 and –40dBV. The sensitivity of –60dBV is equivalent to a microphone output of 1 μA when presented with an input level of 94dB SPL and loaded with 1kΩ. The microphone should be biased as shown:

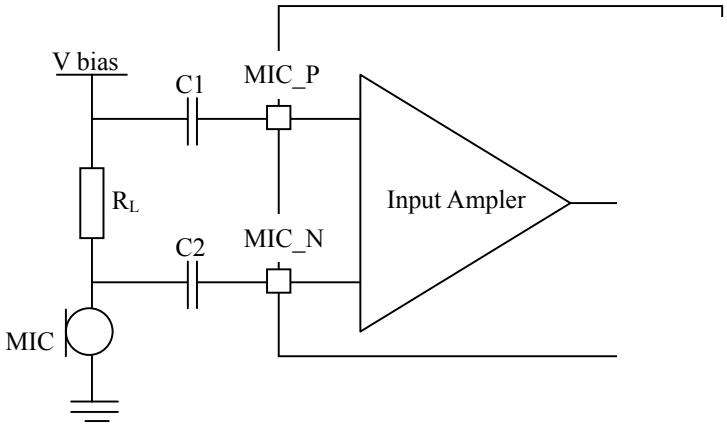


Figure 4. DLBM-CA120 Microphone Biasing

The input impedance at MIC_N and MIC_P is typically 20kΩ. C1 and C2 should be 47nF. R_L sets the microphone load impedance and is normally between 1 and 2kΩ. V bias should be chosen to suit the microphone and have sufficient low noise. It may be obtained by filtering the output of a PIO line.

12. Line Input

If the input gain is set to less than 21dB DLBM-CA120 automatically selects line input mode. In this mode the input impedance at MIC_N and MIC_P is increased to 130kΩ typical. At the minimum gain setting the maximum input signal level is 380 mV rms. Figures 5 show two circuits for line input operation and show connections for either differential or single ended inputs.

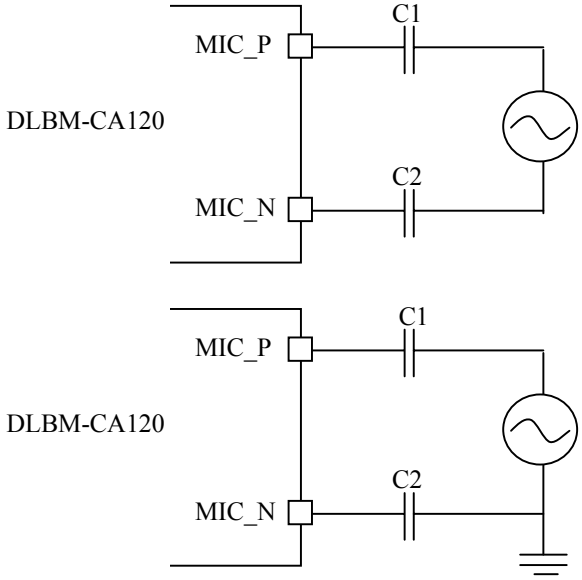


Figure 5. Single-ended Microphone Input

Note: C1 and C2 should be 15nF.

13.Output Stage

The digital data is converted to an analogue value by a DAC, then it is filtered prior to amplification by the output amplifier and it is available as a differential signal between SPKR_P and SPKR_N. the output amplifier is capable of driving a speaker directly if its impedance is greater than or equal to 8Ω. The amplifier is stable with capacitive loads up to 500pF.

The gain is programmable with a range of 21dB and a resolution of 3dB. Maximum output level is typically 700 mV rms for high impedance loads, or 20mA rms for low impedance loads. The signal to noise is better than 70dB and the distortion is less than –75dB.

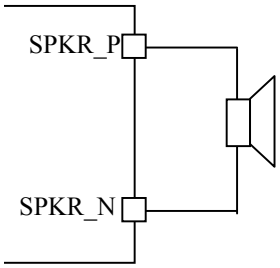


Figure 6. Speaker Output

14.Reference design for Headset application

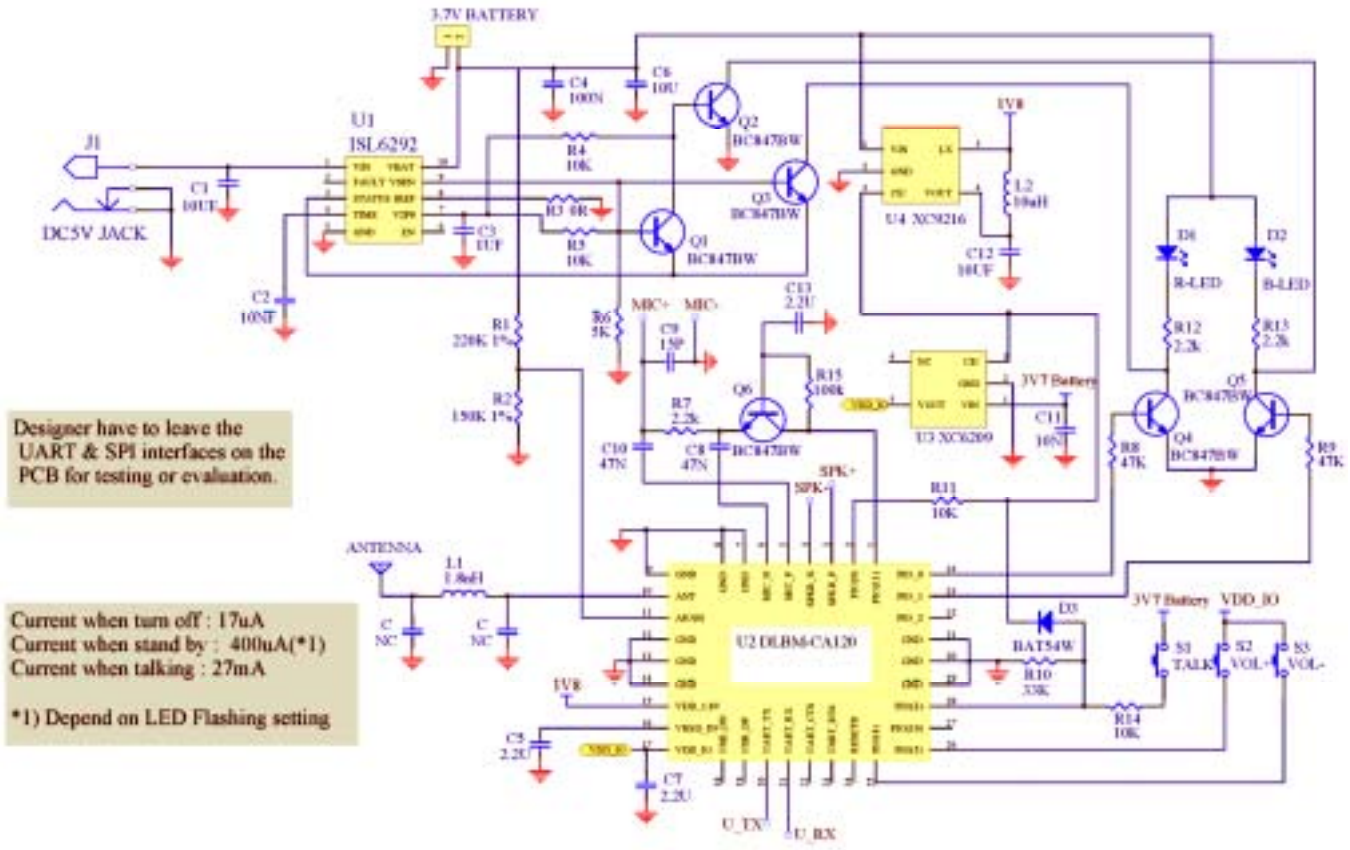


Figure 7. Headset application circuit

Important: The circuit is offered without warranty and Delta is unable to accept any liability for direct or consequential loss associated with their use. It is therefore important for designers to ensure that their Bluetooth headset design is properly evaluated in a Design Verification Test. The results of the Design Verification Test should be used to assess the suitability of the headset for manufacture.

15. RECOMMENDED REFLOW PROFILE

The temperature rise to 150°C for preliminary heating shall be made for 30 seconds or longer
The preliminary heating shall be done at the temperature of 160°C±10°C for 60 ~ 90 seconds.
The heating shall be at the temperature of 200°C or higher For 20 ~ 40 seconds and the peak temperature shall be 230°C±5°C

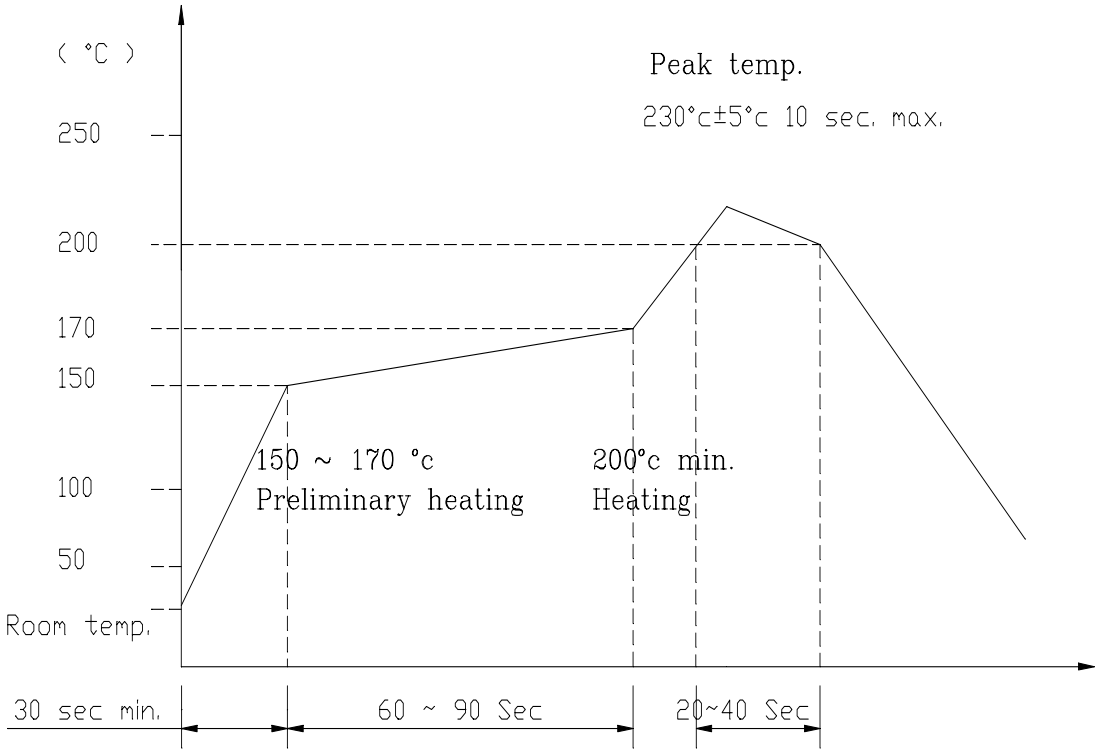


Figure 8. REFLOW PROFILE

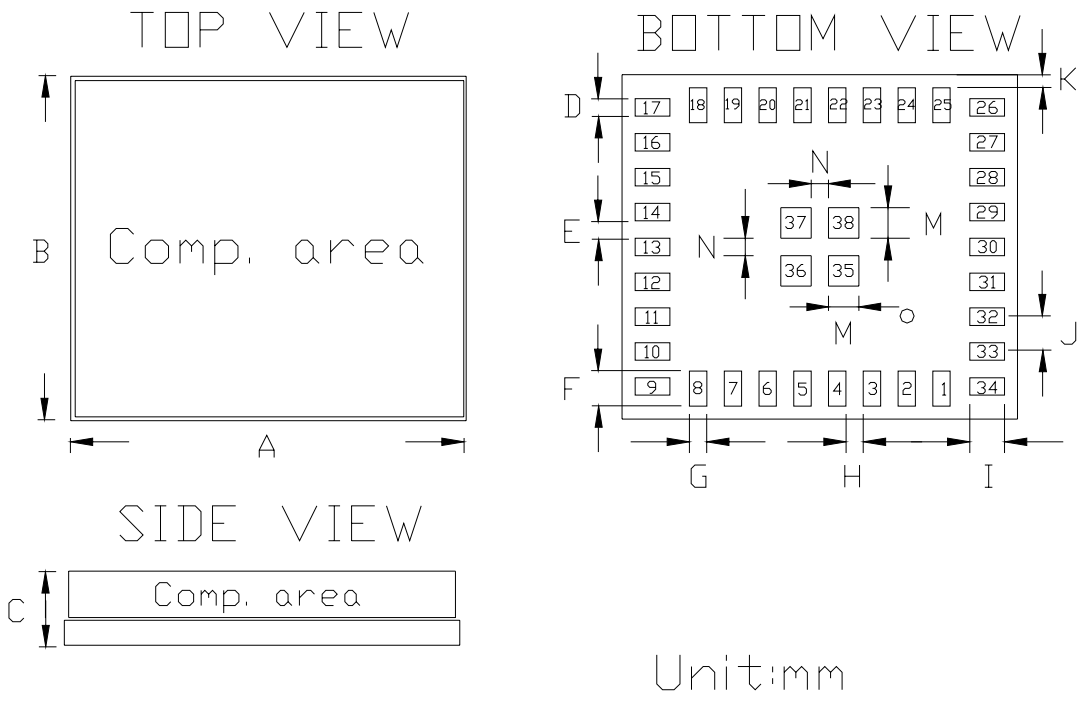
16.Pin description

Pin No.	Name	Description
1	PIO_11	Programmable I/O terminal
2	PIO_9	Programmable I/O terminal
3	SP+	Speaker output positive
4	SP-	Speaker output negative
5	MIC+	Microphone input positive
6	MIC-	Microphone input negative
7	Gnd	
8	Gnd	
9	Gnd	
10	ANT	RF input/output
11	AIO_0	Programmable input/output
12	Gnd	
13	Gnd	
14	Gnd	
15	Vdd_1.8V	Refer to Power supply diagram
16	VREG_IN	Refer to Power supply diagram

17	VDD_IO	Refer to Power supply diagram
18	USB_DN	USB data minus
19	USB_DP	USB data plus with selectable internal 1.5kohm pull-up resistor
20	UART_TX	UART data output active high
21	UART_RX	UART data input active high
22	UART_CTS	UART clear to send active low
23	UART_RTS	UART request to send active low
24	Reset_B	Reset if low
25	PIO_4	Programmable input/output line
26	PIO_5	Programmable input/output line
27	PIO_10	Programmable input/output line
28	PIO_3	Programmable input/output line
29	Gnd	
30	Gnd	
31	Gnd	
32	PIO_2	Programmable input/output line
33	PIO_1	Programmable input/output line
34	PIO_0	Programmable input/output line
35	SPI_MOSI	Serial Peripheral Interface data input

36	SPI_MISO	Serial Peripheral Interface data output
37	SPI_CLK	Serial Peripheral Interface clock
38	SPI_CSB	Chip select for Serial Peripheral Interface, active low

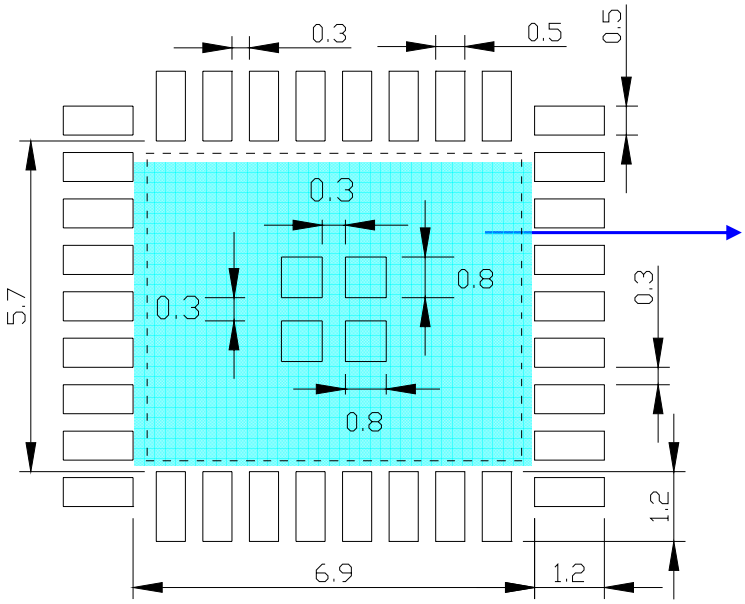
17.Dimensions (mm)



A	9.1±0.2	E	0.35±0.15	I	0.8±0.1	N	0.4±0.1
B	7.9±0.2	F	0.8±0.1	J	0.8±0.1		
C	1.5±0.2	G	0.4±0.1	K	0.3±0.1		
D	0.45±0.15	H	0.4±0.1	M	0.7±0.1		

Figure 9. Output pin dimensions

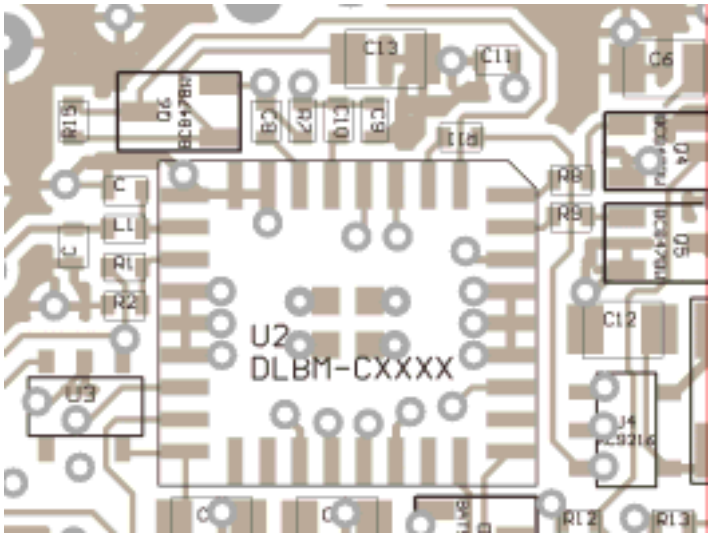
18. Layout Guide

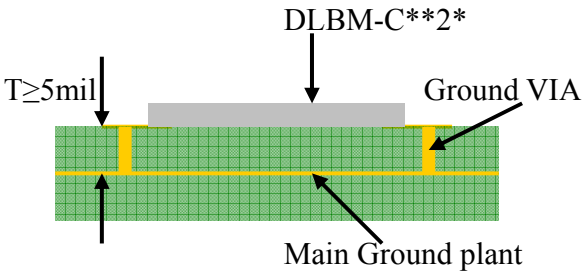


Don't place the ground on the top layer (Inside area)

Figure 10. Land Pattern

Unit: mm





Side View

Figure 11. Layout Example

19. Record of changes

Date	Reason of change	Engineer
Dec 16, 2004'	1) Update application circuit 2) Create DLBM-CA121 64K EEPROM version 3) Includes SPI pin definition	Emerson Shih
Dec 30, 2004'	Application circuit upgrade. (Low current consumption version)	Emerson Shih
Jan 17, 2005'	General Specification & Layout Guide correction	Emerson Shih
April 20, 2005'	Includes pin dimension tolerance	Ming Wu
May 20, 2005'	Change dimensions tolerance 1) D：0.4±0.1➔0.45±0.15 2) E：0.4±0.1➔0.35±0.15	Leo Chuang

Contact information:

Website: http://www.deltaww.com
Email: Richard.meng@delta.com.tw
Tel No.: 886-3-3591968#2930