DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD482234, 482235

2M-Bit Dual Port Graphics Buffer

256K-WORD BY 8-BIT

Description

The μPD482234 and μPD482235 have a random access port and a serial access port. The random access port has a 2M-bit (262, 144 words × 8 bits) memory cell array structure. The serial access port can perform clock operations of up to 55 MHz from the 4K-bit data register (512 words × 8 bits).

To simplify the graphics system design, the split data transfer function and binary boundary jump function have been adopted so that the number of split data registers can be programmed with the software during serial read/write operations.

The μPD482235 is provided with the hyper page mode, an improved version of the fast page mode of the μPD482234. The random access port can input and output data by $\overline{\text{CAS}}$ clock operations of up to 33 MHz.

Features

Dual port structure (Random access port, Serial access port)

● Random access port (262, 144-word × 8-bit structure)

μPD482234

	μPD482234-60	μPD482234-70	μPD482234-80
$\overline{\text{RAS}}$ access time	60 ns(MAX.)	70 ns(MAX.)	80 ns(MAX.)
Fast page mode cycle time	40 ns(MIN.)	45 ns(MIN.)	50 ns(MIN.)

μPD482235

	μPD482235-60	μPD482235-70	μPD482235-80
$\overline{\text{RAS}}$ access time	60 ns(MAX.)	70 ns(MAX.)	80 ns(MAX.)
Hyper page mode cycle time	30 ns(MIN.)	35 ns(MIN.)	40 ns(MIN.)

- Flash write function**Note**
- Block write function (4 columns)**Note**
- Mask write (Write-per-bit function)
- 512 refresh cycles /8 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh

Note Write-per-bit can be specified.

- Serial access port (512 words × 8 bits organization)
  - Serial read/write cycle time

μPD482234-60, 482235-60	μPD482234-70, 482235-70	μPD482234-80, 482235-80
18 ns (MIN.)	22 ns (MIN.)	25 ns (MIN.)

  - Serial data read/write
  - Split buffer data transfer
  - Binary boundary jump function

Version A, F, and E

There are three versions, A, F, and E, to both the μPD482234 and μPD482235. These versions operate with different specifications.

- **Overview of each version**

μPD482234

The table below summarizes the operation of each version of the μPD482234.

Item	Reference	Version A	Versions F and E
Specifying a column for data transfer during split data transfer cycle	**3.2 Split Data Transfer Method**	"MSB Don't Care" only	Version F: MSB Don't Care Version E: MSB Care
Selecting a new mask data method during mask write cycle	**2.8.2 Selecting Mask Data**	Option reset cycle only	Both option reset cycle and new mask selection can be used.

μPD482235

The table below summarizes the operation of each version of the μPD482235.

Item	Reference	Version A	Versions F and E
Specifying a column for data transfer during split data transfer cycle	**3.2 Split Data Transfer Method**	"MSB Don't Care" only	Version F: MSB Don't Care Version E: MSB Care
Selecting a new mask data system during mask write cycle	**2.8.2 Selecting Mask Data**	Option reset cycle only	Both option reset cycle and new mask selection can be used.
$\overline{\text{OE}}$ control system during hyper page mode cycle	**2.4.1 Setting the Output to the High Impedance State**	Latched control (conforming to JEDEC)	Non-latched control

- **How to identify each version**

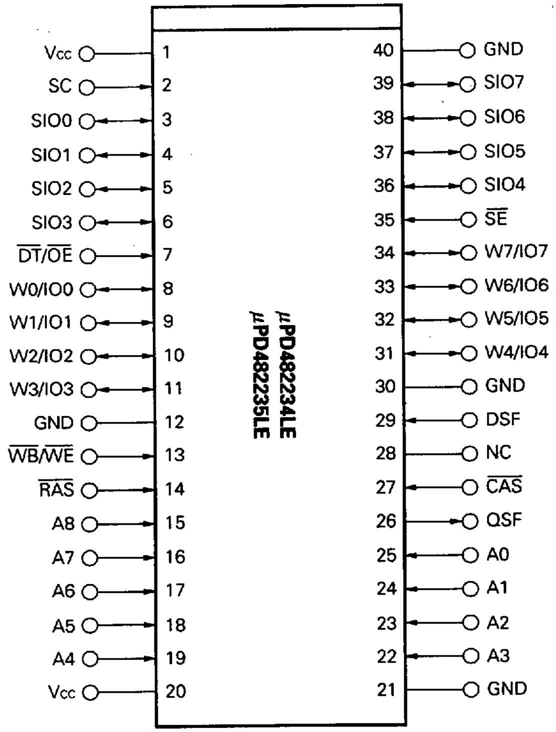
Each version is identified with its lot number (Refer to **7. Example of Stamping**).

Ordering Information

Part Number	$\overline{\text{RAS}}$ Access Time ns (MAX.)	Package	Page Mode
μPD482234LE-60	60	40-pin plastic SOJ (400mil)	Fast page mode
μPD482234LE-70	70		
μPD482234LE-80	80		
μPD482234G5-60	60	44-pin plastic TSOP (II) (400mil)	
μPD482234G5-70	70		
μPD482234G5-80	80		
μPD482235LE-60	60	40-pin plastic SOJ (400mil)	Hyper page mode
μPD482235LE-70	70		
μPD482235LE-80	80		
μPD482235G5-60	60	44-pin plastic TSOP (II) (400mil)	
μPD482235G5-70	70		
μPD482235G5-80	80		

Pin Configurations (Marking Side)

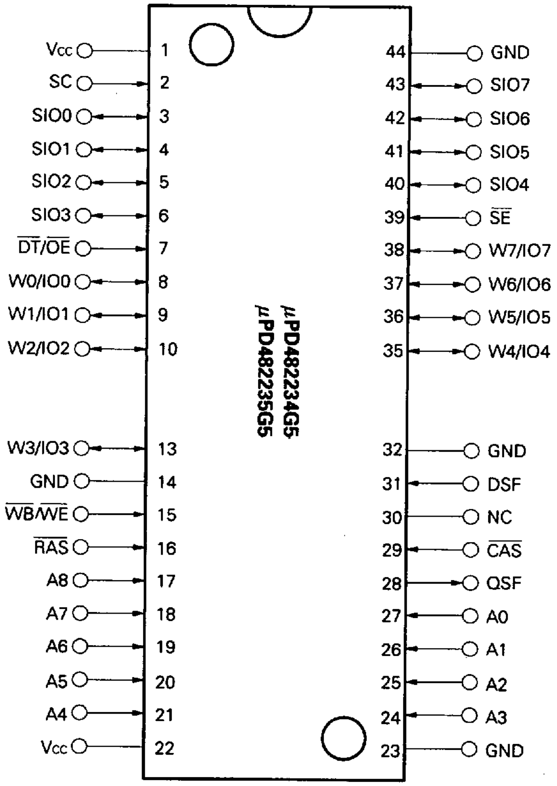
40-pin plastic SOJ (400 mil)



A0 to A8	: Address inputs
W0 to W7/IO0 to IO7	: Mask data selects/Data inputs and outputs
SIO0 to SIO7	: Serial data inputs and outputs
$\overline{\text{RAS}}$	: Row address strobe
$\overline{\text{CAS}}$	: Column address strobe
$\overline{\text{DT}}/\overline{\text{OE}}$	: Data transfer/Output enable
$\overline{\text{WB}}/\overline{\text{WE}}$	: Write-per-bit/Write enable
$\overline{\text{SE}}$	: Serial data input/Output enable
SC	: Serial clock
QSF	: Special function output
DSF	: Special function enable
Vcc	: Power supply voltage
GND	: Ground
NC^{Note}	: No connection

Note Some signals can be applied because this pin is not connected to the inside of the chip.

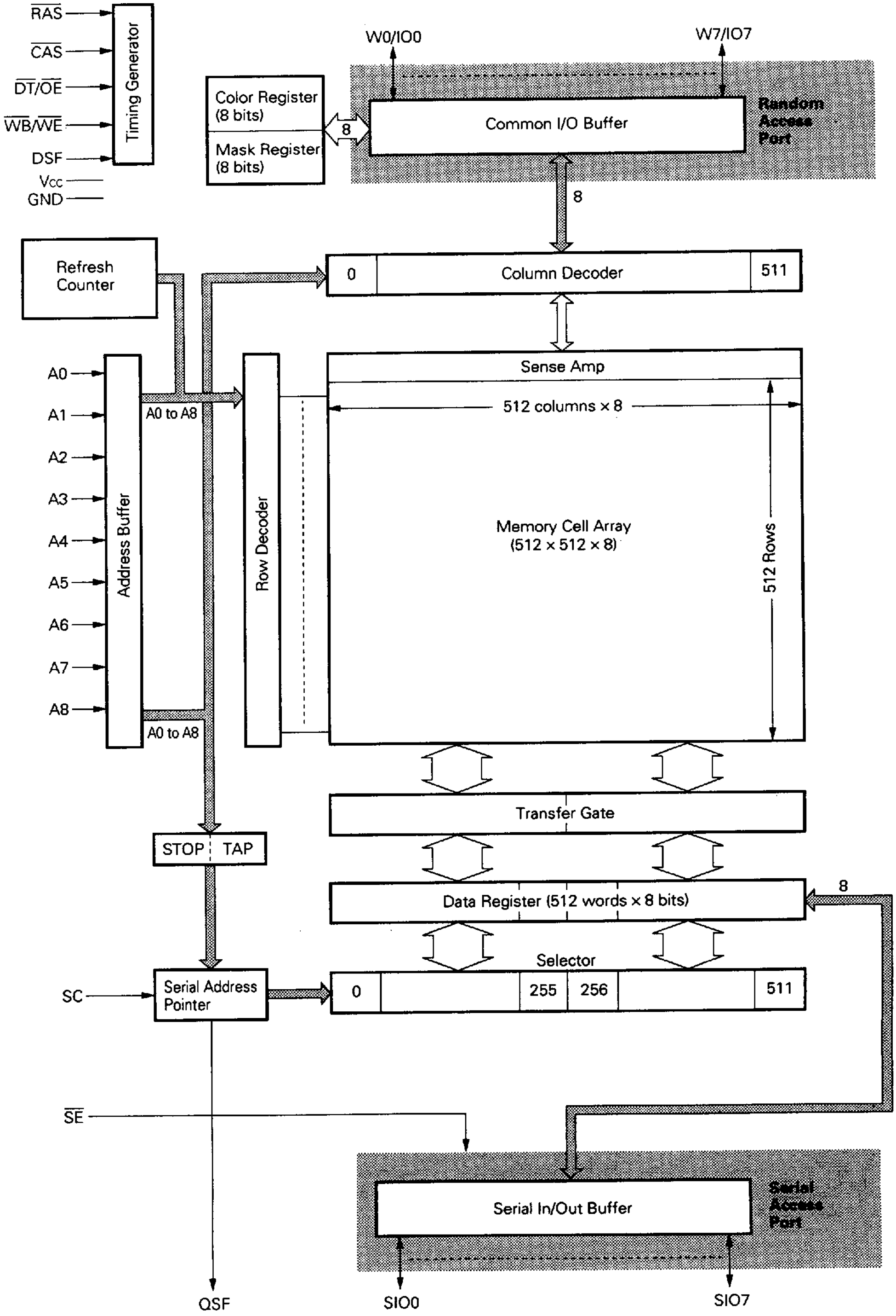
44-pin plastic TSOP (II) (400 mil)



A0 to A8 : Address inputs
W0 to W7/IO0 to IO7 : Mask data selects/Data inputs and outputs
SIO0 to SIO7 : Serial data inputs and outputs
$\overline{\text{RAS}}$: Row address strobe
$\overline{\text{CAS}}$: Column address strobe
$\overline{\text{DT}}/\overline{\text{OE}}$: Data transfer/Output enable
$\overline{\text{WB}}$, $\overline{\text{WE}}$: Write-per-bit/Write enable
$\overline{\text{SE}}$: Serial data input/Output enable
SC : Serial clock
QSF : Special function output
DSF : Special function enable
Vcc : Power supply voltage
GND : Ground
NC[Note] : No connection

Note Some signals can be applied because this pin is not connected to the inside of the chip.

Block Diagram



1. Pin Functions

This product is equipped with the $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WB}}/\overline{\text{WE}}$, $\overline{\text{DT}}/\overline{\text{OE}}$, A0 to A8, DSF, SC, $\overline{\text{SE}}$ inputs, QSF output, and W0 to W7/IO0 to IO7, SIO0 to SIO7 input/output pins.

(1/3)

Pin Name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	This signal latches the row addresses (A0 to A8), selects the corresponding word line, and activates the sense amplifier. It also refreshes the memory cell array of the one line (4,096 bits) selected from the row addresses (A0 to A8). It also serves as the signal which selects the following operations. • Write-per-bit • Flash write • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh • Split data transfer
$\overline{\text{CAS}}$ (Column address strobe)		This signal latches the column addresses (A0 to A8), selects the digit line connecting the sense amplifier, and activates the output circuit which outputs data to the random access port. It also serves as the signal which selects the following operations. • Read/write • Block write • Color register set • Mask register set
A0 to A8 (Address inputs)		These are the address input pins, TAP register input pins, and STOP register input pins. **Address input** This is a 9-bit address bus. It inputs a total of 18 bits of the address signal, starting from the upper 9 bits (row address) and then followed by the lower 9 bits (column bits) (address multiplex method). Using these, one word memory cells (8 bits) are selected from the 262,144 words × 8 bits memory cell array. During use, specify the row address, activate the $\overline{\text{RAS}}$ signal, latch the row address, switch to the column address, and activate the $\overline{\text{CAS}}$ signal. After activating the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals, each address signal is taken into the device. For this reason, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for activating the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals. **TAP Register Input** In the data transfer cycle, this TAP register input pin functions as the address input pin which selects the memory cell for transferring (9 bits are latched at the falling edge of $\overline{\text{RAS}}$) and the TAP register data input pin which specifies the start addresses of the serial read/write operation after data transfer (9 bits are latched at the falling edge of the $\overline{\text{CAS}}$). **STOP Register Input** This pin functions as the STOP register input pin when the STOP register is set (STOP register data (9 bits) are latched at the falling edge of the $\overline{\text{RAS}}$.)

(2/3)

Pin Name	Input/ Output	Function
$\overline{\text{DT}}/\overline{\text{OE}}$ (Data transfer/ output enable)	Input	These are the data transfer control signal and read operation control signal respectively. They have different functions in the data transfer cycle and read cycle. Data transfer control signal (In data transfer cycle) The data transfer cycle is initiated when a low level is input to this pin at the falling edge of $\overline{\text{RAS}}$. Read operations control signal (In read cycle) Read operation is performed when this signal, and the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals are activated. The input/output pin is high impedance when this signal is not activated. When the $\overline{\text{WB}}/\overline{\text{WE}}$ signal is activated while the $\overline{\text{DT}}/\overline{\text{OE}}$ signal is activated, the $\overline{\text{DT}}/\overline{\text{OE}}$ signal is invalid in the memory and read operations cannot be performed.
$\overline{\text{WB}}/\overline{\text{WE}}$ (Write-per-bit/ Write enable)		These are the write operation control signal and mask write cycle (write-per-bit function) mask data input control signal, respectively. When this signal, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals are activated, write operations or mask write can be performed. These mode are determined by the level of $\overline{\text{WB}}/\overline{\text{WE}}$ at the falling edge of $\overline{\text{RAS}}$. • High level.......8-bit write cycle • Low level........Mask write cycle (Write-per-bit)
DSF (Special function enable)		This signal controls the selection of functions. The selection of functions is determined by the level of this signal at the falling edge of the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. The functions will change as follows when this signal is high level. • The data transfer cycle changes to a split data transfer cycle. • The read/write cycle of each $\overline{\text{RAS}}$ clock changes to the flash write cycle. • The write cycle of each $\overline{\text{CAS}}$ clock changes to the block write cycle.
W0 to W7/IO0 to IO7 (Mask data selects/ Data inputs, outputs)	Input/ Output	These are normally 8-bit data bus and are used for inputting and outputting data. (IO0 to IO7). Function as the mask data input pins (W0 to W7) in the mask write cycle (write-per-bit function). Write operations can be performed only for W0 to W7 that are input with a high level at the falling edge of $\overline{\text{RAS}}$ (new mask data). Functions as the column selection data input pin in the block write cycle.

(3/3)

Pin Name	Input/ Output	Function
SC (Serial clock)	Input	This pin inputs the clock which controls the serial access port operation. **Serial Read** The data of the data register which is synchronized with the rising edge of the SC are output from the SIO0 to SIO7 pins and kept until the next SC rising edge. **Serial Write** The data from the SIO0 to SIO7 pins are latched at the rising edge of the SC and written in the data register.
$\overline{\text{SE}}$ (Serial data input/ output enable)		This is a control pin for the serial access port input/output buffer. It controls data output during serial reading and controls data input during serial writing. By inputting the serial clock, the serial pointer will operate even if $\overline{\text{SE}}$ has not been activated (high level input).
SIO0 to SIO7 (Serial data inputs/ outputs)	Input/ Output	These are the serial data input and output pins of the serial access port.
QSF (Special function output)	Output	This is a position discrimination pin of the serial pointer (upper side or lower side). Which side is being serial accessed (upper side or lower side) can be discriminated according to the output of this pin. • High level.......Upper side (Addresses 256 to 511) • Low level........Lower side (Addresses 0 to 255)

2. Random Access Port Operations

The operation mode is determined by the $\overline{\text{CAS}}$, $\overline{\text{DT}}/\overline{\text{OE}}$, $\overline{\text{WB}}/\overline{\text{WE}}$, and DSF level at the falling edge of $\overline{\text{RAS}}$ and DSF level at the falling edge of $\overline{\text{CAS}}$.

Table 2-1. Operation Mode

$\overline{\text{RAS}}$ Falling Edge				$\overline{\text{CAS}}$ Falling Edge	Operation Mode	
$\overline{\text{CAS}}$	$\overline{\text{DT}}/\overline{\text{OE}}$	$\overline{\text{WB}}/\overline{\text{WE}}$	DSF	DSF		
H	H	×	L	×	**Read/Write Cycle**	Read cycle
H	H	H	L	L		Write cycle
H	H	H	L	H		Block write cycle
H	H	L	L	L		Mask write cycle (New mask/Old mask)[Note 1]
H	H	L	L	H		Block mask write cycle (New mask/Old mask)[Note 1]
H	H	H	H	H		Color register set cycle
H	H	H	H	L		Write mask register set cycle
H	H	L	H	×		Flash write cycle (New mask/Old mask)[Note 1]
H	L	H	L	×	**Data Transfer Cycle**	Single read data transfer cycle
H	L	H	H	×		Split read data transfer cycle
H	L	L	L	×		Single write data transfer cycle (New mask/Old mask)[Note 1]
H	L	L	H	×		Split write data transfer cycle (New mask/Old mask)[Note 1]
L	×	×	L	×	**Refresh Cycle**	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle (Option reset)[Note 1, 2]
L	×	H	H	×		$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle (No reset)
L	×	L	H	×		$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle (STOP register set)[Note 2]
H	H	×	L	×		$\overline{\text{RAS}}$ only refresh cycle

Notes 1. Observe the following conditions when using the new mask data or old mask data in these cycles.

(1) **Old mask data**

Can be used after setting the mask data using the write mask register set cycle.

(2) **New mask data**

Can be used after selecting the new mask register using the write mask register set cycle (new mask selection) (Unusable in version A) and after the optional reset cycle.

2. The STOP register is set to "FFH (11111111)" by the optional reset cycle.

Remark H : High level, L : Low level, × : High level or low level

2.1 Random Read Cycle

This product has a common 8-bit input/output pin. To output data, specify the address using the $\overline{\mathrm{RAS}}$ and $\overline{\mathrm{CAS}}$ clocks and then set $\overline{\mathrm{DT}}/\overline{\mathrm{OE}}$ to low level.

The data output will be kept until one of the following conditions is set.

(1) Set $\overline{\mathrm{RAS}}$ and $\overline{\mathrm{CAS}}$ to high level
(2) Set $\overline{\mathrm{DT}}/\overline{\mathrm{OE}}$ to high level
(3) Set $\overline{\mathrm{WB}}/\overline{\mathrm{WE}}$ to low level

The read cycle and data transfer cycle are differentiated according to the level of $\overline{\mathrm{DT}}/\overline{\mathrm{OE}}$ at the falling edge of the $\overline{\mathrm{RAS}}$ clock. If $\overline{\mathrm{DT}}/\overline{\mathrm{OE}}$ is set to low level at the falling edge of the $\overline{\mathrm{RAS}}$ clock, data transfer cycle operations will be initiated. Therefore, to set the read cycle, input a high level above t_{DHH} (MIN.) to $\overline{\mathrm{DT}}/\overline{\mathrm{OE}}$ from the falling edge of the $\overline{\mathrm{RAS}}$ clock, and then input a low level.

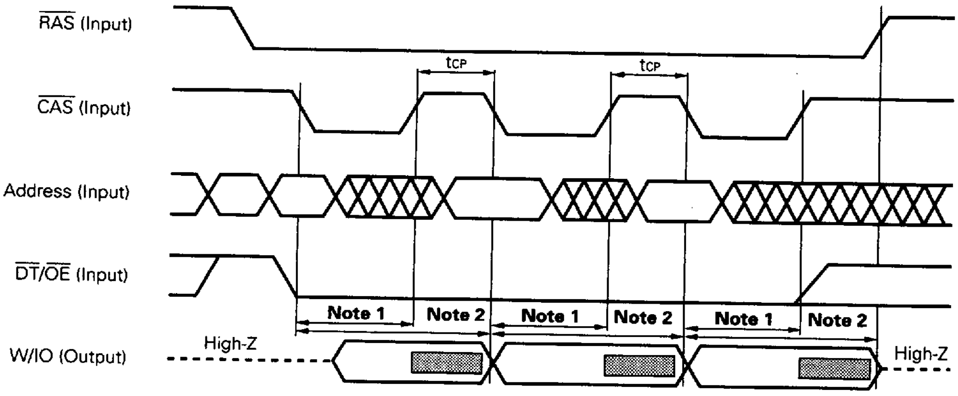
Caution Set the DSF to low level at the falling edge of $\overline{\mathrm{RAS}}$. If set to high level, the memory cell data cannot be output.

2.1.1 Extended Read Data Output (μPD482235)

The μPD482235 adopt the hyper page mode cycle which is a faster read/write cycle than the fast page mode of the μPD482234 (Hyper page mode cycle time: 30 ns (MIN.)).

With this cycle, the read data output can be kept until the next $\overline{\mathrm{CAS}}$ cycle, and because the output is extended, the minimum cycle can easily be used. For example, by fixing $\overline{\mathrm{DT}}/\overline{\mathrm{OE}}$ at low level after dropping $\overline{\mathrm{RAS}}$ and executing the hyper page read cycle, each time the column address is latched at the falling edge of $\overline{\mathrm{CAS}}$, the data output will be updated and kept until the next falling edge of $\overline{\mathrm{CAS}}$. As a result, the output will be extended only during $\overline{\mathrm{CAS}}$ precharge time (t_{CP}) as compared to the normal fast page mode.

Figure 2-1. Extended Data Output of Hyper Page Mode



Notes 1. Time during which the output data is kept in the fast page read cycle.
2. Time during which the output data is kept in the hyper page read cycle (▨ part: Extended data output).

2.2 Random Write Cycle (Early Write, Late Write, Read Modify Write)

There are three types of random write cycles-the early write, late write, and read modify write. To use these cycles, activate the $\overline{RAS}$ and $\overline{CAS}$ clocks and set $\overline{WB}/\overline{WE}$ to low level.

The $\overline{WB}/\overline{WE}$ also controls the mask data for the write-per-bit function (mask write cycle). Therefore, when performing the normal write cycle which does not use the write-per-bit function, set this pin to high level at the falling edge of the $\overline{RAS}$ clock.

2.2.1 Early Write Cycle

The early write cycle controls data writing according to the $\overline{CAS}$ clock.

To execute this cycle, set $\overline{WB}/\overline{WE}$ to low level earlier than the $\overline{CAS}$ clock. The write data is taken into the device at the falling edge of the $\overline{CAS}$ clock.

2.2.2 Late Write Cycle

The late write cycle controls data writing according to the $\overline{WE}$ clock.

To execute this cycle, set $\overline{WB}/\overline{WE}$ to low level later than the $\overline{CAS}$ clock. The write data is taken into the device at the falling edge of $\overline{WB}/\overline{WE}$. To set the output to high impedance at this time, keep $\overline{DT}/\overline{OE}$ at high level until $\overline{WB}/\overline{WE}$ is input.

2.2.3 Read Modify Write Cycle

The read modify write cycle performs data reading and writing in one $\overline{RAS}$ and $\overline{CAS}$ cycle.

To execute this cycle, delay $\overline{WB}/\overline{WE}$ from the late write cycle by t_{RWD} (MIN.), t_{CWD} (MIN.), and t_{AWD} (MIN.). Follow the t_{OEZ} and t_{OED} specifications so that the output data and input data do not clash in the data bus. The data after modification can be input after more than t_{OED} (MIN.) from the rising edge of $\overline{DT}/\overline{OE}$.

2.3 Fast Page Mode Cycle (μPD482234)

The μPD482234 adopts the fast page mode. This mode accesses memory cells in the same row array in about 1/3 of the time taken by the normal random read/write cycle. This fast page mode cycle is executed by repeating the $\overline{\text{CAS}}$ clock cycle more than two times while the $\overline{\text{RAS}}$ clock is being activated. In this mode read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

2.4 Hyper Page Mode Cycle (μPD482235)

The μPD482235 adopts a hyper page mode cycle which is a faster read/write cycle than the fast page mode of the μPD482434 (Hyper page mode cycle time: 30 ns (MIN.)).

In this cycle, because the read data output is kept until the following $\overline{\text{CAS}}$ cycle and as a result, the output is extended, the minimum cycle can easily be used. The output is extended compared to the normal fast page mode of μPD482234. Refer to **2.1.1 Extended Read Data Output.**

2.4.1 Setting the Output to the High Impedance State

The hyper page mode can use one of three methods of setting the output pin to the high impedance state depending on the version; these methods are $\overline{\text{WE}}$ control, $\overline{\text{OE}}$ control (latched control), and $\overline{\text{OE}}$ control (non-latched control).

Table 2-2 lists the correspondence between the output control types and versions A, F, and E.

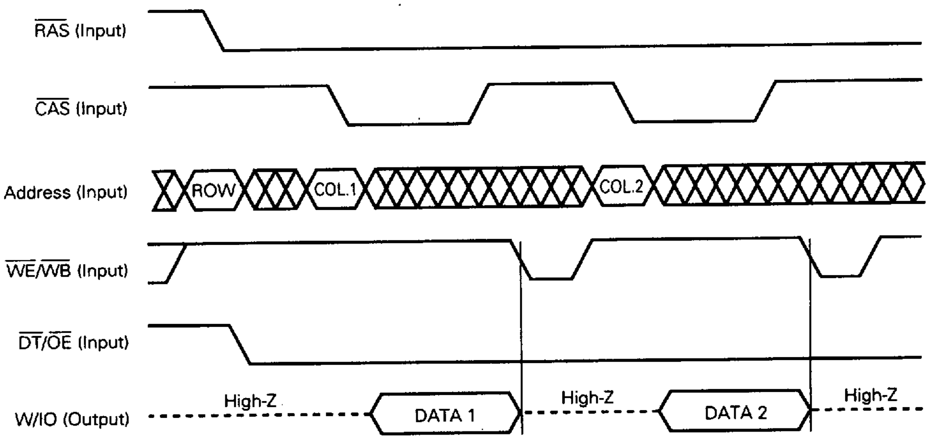
Table 2-2. Correspondence between Each Output Control Method and Versions A, F, and E

Output control	Version A	Version F	Version E
$\overline{\text{WE}}$ control	usable	usable	usable
$\overline{\text{OE}}$ control (latched control), conforming to JEDEC	usable	unusable	unusable
$\overline{\text{OE}}$ control (non-latched control)	unusable	usable	usable

(1) $\overline{\text{WE}}$ control (usable in all versions)

After a high level is input to $\overline{\text{CAS}}$, when a pulse conforming to the t_{WEZ} specification is supplied to the $\overline{\text{WE}}$ pin ($\overline{\text{WE}}$ = enable) during the same $\overline{\text{CAS}}$ cycle, the W/IO pin is held in the high impedance state until the next $\overline{\text{CAS}}$ cycle.

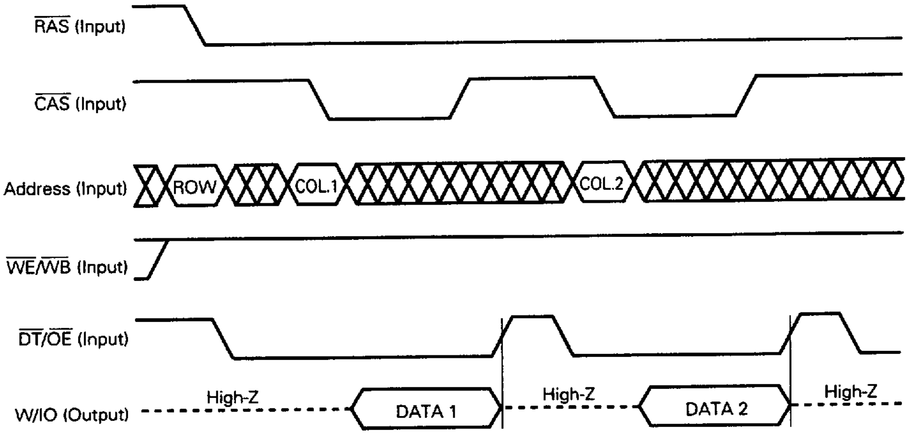
Figure 2-2. $\overline{\text{WE}}$ Control Output Control



(2) $\overline{\text{OE}}$ control (latched control) (usable in version A)

After a high level is input to $\overline{\text{CAS}}$, when a high level is supplied to the $\overline{\text{OE}}$ pin ($\overline{\text{OE}}$ = disable) during the same $\overline{\text{CAS}}$ cycle, the W/IO pin is held in the high impedance state until the next $\overline{\text{CAS}}$ cycle. This specification enables efficient use of $\overline{\text{OE}}$ interleaving during parallel connection.

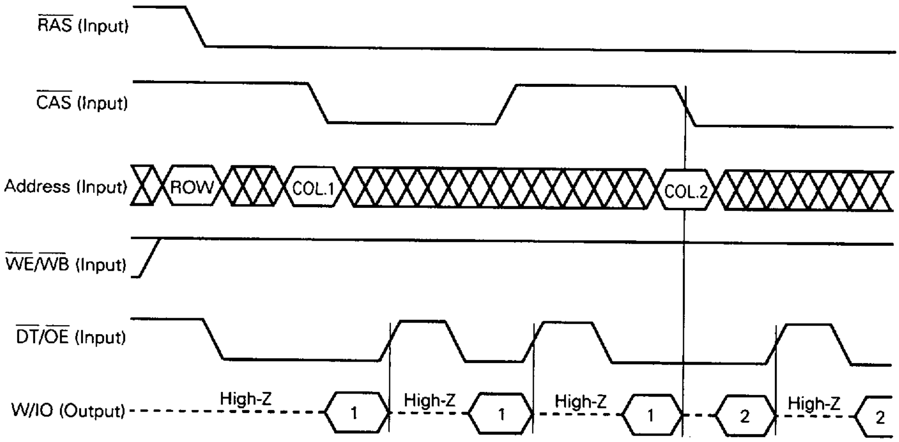
Figure 2-3. $\overline{\text{OE}}$ Control Output Control (Latched Control)



(3) $\overline{\text{OE}}$ control (non-latched control) (usable in versions F and E)

When a high level is input to the $\overline{\text{OE}}$ pin ($\overline{\text{OE}}$ = disable) during the same $\overline{\text{CAS}}$ cycle, the W/IO pin enters the high impedance state. If a low level is input to the $\overline{\text{OE}}$ pin again before the next $\overline{\text{CAS}}$ cycle ($\overline{\text{OE}}$ = enable), the data at the same address is output to the W/IO pin again.

Figure 2-4. $\overline{\text{OE}}$ Control Output Control (Non-Latched Control)



2.5 Flash Write Cycle

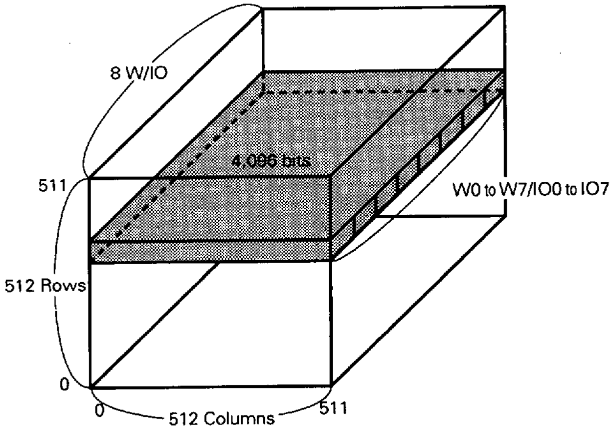
This cycle writes the color register data in a 4,096-bit memory cell in one cycle. The memory cell range for one flash write cycle is 512 columns on the same row address (512-column × 8 · IO = 4,096 bits).

2.5.1 Execution of Flash Write Cycle

To execute the flash write cycle, set $\overline{\text{WB}}/\overline{\text{WE}}$ to low level at the falling edge of $\overline{\text{RAS}}$.

By using the write-per-bit function (new mask data/old mask data), only the required W/IO can be selected and written.

Figure 2-5. Memory Cell Range That Can be Written with Flash Write Cycle



Remark ▨ is the memory cell range that can be written in one flash write cycle.

2.6 Block Write Cycle

This cycle writes the color register data in 32-bit memory cell in one cycle. The memory cell range in which data can be written in one block write cycle is four continuous columns on one row address (4-column × 8 · IO = 32 bits).

Any column of the four columns can be selected and writing prohibited. Determine whether to write or prohibit writing according to the data selected for column.

2.6.1 Free Column Selection

Determine which column to select according to the W/IO pin to which the data selected for the column is to be input.

The four columns (1st to 4th) correspond to W0 to W3/IO0 to IO3 to which the data selected for column will be input (The following table shows the 1st to 4th columns specified by A0 and A1 and the corresponding W/IO pins to which the data selected will be input.).

2.6.2 Column Select Data

Input column select data for every four columns at the 32 bits (4-column × 8 · IO). The data will be written if the column select data is "1". Writing will be prohibited if the column select data is "0"

2.6.3 Execution of Block Write Cycle

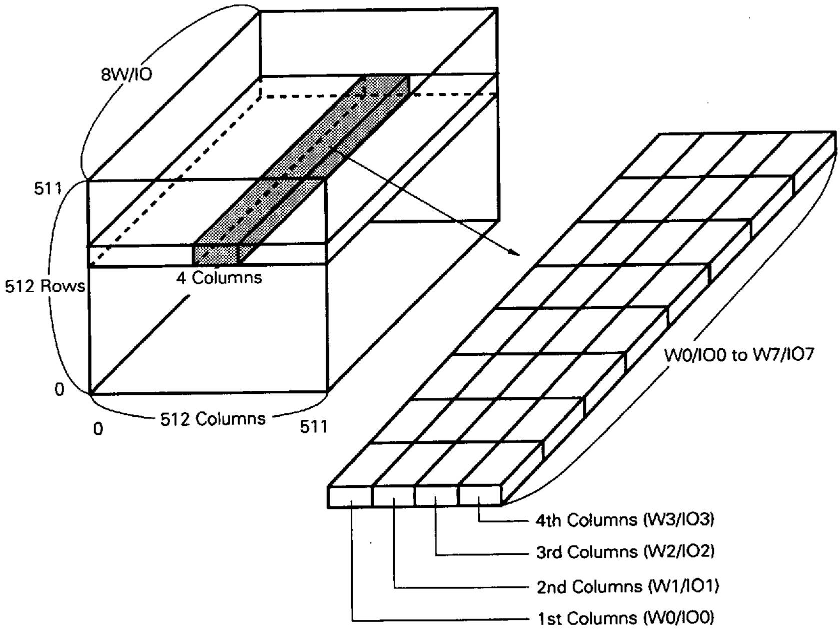
At the falling edge of the slowest signal ($\overline{CAS}$, $\overline{WB}/\overline{WE}$), input the "1" column select data or "0" column select data to W0 to W3/IO0 to IO3 corresponding to columns 1st to 4th.

By using the write-per-bit (new mask data/old mask data) function, only the required W/IO can be selected and written.

Table 2-3. I/O Pins Input with Column Select Data Corresponding to Columns 1st to 4th

Selected 4 Columns	Column Address and Corresponding W/IO Pin			Column Select Data	Writing
	A1	A0	IO		
1st column	0	0	IO0	1	Yes
				0	No
2nd column	0	1	IO1	1	Yes
				0	No
3rd column	1	0	IO2	1	Yes
				0	No
4th column	1	1	IO3	1	Yes
				0	No

Figure 2-6. Memory Cell Range That Can be Written in Block Write Cycle



Remarks 1. ▨ is the memory cell range that can be written in one block write cycle.

2. ( ) is the W/IO pin input with the column select data.

2.7 Register Set Cycle (Color Register, Write Mask Register)

This cycle writes data in the color register and write mask register. To execute the register set cycle, set $\overline{\text{CAS}}$, $\overline{\text{DT}}/\overline{\text{OE}}$, $\overline{\text{WB}}/\overline{\text{WE}}$ and DSF to high level at the falling edge of $\overline{\text{RAS}}$. Determine which register to select according to the DSF level at the falling edge of $\overline{\text{CAS}}$.

The register set cycle also serves as the $\overline{\text{RAS}}$ only refresh cycle.

Table 2-4. Register Selection

DSF level at $\overline{\text{CAS}}$ falling edge	Selected register
High level	Color register
Low level	Write mask register

Caution **After selecting the write mask register and writing the mask data, the write-per-bit function in the mask write cycle will be set for the old mask register. Refer to 2.8.1 Write-Per-Bit Function.**

2.8 Mask Write Cycle

Cycles that use the write-per-bit function during the random write cycle, flash write cycle, block write cycle, write data transfer cycle, are called mask write cycles. In the fast page/hyper page mode write cycle, the mask data cannot be changed during the $\overline{\text{CAS}}$ cycle.

2.8.1 Write-Per-Bit Function

The write-per-bit function writes data using the mask data only in the required IO-pin. It writes when the mask data is "1" and prohibits writing when the data is "0".

Table 2-5. Mask Data Selection

W Pin	Mask Data	Writing
W0 to W7	1	Yes
	0	No

2.8.2 Selecting Mask Data

There are two ways of selecting mask data. One is the new mask data method and the other is the old mask data method.

With the new mask data method, new mask data is set in the cycle writing. With the old mask data, mask data set in the write mask register is used.

(1) New Mask Data Method

The new mask data method consists of the write mask register set cycle (new mask selection) method and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle (optional reset cycle) method.

However, only the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle (option reset cycle) can be used in version A. **Table 2-6** lists how to select the new mask data method for each version.

Table 2-6. New Mask Data Selection Method for Each Version

New mask data selection method	Version A	Version F	Version E
Method to use the write mask register set cycle (new mask selection)	unusable	usable	usable
Method to use the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle (option reset cycle.)	usable	usable	usable

(a) Method Using Write Mask Register Set Cycle (New Mask Selection) (Versions F and E)

This method is usable in both version F and version E.

To switch to the mode using new mask data, keep the $\overline{\text{DT}}/\overline{\text{OE}}$, $\overline{\text{WB}}/\overline{\text{WE}}$ DSF to high level and set the $\overline{\text{CAS}}$ and DSF to high level at the falling edge of $\overline{\text{RAS}}$, the DSF to low level at the falling edge of $\overline{\text{CAS}}$, and start up the next $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ after the t_{CAS} and t_{RAS}.

As a result, the write-per-bit function can be used using the new mask data from the next mask write cycle.

(b) Method Using $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle (Optional Reset Cycle) (All versions)

This method is usable in all versions.

To switch to the mode using new mask data, set the DSF to low level at the falling edge of $\overline{\text{CAS}}$ in the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.

As a result, the write-per-bit function can be used using the old mask data from the next mask write cycle.

(2) Old Mask Data Method

To switch to the mode using old mask data, set the DSF to low level at the falling edge of $\overline{\text{CAS}}$ in the write mask register set cycle, and write the mask data in the write mask register.

As a result, the write-per-bit function can be used using the old mask data from the next mask write cycle.

2.8.3 Execution of Mask Write Cycle

To execute the write-per-bit function, select the new mask data method or old mask data method, and set $\overline{\text{WB}}/\overline{\text{WE}}$ to low level at the falling edge of $\overline{\text{RAS}}$ of each write cycle. At this time, input the mask data to the W pin in the write cycle using the new mask data. In the write cycle using the old mask data, as the mask data set to the write mask register will be used, there is no need to input the mask data to the W pin.

This function is valid only at the falling edge of $\overline{\text{RAS}}$. In the fast page/hyper page mode write cycle, the mask data determined in the first $\overline{\text{RAS}}$ cycle for moving onto the next fast page/hyper page mode will be valid while the fast page/hyper page mode write cycle continues.

2.9 Refresh Cycle

The refresh cycle of this product consists of the CAS before RAS refresh cycle and refresh cycle using external address inputs (RAS only refresh and read/write refresh). The refresh period is the same as the DRAM (Standard), 512 cycles/8 ms.

2.9.1 Refresh Cycle Using External Address Input (RAS Only Refresh and Read/Write Refresh)

By specifying the row address using the 9 bits between A0 to A8 at the falling edge of RAS, setting CAS and DT/OE to high level, and keeping CAS at high level while RAS is low level, the memory cells on the specified row address (512 × 8 bits) can be refreshed. At this time, refresh is executed, W0 to W7/IO0 to IO7 pins are kept at high impedance, and information such as memory contents, register data, function settings, etc. are all also kept.

At the falling edge of RAS, all cycles whose CAS are high level input the external address. Therefore, in addition to the read/write cycle operations, etc. refresh operations similar to the RAS only refresh operations will be performed. For this reason, in systems in which addresses in the memory are always increased or decreased, it may not be necessary to perform refresh again.

When several devices exist on one bus, data will clash in the bus during the above read/write operations unless each device is equipped with a buffer. Consequently, as it is necessary to set the I/O line to high impedance beforehand during refresh, normally the RAS only refresh operation is used.

2.9.2 CAS Before RAS Refresh Cycle (Including Hidden Refresh)

When CAS is set to low level at the falling edge of RAS, the refresh address is supplied from the internal refresh address counter. The internal refresh address counter is increased automatically each time this refresh cycle is executed.

During this refresh cycle, functions of random access port and serial access port are selected as follows according to the DSF and WB/WE levels at the falling edge of RAS.

(1) When DSF is low level: Optional reset

All STOP register data become "1" and the mask write cycle switches to the new mask data method.

(2) When DSF is high level and WB/WE is low level: STOP register set

The STOP register data is input from the A0 to A7 pins at the falling edge of RAS.

(3) When DSF, WB/WE is high level: No reset

Only refresh operations are performed and the function selection state is kept.

In all cases, the W/IO pin is kept at high impedance. When CAS and DT/OE are kept low level while the mode is changed to the CAS before RAS refresh cycle following the read cycle, and RAS is activated, the hidden refresh cycle will be initiated. In this cycle, the W/IO pin does not become high impedance and the data read in the former read cycle will be kept as it is.

Because internal memory operations are equivalent to CAS before RAS refresh, no external addresses are required.

Like CAS before RAS refresh, in the hidden cycle, functions will be selected according to the level of DSF, WB/WE at the falling edge of RAS. Operations are guaranteed when DSF is low level and when DSF, WB/WE are high level.

3. Serial Access Port Operations

There are two types of data transfer cycles-data transfer from the random access port to the serial access port (read data transfer) and data transfer from the serial access port to the random access port (write data transfer). There are also two types of data transfer methods-single data transfer and split data transfer.

To set the data transfer cycle, input high level to $\overline{\text{CAS}}$ and input low level to $\overline{\text{DT}}/\overline{\text{OE}}$ at the falling edge of $\overline{\text{RAS}}$.

The data transfer type differs according to the input levels of $\overline{\text{WB}}/\overline{\text{WE}}$, and DSF at the falling edge of $\overline{\text{RAS}}$.

Table 3-1. Serial Access Port Operation Mode

At $\overline{\text{RAS}}$ Falling Edge				Data Transfer Type	Transfer Direction	
$\overline{\text{CAS}}$	$\overline{\text{DT}}/\overline{\text{OE}}$	$\overline{\text{WB}}/\overline{\text{WE}}$	$\overline{\text{DSF}}$		Transfer Source	Transfer Destination
H	L	H	L	Single read data transfer	Random access port	Serial access port
H	L	H	H	Split read data transfer		
H	L	L	L	Single mask write data transfer[Note]	Serial access port	Random access port
H	L	L	H	Split mask write data transfer[Note]		

Note Write-per-bit function can be specified.

Remark H: High level, L: Low level

3.1 Single Data Transfer Method

With this method, 512 words × 8 bits (whole memory range of serial access port) data is transferred at one time. This method can be used in both write data transfer and read data transfer.

3.1.1 Single Read Data Transfer Cycle

This cycle transfers the 4K-bit (512 words × 8 bits) data of the random access port to the serial access port in one cycle.

(a) Setting of Single Read Data Transfer Cycle

To set the data transfer cycle, input a high level to $\overline{\text{CAS}}$ and $\overline{\text{WB}}/\overline{\text{WE}}$ and low level to $\overline{\text{DT}}/\overline{\text{OE}}$ and DSF at the falling edge of $\overline{\text{RAS}}$.

Using the row address input to A0 to A8 at the falling edge of $\overline{\text{RAS}}$, the memory cells (512 words × 8 bits) of the transfer source of the random access port can be selected. The address data input to A0 to A8 at the falling edge of $\overline{\text{CAS}}$ will be latched as the TAP register data of serial access port. Refer to **3.4 TAP Register.**

(b) Execution of Single Read Data Transfer Cycle

To execute the data transfer cycle, set the single read data transfer cycle and then input a high level to $\overline{\text{DT}}/\overline{\text{OE}}$ and $\overline{\text{RAS}}$.

When SC is active (edge control), data transfer will be executed at the rising edge of $\overline{\text{DT}}/\overline{\text{OE}}$. When SC is inactive (self control), it will be executed at the rising edge of $\overline{\text{RAS}}$. At the same time, the serial address pointer jumps to the start column (TAP) of the next serial read cycle, and the TAP register will be set the empty state.

After the transfer is completed, the new serial access port data is output after t_{SCA} following the rise of the SC clock that occurs after t_{SDH} if the SC is active, and after t_{SDHR} if SC is inactive.

Caution When the single read data transfer cycle is executed while the serial access port is performing serial write operations, the serial access port will start serial read operations at the rising edge of $\overline{\text{RAS}}$. Refer to 4. Electrical Characteristics Read Data Transfer Cycle (Serial Write → Serial Read Switching) Timings.

3.1.2 Single Mask Write Data Transfer Cycle

This cycle transfers 4K-bit (512 word × 8 bits) data of the serial access port to the random access port in one cycle. Because $\overline{\text{WB}}/\overline{\text{WE}}$ is low level at the falling edge of $\overline{\text{RAS}}$, the write-per-bit function always functions in this transfer cycle. Refer to **2.8 Mask Write Cycle**.

(a) Setting of Single Mask Write Data Transfer Cycle

To set this cycle, latch the data to be transferred to the serial access port, and then input a high level to $\overline{\text{CAS}}$ and low level to $\overline{\text{DT}}/\overline{\text{OE}}$, $\overline{\text{WB}}/\overline{\text{WE}}$, and DSF at the falling edge of $\overline{\text{RAS}}$. Because the write-per-bit function functions in this transfer operation, for the new mask data method, the mask data must be supplied to W0 to W7 at the falling edge of $\overline{\text{RAS}}$, and for the old mask data method, there is no need to control the mask data.

The memory cells (512 words × 8 bits) of the transfer destination of the random access port are selected using the row address input to A0 to A8 at the falling edge of $\overline{\text{RAS}}$. The address data input to A0 to A8 at the falling edge of $\overline{\text{CAS}}$ is input as the TAP register data of serial access port. Refer to **3.4 TAP Register**.

(b) Execution of Single Mask Write Data Transfer Cycle

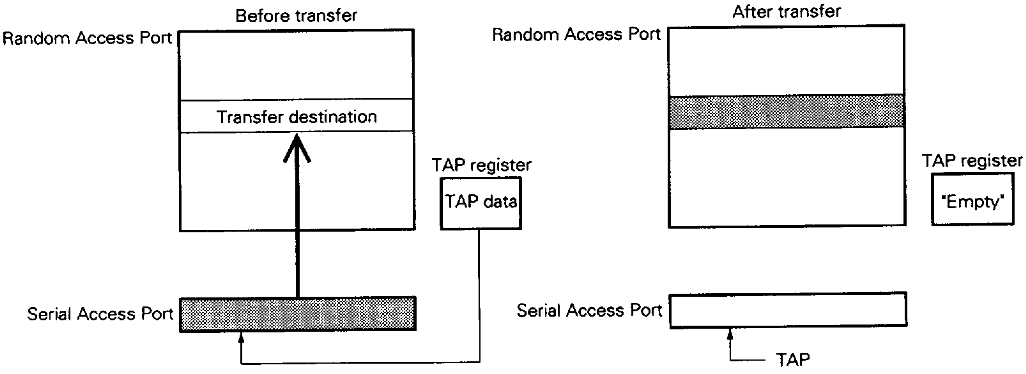
To execute this cycle, set the single write data transfer cycle and then input high level to $\overline{\text{RAS}}$. Data will be transferred at the rising edge of $\overline{\text{RAS}}$. At the same time, the serial address pointer jumps to the start column (TAP) of the next serial write cycle, and the TAP register will be set the empty state.

After the transfer is completed, the new serial access port data is latched at the rising edge of the SC clock that occurs after t_{SDHR}.

Caution

1. **When the single mask write data transfer cycle is executed while the serial access port is performing serial read operations, the serial access port will start serial write operations at the rising edge of $\overline{\text{RAS}}$. Refer to 4. Electrical Characteristics Write Data Transfer Cycle (Serial Read → Serial Write Switching) Timings.**
2. **Always make $\overline{\text{CAS}}$ low level in the write data transfer cycle and latch TAP. If write data transfer is performed without setting TAP, serial access port operations cannot be ensured until either one of the following points. If the SC clock is input during this time, the serial register value also cannot be guaranteed.**
   - **Until the falling edge of $\overline{\text{CAS}}$ during the write data transfer cycle**
   - **Until the read data transfer cycle is executed again**

Figure 3-1. Single Write Data Transfer and TAP Operation



3.2 Split Data Transfer Method

With this method, the 512 words × 8 bits (whole memory range of serial access port) data is divided into the lower column (0 to 255) and upper column (256 to 511), each consisting of 256 words × 8 bits.

Because the columns are divided into upper and lower columns with this method, data transfer can be performed on lower column (or upper column) while performing read/write operations in the upper column (or lower column). For this reason, transfer timing design is easy. This transfer method can be used in both write data transfer and read data transfer.

This transfer method uses either of two modes, "MSB Care" and "MSB Don't Care," depending on the method used to select the column for data transfer (See the table below.). The mode to be used varies from one version to another. Refer to **7. Example of Stamping** for how to identify each version.

Table 3-2. Differences between the MSB Don't Care and MSB Care Modes

Mode	Version	Function
MSB Don't Care	Versions A and F	A8 input as TAP is ignored, and an inactive column is selected automatically for data transfer.
MSB Care	Version E	The column (upper or lower) is specified for data transfer according to A8 input as TAP.

3.2.1 Split Read Data Transfer Cycle (Versions A and F: For "MSB Don't Care")

This cycle divides the 4K-bit (512 words × 8 bits) data of the random access port into the lower and upper columns and transfers them to the serial access port.

In this cycle, the serial read/write can be performed in the columns to which data is not transfer.

(a) Setting of Split Read Data Transfer Cycle

To set this cycle, input a high level to $\overline{\text{CAS}}$, $\overline{\text{WB}}/\overline{\text{WE}}$ and DSF, and low level to $\overline{\text{DT}}/\overline{\text{OE}}$ at the falling edge of $\overline{\text{RAS}}$.

The memory cells (512 words × 8 bits) of the transfer source of the random access port are selected using the row address input to A0 to A8 at the falling edge of $\overline{\text{RAS}}$. And the address data input to A0 to A7 at the falling edge of $\overline{\text{CAS}}$ is latched as the TAP register data of serial access port. Refer to **3.4 TAP Register.** There is no need to control address data input to A8 (See the table below.).

Table 3-3. Relationships among Data Register Transfer Destination, A8 Inputs, and QSF Outputs (Split Read Data Transfer Cycle in the MSB Don't Care Mode)

A8 data input to the TAP register	QSF output	Data register transfer destination
A8 = ×	QSF = 1	Lower column (addresses 0 to 255)
	QSF = 0	Upper column (addresses 256 to 511)

Remark 1 = high level; 0 = low level; × = high or low level

(b) Execution of Split Read Data Transfer Cycle

To execute this cycle, set the split read data transfer cycle and then input the high level to $\overline{\text{RAS}}$. Data will be transferred at the rising edge of $\overline{\text{RAS}}$. Data is transferred from the random access port to the serial access port automatically at the column side (Column not pointed to by the serial address pointer) where serial access port is inactive. To confirm the transferred column side, check the output state of the QSF pin. Refer to **3.3.3 QSF Pin Output.**

When the serial address pointer comes to the jump source address specified by the STOP register, the serial address pointer jumps to the start column (TAP) of the serial read/write cycle at the inactive column side, and the TAP register will be set the empty state.

3.2.2 Split Read Data Transfer Cycle (Versions E: For "MSB Care")

This cycle divides the 4K-bit (512 words × 8 bits) data of the random access port into the lower and upper columns and transfers them to the serial access port.

In this cycle, the serial read/write can be performed in the columns to which data is not transfer.

(a) Setting of Split Read Data Transfer Cycle

To set this cycle, input a high level to $\overline{\text{CAS}}$, $\overline{\text{WB}}/\overline{\text{WE}}$ and DSF, and low level to $\overline{\text{DT}}/\overline{\text{OE}}$ at the falling edge of $\overline{\text{RAS}}$.

The memory cells (512 words × 8 bits) of the transfer source of the random access port are selected using the row address input to A0 to A8 at the falling edge of $\overline{\text{RAS}}$. And the address data input to A0 to A8 at the falling edge of $\overline{\text{CAS}}$ is latched as the TAP register data of serial access port. Refer to **3.4 TAP Register.**

If the address data input to A8 is 0, data in lower columns is trasferred from the random access port to the serial access port. If it is 1, data in upper columns is transferred from the random access port to the serial access port. To perform the data transfer in columns for which no serial read is not being made (columns for which the serial register is inactive), it is necessary to supply an inverted QSF output to A8 (See the table below.).

Table 3-4. Relationships among Data Register Transfer Destination, A8 Inputs, and QSF Outputs (Split Read Data Transfer Cycle in the MSB Care Mode)

A8 data input to the TAP register	QSF output	Data register transfer destination
A8 = 0	QSF = 1	Lower column (addresses 0 to 255)
A8 = 1	QSF = 0	Upper column (addresses 256 to 511)

Remark 1 = high level; 0 = low level

(b) Execution of Split Read Data Transfer Cycle

To execute this cycle, set the split read data transfer cycle and then input the high level to $\overline{\text{RAS}}$. Data will be transferred at the rising edge of $\overline{\text{RAS}}$. Data in the upper or lower column is transferred from the random access port to the serial access port, depending on the data input to A8. To confirm the transferred column side, check the output state of the QSF pin. Refer to **3.3.3 QSF Pin Output.**

When the serial address pointer comes to the jump source address specified by the STOP register, the serial address pointer jumps to the start column (TAP) of the serial read/write cycle at the inactive column side, and the TAP register will be set the empty state.

Caution When data is tranferred in a split read data transfer cycle, if the related serial register is already involved in serial read/write operation, the serial address pointer changes during data transfer, and the TAP register becomes empty. The timing for this operation is the same as for the read data transfer cycle (SC inactive).

3.2.3 Split Mask Write Data Transfer Cycle (Versions A and F: For "MSB Don't Care")

This cycle divides the 4K-bit (512 words × 8 bits) data of the serial access port into the lower and upper columns and transfers them to the random access port.

In this cycle, serial read/write can be performed for columns to which data is not transferred.

Because $\overline{\text{WB}}/\overline{\text{WE}}$ is low level at the falling edge of $\overline{\text{RAS}}$, the write-per-bit function always functions in this transfer cycle. Refer to **2.8 Mask Write Cycle**.

(a) Setting of Split Mask Write Data Transfer Cycle

To set this data transfer cycle, input a high level to $\overline{\text{CAS}}$ and DSF and low level to $\overline{\text{DT}}/\overline{\text{OE}}$, $\overline{\text{WB}}/\overline{\text{WE}}$ at the falling edge of $\overline{\text{RAS}}$. Because the write-per-bit function functions in this transfer operation, for the new mask data method, the mask data must be supplied to W0 to W7 at the falling edge of $\overline{\text{RAS}}$, and for the old mask data method, there is no need to control the mask data.

The memory cells (512 words × 8 bits) of the transfer destination of the random access port are selected using the row address input to A0 to A8 at the falling edge of $\overline{\text{RAS}}$. The address data input to A0 to A7 at the falling edge of $\overline{\text{CAS}}$ is input as the TAP register data. Refer to **3.4 TAP Register**. There is no need to control address data input to A8 (See the table below.).

Table 3-5. Relationships among Data Register Transfer Source, A8 Inputs, and QSF Outputs (Split Write Data Transfer Cycle in the MSB Don't Care Mode)

A8 data input to the TAP register	QSF output	Data register transfer destination
A8 = ×	QSF = 1	Lower column (addresses 0 to 255)
	QSF = 0	Upper column (addresses 256 to 511)

Remark 1 = high level; 0 = low level; × = high or low level

(b) Execution of Split Mask Write Data Transfer Cycle

To execute this cycle, set the split write data transfer cycle and then input high level to $\overline{\text{RAS}}$. Data will be transferred at the rising edge of $\overline{\text{RAS}}$. Data is transferred from the serial access port to the random access port automatically at the column side (Column not pointed to by the serial address pointer) where the serial access port is inactive. To confirm the transferred column side, check the output state of the QSF pin. Refer to **3.3.3 QSF Pin Output**.

When the serial address pointer comes to the jump source address specified by the STOP register, the serial address pointer jumps to the start column (TAP) of the serial read/write cycle at the inactive column side, and the TAP register will be set the empty state.

3.2.4 Split Mask Write Data Transfer Cycle (Versions E: For "MSB Care")

This cycle divides the 4K-bit (512 words × 8 bits) data of the serial access port into the lower and upper columns and transfers them to the random access port.

In this cycle, serial read/write can be performed for columns to which data is not transferred.

Because $\overline{\text{WB}}/\overline{\text{WE}}$ is low level at the falling edge of $\overline{\text{RAS}}$, the write-per-bit function always functions in this transfer cycle. Refer to **2.8 Mask Write Cycle.**

(a) Setting of Split Mask Write Data Transfer Cycle

To set this data transfer cycle, input a high level to $\overline{\text{CAS}}$ and DSF and low level to $\overline{\text{DT}}/\overline{\text{OE}}$, $\overline{\text{WB}}/\overline{\text{WE}}$ at the falling edge of $\overline{\text{RAS}}$. Because the write-per-bit function functions in this transfer operation, for the new mask data method, the mask data must be supplied to W0 to W7 at the falling edge of $\overline{\text{RAS}}$, and for the old mask data method, there is no need to control the mask data.

The memory cells (512 words × 8 bits) of the transfer destination of the random access port are selected using the row address input to A0 to A8 at the falling edge of $\overline{\text{RAS}}$. The address data input to A0 to A8 at the falling edge of $\overline{\text{CAS}}$ is input as the TAP register data. Refer to **3.4 TAP Register.**

If the address data input to A8 is 0, data in lower columns is transferred from the serial access port to the random access port. If it is 1, data in upper columns is transferred from the serial access port to the random access port. To perform the data transfer in columns for which no serial write is not being made (columns for which the serial register is inactive), it is necessary to supply an inverted QSF output to A8 (See the table below.).

Table 3-6. Relationships among Data Register Transfer Source, A8 Inputs, and QSF Outputs (Split Write Data Transfer Cycle in the MSB Care Mode)

A8 data input to the TAP register	QSF output	Data register transfer destination
A8 = 0	QSF = 1	Lower column (addresses 0 to 255)
A8 = 1	QSF = 0	Upper column (addresses 256 to 511)

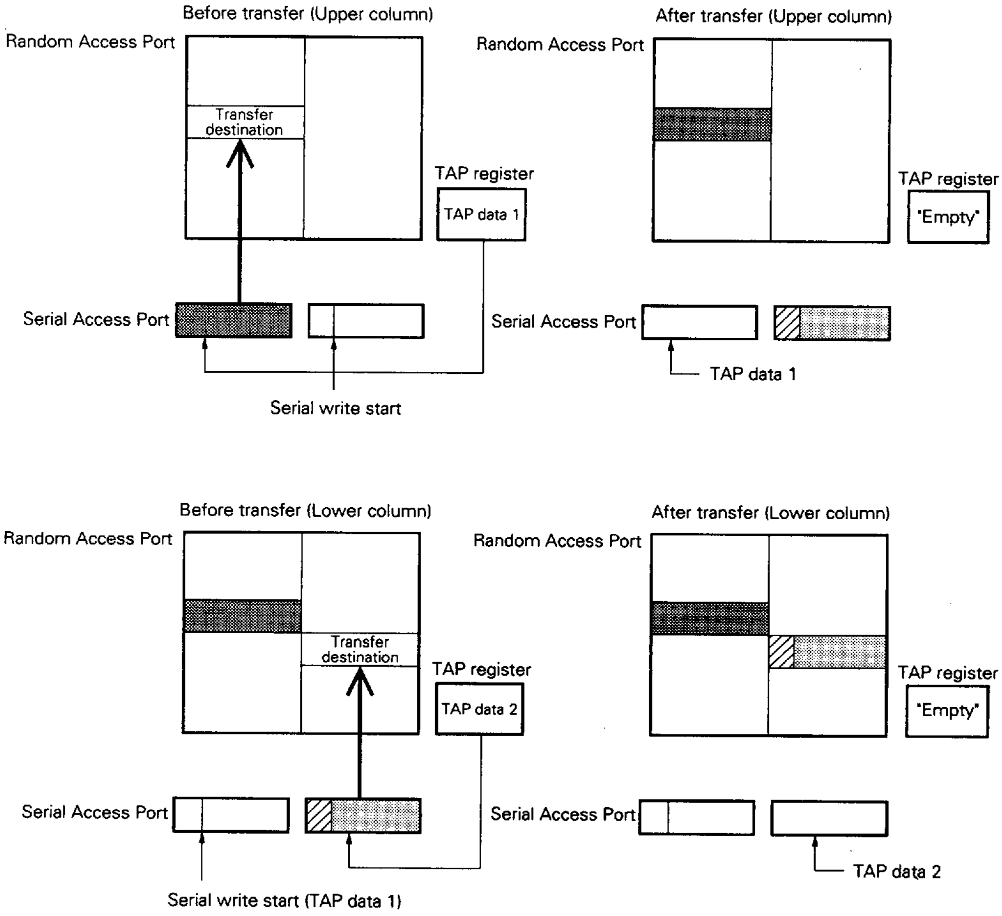
Remark 1 = high level; 0 = low level

(b) Execution of Split Mask Write Data Transfer Cycle

To execute this cycle, set the split write data transfer cycle and then input high level to $\overline{\text{RAS}}$. Data will be transferred at the rising edge of $\overline{\text{RAS}}$. Data in the upper or lower column is transferred from the serial access port to the random access port, depending on the data input to A8. To confirm the transferred column side, check the output state of the QSF pin. Refer to **3.3.3 QSF Pin Output.**

When the serial address pointer comes to the jump source address specified by the STOP register, the serial address pointer jumps to the start column (TAP) of the serial read/write cycle at the inactive column side, and the TAP register will be set the empty state.

Figure 3-2. Split Mask Write Data Transfer and TAP Operations



3.3 Serial Read/Write

The serial access port (512K × 8 bits) is independent from the random access port and can perform read and write operations. The serial access port performing single data transfer and split data transfer can not perform read and write operations independently.

Caution When the power is turned on, the serial access port sets into the input (write) mode and the SIO pin is the high impedance state.

3.3.1 Serial Read Cycle

To set the serial read cycle, perform the single read data transfer cycle (The mode will not change in the split read data transfer cycle.).

Execute the single read data transfer cycle and latch the data and TAP data. By inputting a clock signal to the SC pin and inputting a low level to the $\overline{\mathrm{SE}}$ pin, data will be output from the serial address pointer specified by TAP register. The data synchronizes with the rising edge of the SC clock and is output from the SIO0 to SIO7 pin, and the data is kept until the next rising edge of the SC clock.

(a) Reading-Jump

The $\overline{\mathrm{SE}}$ pin controls the SIO pin output buffer independently from the SC clock. By setting the $\overline{\mathrm{SE}}$ pin to high level even while inputting the SC clock, SIO0 to SIO7 pins become high impedance. But the operations of serial address pointer will be continued while the SC clock is being input even though reading has been prohibited from $\overline{\mathrm{SE}}$ pin. Reading-jump of the column can be performed using this function.

3.3.2 Serial Write Cycle

To set the serial write cycle, perform the single write data transfer cycle (The mode will not change in the split write data transfer cycle.). To prevent the transfer data from being written in the memory cell of the random access port, set all bits of the mask data to "0" and control the mask data.

Execute the single write data transfer cycle and set the serial write cycle. By inputting the clock signal to the SC pin and inputting a low level to the $\overline{\mathrm{SE}}$ pin, data can be latched from the serial address pointer specified by TAP register. The data synchronizes with the rising edge of the SC clock and is input from SIO0 to SIO7 pins. Be sure to follow the specifications for the setup time (t_{SES}) and hold time (t_{SEH}) of $\overline{\mathrm{SE}}$ pin for the SC clock.

(a) Writing-Jumps (Intermittent Writing)

The $\overline{\mathrm{SE}}$ pin controls writing operations independently from the SC clock. By setting the $\overline{\mathrm{SE}}$ pin to high level even while inputting the SC clock, writing will not be executed. But the operations of serial address pointer will be continued while the SC clock is being input even though writing has been prohibited from $\overline{\mathrm{SE}}$ pin. These functions enable writing-jumps (intermittent writing) to be performed. The masked data is kept as the old data.

3.3.3 QSF Pin Output

QSF pin determines whether the serial address pointer is at the upper column side (addresses 256 to 511) or the lower column side (addresses 0 to 255) at the rising edge of the following SC clock during serial read or write. In other words, it outputs the uppermost bit (A8) of the column address of the serial address pointer.

The following table shows the QSF pin output state and the access pointer of following SC clocks.

Access Address of Following SC clock	QSF Output
Addresses 0 to 255	Low level
Addresses 256 to 511	High level

3.4 TAP (Top Access Point) Register

The TAP register is a data register which specifies the start address (first serial address point = TAP) of the serial read or serial write.

Set data to this register each time a transfer cycle is executed.

3.4.1 Setting of TAP Register

The data input to A0 to A8 at the falling edge of $\overline{\text{CAS}}$ during the setting of a transfer cycle is set as the TAP register data. By executing the transfer cycle, the start address of the following serial read (or write) operations is specified by the data of the TAP register and the TAP register will be kept in the empty state until the TAP register is set again.

In the split data transfer cycle (Versions A and F: For "MSB Don't Care"), because the inactive serial access port column addresses are specified by the data of the TAP register automatically, there is no need to control the A8 data. However in the split data transfer cycle (Version E: For "MSB Care"), the data in the TAP register, which is input to A8, specifies the column on the side that performs the transfer (A8 = 0: Lower column, A8 = 1: Upper column).

Caution **When the TAP register is empty, the address following the 511 serial address point will be 0. In addition, because the serial address pointer will not jump to the column specified by the STOP register, the binary boundary jump function cannot be used. Refer to 3.6 Binary Boundary Jump Function.**

3.5 STOP Register

The STOP register is a data register which determines the column of the jump source when jumping to a different column side (lower column or upper column) in the split data transfer cycle. Five types of columns can be selected for starting jump (jumping is possible at 2, 4, 8, 16, and 32 points). The following table shows the correspondence between the column at the jump source and data of the STOP register.

Once set, the STOP register data is kept until it is set again.

3.5.1 Setting of STOP Register

To set the STOP register, set $\overline{\text{WB}}/\overline{\text{WE}}$ to low level at the falling edge of $\overline{\text{RAS}}$ in the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. The data input to A0 to A7 will be input as the STOP register data.

Table 3-7. STOP Register Data and Jump Source Column

STOP Register Data					Division	Bit Width	Jump Source Bit Column (Decimal Number)
A7	A6	A5	A4	A3 to A0			
1	1	1	1	1	1/2	256	255
							511
0	1	1	1	1	1/4	128	127, 255
							383, 511
0	0	1	1	1	1/8	64	63, 127, 191, 255
							319, 383, 447, 511
0	0	0	1	1	1/16	32	31, 63, 95, 127, 159, 191, 223, 255
							287, 319, 351, 383, 415, 447, 479, 511
0	0	0	0	1	1/32	16	15, 31, 47, 63, 79, 95, 111, 127, 143, 159, 175, 191, 207, 223, 239, 255
							271, 287, 303, 319, 335, 351, 367, 383, 399, 415, 431, 447, 463, 479, 495, 511

Remark A8: Don't care.

Caution When the power is supplied, all STOP register data will be set to all "1".

3.6 Binary Boundary Jump Function

This function causes the serial address pointer jump to the TAP specified by the TAP register when the pointer moves to a column specified by the STOP register (split data transfer).

This function cannot be used when the jump destination address is not set (TAP register is empty).

This function facilitates tile map application which divides the screen into tiles and manages data for each tile.

3.6.1 Usage of Binary Boundary Jump Function

After setting the STOP register, execute the single read (or write) data transfer and initialize the serial access port. The initialization process will switch the serial access port read (or write) operations, set TAP, set the serial access port data, and set the TAP register to empty. By inputting the serial clock in this state, the serial access port will read (or write) operations from TAP in ascending order of address. Because the TAP register is in the empty state, the address at the jump source set by the STOP register will be ignored, and the serial address pointer will move on.

When the column to be jumped approaches, execute split data transfer and set new TAP data in the TAP register. The serial pointer will jump at the desired jump source address. Jump can be controlled freely by repeating these operations.

3.7 Special Operations

3.7.1 Serial Address Set Operations

Because the serial address counter is undefined when the power up, the serial access port operations when the SC clock is input are not guaranteed. Execute single read (or write) transfer after turning on the power. The serial access port will be initialized, enabling serial access port operations to be performed.

3.7.2 Lap Around Operations

If all the data of the register is read (write) during data transfer while the serial read (write) cycle is being executed, the serial pointer will repeat 0 to 511.

3.7.3 Cycle After Power On

After supplying power, initialize the internal circuitry by waiting for at least 100 μs after $V_{CC} \geq 4.5$ V, then supplying at least 8 $\overline{\text{RAS}}$ clock cycles. The $\overline{\text{RAS}}$ clock only requires that t_{RC}, t_{RAS}, and t_{RP} are satisfied; there is no problem if other signals are in any state. Note however that if the signal supplied to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{DT}}/\overline{\text{OE}}$, and $\overline{\text{WB}}/\overline{\text{WE}}$ is high at power-on, the serial access port and each register have the following values.

- Serial access port ....Input mode, SIO: High impedance
- Color register ....Undefined
- Mask register ....All "1"
- TAP register ....Undefined
- STOP register ....All "1"

4. Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Pin voltage	V_T	–1.0 to +7.0	V
Supply voltage	V_{CC}	–1.0 to +7.0	V
Output current	I_O	50	mA
Power dissipation	P_D	1.5	W
Operating ambient temperature	T_A	0 to 70	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits in the operational sections of this characteristics. Exposure to Absolute Maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
High level input voltage	V_{IH}	2.4		5.5	V
Low level input voltage	V_{IL}	–1.0		+0.8	V
Operating ambient temperature	T_A	0		70	°C

DC Characteristics 1 (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input leakage current	I_{IL}	V_{IN} = 0 V to 5.5 V, Other inputs are 0 V	−10		+10	μA
Output leakage current	I_{OL}	W/IO, SIO, QSF are inactive, V_{OUT} = 0 V to 5.5 V	−10		+10	μA
Random access port high level output voltage	V_{OH} (R)	I_{OH} (R) = −1.0mA	2.4			V
Random access port low level output voltage	V_{OL} (R)	I_{OL} (R) = 2.1mA			0.4	V
Serial access port high level output voltage	V_{OH} (S)	I_{OH} (S) = −1.0mA	2.4			V
Serial access port low level output voltage	V_{OL} (S)	I_{OL} (S) = 2.1mA			0.4	V

Capacitance (T_A = 25 °C, f = 1MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WB}}/\overline{\text{WE}}$, $\overline{\text{DT}}/\overline{\text{OE}}$, DSF, $\overline{\text{SE}}$, SC			8	pF
	C_{I2}	A0 to A8			5	
Input/Output Capacitance	C_{IO}	W/IO (0 to 7), SIO (0 to 7)			7	pF
Output Capacitance	C_O	QSF			7	pF

DC Characteristics 2 (Recommended operating conditions unless otherwise noted)[Note 1]

(μPD482234)

Random Access Port	Serial Access Port		Symbol	μPD482234-60		μPD482234-70		μPD482234-80		Unit	Conditions
	Standby	Active		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read/Write Cycle $\overline{RAS}$, $\overline{CAS}$ cycle, $t_{RC} = t_{RC}$ (MIN.), I_O = 0mA	○		I_{CC1}		110		130		130	mA	Note 2
		○	I_{CC7}		155		195		190		
Standby $\overline{RAS} = \overline{CAS} = V_{IH}$, D_{OUT} = high impedance	○		I_{CC2}		10		10		10	mA	
					1		1		1	mA	Note 3
		○	I_{CC8}		55		70		65	mA	
$\overline{RAS}$ only refresh cycle $\overline{RAS}$ cycle, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ (MIN.)	○		I_{CC3}		110		115		115	mA	Note 4
		○	I_{CC9}		155		180		175		
Fast page mode cycle $\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycle, $t_{PC} = t_{PC}$ (MIN.)	○		I_{CC4}		100		100		90	mA	Note 5
		○	I_{CC10}		145		165		150		
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle $t_{RC} = t_{RC}$ (MIN.)	○		I_{CC5}		110		90		90	mA	
		○	I_{CC11}		155		155		150		
Data transfer cycle $t_{RC} = t_{RC}$ (MIN.)	○		I_{CC6}		120		140		140	mA	
		○	I_{CC12}		165		205		200		
Color/Mask write register set cycle $t_{RC} = t_{RC}$ (MIN.)	○		I_{CC13}		100		120		120	mA	
		○	I_{CC14}		145		185		180		
Flash write cycle $t_{RC} = t_{RC}$ (MIN.)	○		I_{CC15}		100		120		120	mA	
		○	I_{CC16}		145		185		180		
Block write cycle $t_{RC} = t_{RC}$ (MIN.)	○		I_{CC17}		120		130		130	mA	
		○	I_{CC18}		165		195		190		
Fast page mode block write cycle $t_{PC} = t_{PC}$ (MIN.)	○		I_{CC19}		100		110		100	mA	
		○	I_{CC20}		130		175		160		Note 5

Notes 1. No load on W/IO, SIO, QSF. The current consumption actually used depends on the output load and operating frequency of each pin.

2. A change in row addresses must not occur more than once in $t_{RC} = t_{RC}$ (MIN.).
3. $\overline{RAS}$, $\overline{CAS}$, and $\overline{SE}$ remain at $V_{IH} \geq V_{CC} - 0.2$ V, and A0 to A8, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, DSF, SC remain at $V_{IH} \geq V_{CC} - 0.2$ V or $V_{IL} \leq GND + 0.2$ V.
4. When the address input is set to V_{IH} or V_{IL} during the t_{RAS} period.
5. Value when the address in t_{PC} one cycle is changed once when $t_{PC} = t_{PC}$ (MIN.).

DC Characteristics 2 (Recommended operating conditions unless otherwise noted)Note 1 (μPD482235)

Random Access Port	Serial Access Port		Symbol	μPD482235-60		μPD482235-70		μPD482235-80		Unit	Conditions
	Standby	Active		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read/Write Cycle $\overline{RAS}$, $\overline{CAS}$ cycle, $t_{RC} = t_{RC}$ (MIN.), I_O = 0mA	○		I_{CC1}		110		130		130	mA	**Note 2**
		○	I_{CC7}		155		195		190		
Standby $\overline{RAS} = \overline{CAS} = V_{IH}$, D_{OUT} = high impedance	○		I_{CC2}		10		10		10	mA	
					1		1		1	mA	**Note 3**
		○	I_{CC8}		55		70		65	mA	
$\overline{RAS}$ only refresh cycle $\overline{RAS}$ cycle, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ (MIN.)	○		I_{CC3}		110		115		115	mA	**Note 4**
		○	I_{CC9}		155		180		175		
Hyper page mode cycle $\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycle, $t_{HPC} = t_{HPC}$ (MIN.)	○		I_{CC4}		120		130		120	mA	**Note 5**
		○	I_{CC10}		155		195		180		
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle $t_{RC} = t_{RC}$ (MIN.)	○		I_{CC5}		110		90		90	mA	
		○	I_{CC11}		155		155		150		
Data transfer cycle $t_{RC} = t_{RC}$ (MIN.)	○		I_{CC6}		120		140		140	mA	
		○	I_{CC12}		165		205		200		
Color/Mask write register set cycle $t_{RC} = t_{RC}$ (MIN.)	○		I_{CC13}		100		120		120	mA	
		○	I_{CC14}		145		185		180		
Flash write cycle $t_{RC} = t_{RC}$ (MIN.)	○		I_{CC15}		100		120		120	mA	
		○	I_{CC16}		145		185		180		
Block write cycle $t_{RC} = t_{RC}$ (MIN.)	○		I_{CC17}		120		130		130	mA	
		○	I_{CC18}		165		195		190		
Hyper page mode block write cycle $t_{HPC} = t_{HPC}$ (MIN.)	○		I_{CC19}		140		135		125	mA	
		○	I_{CC20}		190		200		185		**Note 5**

Notes

1. No load on W/IO, SIO, QSF. The current consumption actually used depends on the output load and operating frequency of each pin.
2. A change in row addresses must not occur more than once in $t_{RC} = t_{RC}$ (MIN.).
3. $\overline{RAS}$, $\overline{CAS}$, and $\overline{SE}$ remain at $V_{IH} \geq V_{CC} - 0.2$ V, and A0 to A8, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, DSF, SC remain at $V_{IH} \geq V_{CC} - 0.2$ V or $V_{IL} \leq GND + 0.2$ V.
4. When the address input is set to V_{IH} or V_{IL} during the t_{RAS} period.
5. Value when the address in t_{HPC} one cycle is changed once when $t_{HPC} = t_{HPC}$ (MIN.).

AC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5.0 V ± 10 %, GND = 0 V)Notes 1, 2, 3, 4
(Common for μPD482234, 482235)

(1/4)

Parameter	Symbol	μPD482234-60 μPD482235-60		μPD482234-70 μPD482235-70		μPD482234-80 μPD482235-80		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{\text{RAS}}$	t_{RAC}		60		70		80	ns	**Note 5**
Access time from $\overline{\text{CAS}}$	t_{CAC}		15		20		25	ns	**Note 5**
Access time from column address	t_{AA}		30		35		40	ns	**Note 5**
Access time from $\overline{\text{CAS}}$ trailing edge	t_{ACP}		35		40		45	ns	
Access time from $\overline{\text{OE}}$	t_{OEA}		15		20		25	ns	
Serial output access time from SC	t_{SCA}		15		17		20	ns	
Serial output access time from $\overline{\text{SE}}$	t_{SEA}		15		17		20	ns	
Output disable time from $\overline{\text{SE}}$ high	t_{SEZ}	0	15	0	15	0	20	ns	**Note 6**
Random read or write cycle time	t_{RC}	120		140		150		ns	
Read modify-write cycle time	t_{RWC}	165		185		205		ns	
Transition time (Rise/Fall)	t_T	3	35	3	35	3	35	ns	
$\overline{\text{RAS}}$ precharge time	t_{RP}	50		60		60		ns	
$\overline{\text{RAS}}$ pulse width (Non page mode)	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ pulse width (Fast page/Hyper page mode)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ hold time	t_{RSH}	15		20		25		ns	
$\overline{\text{CAS}}$ precharge time (Non page mode)	t_{CPN}	10		10		10		ns	
$\overline{\text{CAS}}$ precharge time (Fast page/Hyper page mode)	t_{CP}	10		10		10		ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	20	40	20	50	22	55	ns	**Note 5**
$\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low precharge time	t_{CRP}	5		10		10		ns	
$\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low precharge time	t_{RPC}	10		10		10		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		12		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		10		12		ns	
$\overline{\text{RAS}}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	ns	**Note 5**
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30		35		40		ns	
Read command setup time	t_{RCS}	0		0		0		ns	

(Common for μPD482234, 482235)

(2/4)

Parameter	Symbol	μPD482234-60 μPD482235-60		μPD482234-70 μPD482235-70		μPD482234-80 μPD482235-80		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read command hold time after $\overline{\text{RAS}}$ high	t_{RRH}	0		0		0		ns	**Note 7**
Read command hold time after $\overline{\text{CAS}}$ high	t_{RCH}	0		0		0		ns	**Note 7**
$\overline{\text{OE}}$ hold time after $\overline{\text{RAS}}$ high	t_{ORH}	10		10		10		ns	**Note 8**
$\overline{\text{OE}}$ hold time after $\overline{\text{CAS}}$ high	t_{OCH}	10		10		10		ns	**Note 8**
Write command setup time	t_{WCS}	0		0		0		ns	**Note 10**
Write command hold time	t_{WCH}	10		12		15		ns	
Write command pulse width	t_{WP}	10		12		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	20		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	15		15		20		ns	
Data in setup time	t_{DS}	0		0		0		ns	**Note 9**
Data in hold time	t_{DH}	12		12		15		ns	**Note 9**
Refresh period	t_{REF}		8		8		8	ms	
$\overline{\text{CAS}}$ to $\overline{\text{WB}}/\overline{\text{WE}}$ delay time	t_{CWD}	40		40		50		ns	**Note 10**
$\overline{\text{RAS}}$ to $\overline{\text{WB}}/\overline{\text{WE}}$ delay time	t_{RWD}	85		90		105		ns	**Note 10**
Column address to $\overline{\text{WB}}/\overline{\text{WE}}$ delay time	t_{AWD}	55		55		65		ns	**Note 10**
$\overline{\text{CAS}}$ setup time (for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle)	t_{CSR}	0		0		0		ns	
$\overline{\text{CAS}}$ hold time (for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle)	t_{CHR}	10		10		12		ns	
$\overline{\text{DT}}$ low setup time	t_{DLS}	0		0		0		ns	
$\overline{\text{DT}}$ low hold time after $\overline{\text{RAS}}$ low	t_{RDH}	55		65		70		ns	**Note 11**
$\overline{\text{DT}}$ low hold time after $\overline{\text{RAS}}$ low	t_{RDHS}	10		25		30		ns	**Note 11**
$\overline{\text{DT}}$ low hold time after $\overline{\text{CAS}}$ low	t_{CDH}	15		20		25		ns	**Note 11**
$\overline{\text{DT}}$ low hold time after address	t_{ADD}	20		25		30		ns	**Note 11**
SC high to $\overline{\text{DT}}$ high	t_{SDD}	0		0		0		ns	**Note 11**
SC high to $\overline{\text{CAS}}$ low	t_{SSC}	10		10		10		ns	**Note 11, 15, 16**
SC low hold time after $\overline{\text{DT}}$ high	t_{SDH}	40		40		50		ns	**Note 11**

(Common for μPD482234, 482235) (3/4)

Parameter	Symbol	μPD482234-60 μPD482235-60		μPD482234-70 μPD482235-70		μPD482234-80 μPD482235-80		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
SC low hold time after $\overline{DT}$ high	t_{SDHR}	40		45		55		ns	**Note 11, 15**
$\overline{OE}$ high to data in setup delay time	t_{OED}	15		15		20		ns	
$\overline{OE}$ high hold time after $\overline{WB}/\overline{WE}$ low	t_{OEH}	0		0		0		ns	
Serial clock cycle time	t_{SCC}	18		22		25		ns	
SC pulse width	t_{SCH}	5		5		7		ns	
SC precharge time	t_{SCL}	5		5		7		ns	
$\overline{SE}$ low to serial output setup delay time	t_{SOO}	3		5		5		ns	
Serial output hold time after SC high	t_{SOH}	3		5		5		ns	
$\overline{DT}$ high setup time	t_{DHS}	0		0		0		ns	
$\overline{DT}$ high hold time	t_{DHH}	10		10		12		ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay time	t_{DTR}	0		0		0		ns	**Note 11**
$\overline{DT}$ high pulse width	t_{DTP}	20		20		25		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		ns	
Write-per-bit setup time	t_{WBS}	0		0		0		ns	
Write-per-bit hold time	t_{WBH}	10		10		12		ns	
DSF setup time from $\overline{RAS}$	t_{FRS}	0		0		0		ns	
DSF hold time from $\overline{RAS}$	t_{FRH}	10		10		12		ns	
DSF setup time from $\overline{CAS}$	t_{FCS}	0		0		0		ns	
DSF hold time from $\overline{CAS}$	t_{FCH}	10		12		15		ns	
Write-per-bit selection setup time	t_{WS}	0		0		0		ns	
Write-per-bit selection hold time	t_{WH}	10		10		12		ns	
$\overline{SE}$ pulse width	t_{SEE}	5		5		7		ns	
$\overline{SE}$ precharge time	t_{SEP}	5		5		7		ns	
$\overline{SE}$ setup time	t_{SES}	0		0		0		ns	
$\overline{SE}$ hold time from SC	t_{SEH}	10		10		12		ns	
Serial data in setup time	t_{SIS}	0		0		0		ns	
Serial data in hold time	t_{SIH}	10		10		12		ns	
Serial input disable time from SC	t_{SIZ}	0		0		0		ns	
Serial output disable time from $\overline{RAS}$	t_{SRZ}	0		0		0		ns	

(Common for μPD482234, 482235)

(4/4)

Parameter	Symbol	μPD482234-60 μPD482235-60		μPD482234-70 μPD482235-70		μPD482234-80 μPD482235-80		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Serial input enable time from $\overline{RAS}$	t_{SZH}	20		20		25		ns	
SC setup time from $\overline{RAS}$	t_{SRS}	10		10		10		ns	**Note 14, 15, 16**
SC hold time from $\overline{RAS}$	t_{SRH}	10		10		10		ns	**Note 14**
Propagation delay time from SC to QSF	t_{PD}		20		20		25	ns	
Propagation delay time from $\overline{RAS}$ to QSF	t_{RQD}		80		95		105	ns	
Propagation delay time from $\overline{CAS}$ to QSF	t_{CQD}		60		65		75	ns	
Propagation delay time from $\overline{DT}/\overline{OE}$ to QSF	t_{DQD}		30		30		35	ns	
Propagation delay time from $\overline{RAS}$ high to QSF	t_{DQR}		40		40		45	ns	

(μPD482234 Only)

Parameter	Symbol	μPD482234-60		μPD482234-70		μPD482234-80		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Output disable time from $\overline{CAS}$ high	t_{OFF}	0	15	0	15	0	20	ns	**Note 6, 12**
Output disable time from $\overline{OE}$ high	t_{OEZ}	0	15	0	15	0	20	ns	**Note 6, 12**
Output disable time from $\overline{WB}/\overline{WE}$ low	t_{WEZ}	0	15	0	15	0	20	ns	**Note 6, 12**
Write command pulse width	t_{WPZ}	10		12		15		ns	**Note 12**
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read modify write cycle time	t_{PRWC}	90		90		105		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	

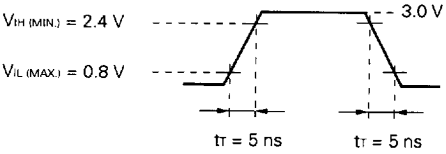
(μPD482235 Only)

Parameter	Symbol	μPD482235-60		μPD482235-70		μPD482235-80		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from previous $\overline{CAS}$	t_{ACE}		60		65		75	ns	**Note 17**
Access time from previous $\overline{WE}$	t_{AWE}		55		60		70	ns	**Note 17**
Output hold time from $\overline{CAS}$	t_{DHC}	3		5		5		ns	
Output disable time from $\overline{RAS}$ high	t_{OFR}	0	15	0	15	0	20	ns	**Note 6, 13**
Output disable time from $\overline{CAS}$ high	t_{OFC}	0	15	0	15	0	20	ns	**Note 6, 13**
Output disable time from $\overline{OE}$ high	t_{OEZ}	0	15	0	15	0	20	ns	**Note 6, 13**
Output disable time from $\overline{WB}/\overline{WE}$ low	t_{WEZ}	0	15	0	15	0	20	ns	**Note 6, 13**
Write command pulse width	t_{WPZ}	10		12		15		ns	**Note 13**
Hyper page mode cycle time	t_{HPC}	30		35		40		ns	
Hyper page mode read modify write cycle time	t_{HPRWC}	80		90		105		ns	
$\overline{CAS}$ pulse width	t_{HCAS}	10	10,000	10	10,000	12	10,000	ns	

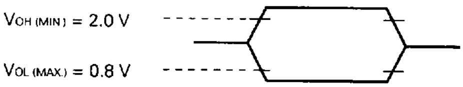
Notes 1. All applied voltages are referenced to GND.

2. After supplying power, initialize the internal circuitry by waiting for at least 100 μs after $V_{CC} \geq 4.5$ V, then supplying at least 8 $\overline{\text{RAS}}$ clock cycles. The $\overline{\text{RAS}}$ clock only requires t_{RC}, t_{RAS}, and t_{RP} are satisfied; there is no problem if other signals are in any state.
3. Measure at $t_T = 5$ ns
4. AC characteristic measuring conditions

(1) Input voltage, timing

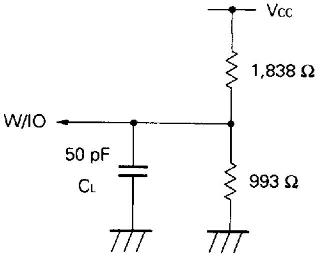


(2) Output voltage determined

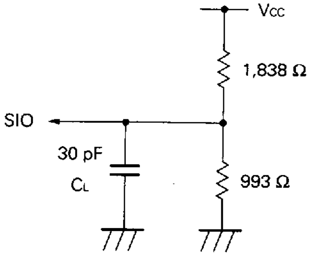


(3) Output load conditions

Random Access Port



Serial Access Port



5. For read cycle, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{\text{RAS}}$
$t_{RAD} \leq t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{RAC} (MAX.)	t_{RAC} (MAX.)
$t_{RAD} > t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{AA} (MAX.)	$t_{RAD} + t_{AA}$ (MAX.)
$t_{RCD} > t_{RCD}$ (MAX.)	t_{CAC} (MAX.)	$t_{RCD} + t_{CAC}$ (MAX.)

t_{RAD} (MAX.) and t_{RCD} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA}, t_{CAC}) is to be used for finding out data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}$ (MAX.) and $t_{RCD} \geq t_{RCD}$ (MAX.) will not cause any operation problems.

6. t_{SEZ}, t_{OEZ}, t_{WEZ}, t_{OFF}, t_{OFR}, and t_{OFC} define the time when the output achieves the condition of high impedance and is not referenced to V_{OH} or V_{OL}.
7. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
8. Because t_{ORH} and t_{OCH} are used during the mask register set cycle (new mask selection) only, these ratings are applied only to versions F and E.
9. These parameters are referenced to the following points.
   (1) Early write cycle : The falling edge of $\overline{\text{CAS}}$
   (2) Late write cycle : The falling edge of $\overline{\text{WB/WE}}$
   (3) Read modify write cycle : The falling edge of $\overline{\text{WB/WE}}$

Notes 10. $t_{WCS} \geq t_{WCS}$ (MIN.) is the condition for early write cycle to be set. D_{OUT} becomes high impedance during the cycle.
$t_{RWD} \geq t_{RWD}$ (MIN.), $t_{CWD} \geq t_{CWD}$ (MIN.), $t_{AWD} \geq t_{AWD}$ (MIN.), are conditions for read modify write cycle to be set. The data of the selected address is output to D_{OUT}.
If any of the above conditions are not met, pin W/IO will become undefined.

11. One of the following specifications will be valid depending on the type of read data transfer method used.
    (1) $\overline{\text{DT}}/\overline{\text{OE}}$ edge control: Satisfy the following specifications.
    - For $\overline{\text{DT}}/\overline{\text{OE}}$ edge inputs : t_{RDH}, t_{CDH}, t_{ADD}, t_{DTR}
    - For SC inputs : t_{SDD}, t_{SDH}

    (2) Self control: Satisfy the following specification.
    - For $\overline{\text{DT}}/\overline{\text{OE}}$ edge inputs : t_{RDHS}
    - For SC inputs : t_{SSC}, t_{SDHR}

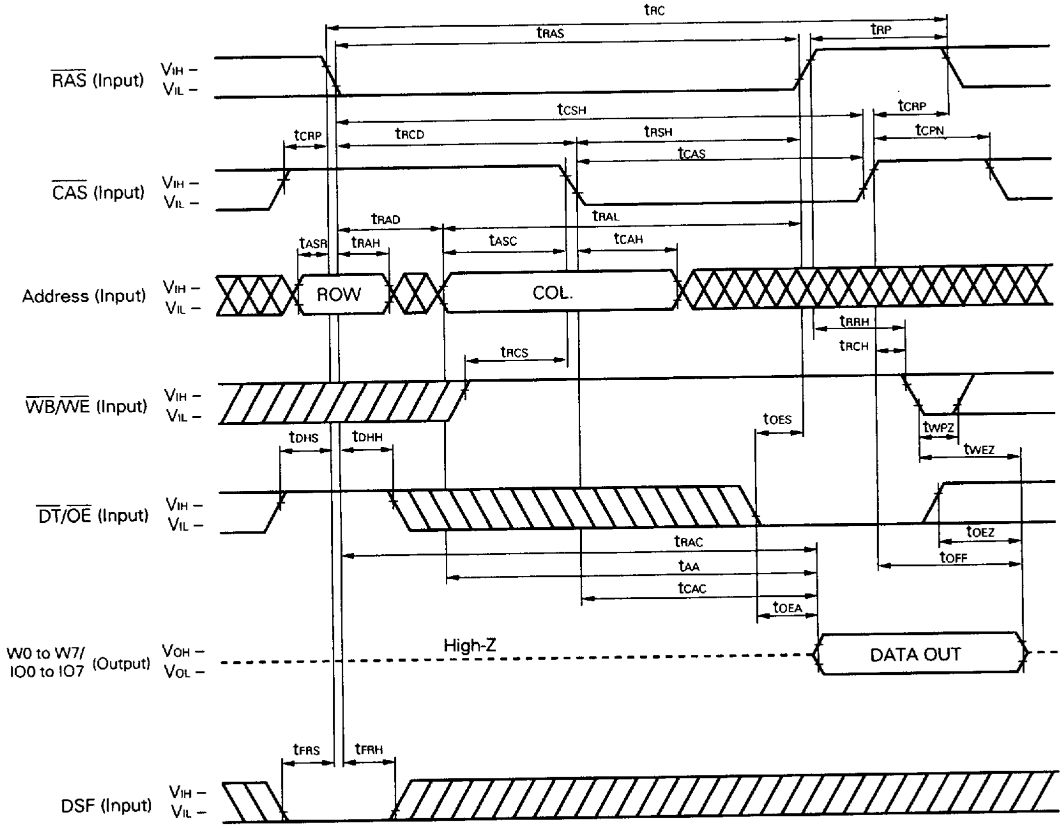
12. Control pins $\overline{\text{CAS}}$, $\overline{\text{DT}}/\overline{\text{OE}}$, $\overline{\text{WB}}/\overline{\text{WE}}$ to set pin W/IO to high impedance. Because the timings at which CAS and $\overline{\text{DT}}/\overline{\text{OE}}$ are set to high level and $\overline{\text{WB}}/\overline{\text{WE}}$ is set to low level affect the high impedance state, the specifications will change as follows.
    (1) When $\overline{\text{CAS}}$ is set to high level at $\overline{\text{DT}}/\overline{\text{OE}}$ (low level) and $\overline{\text{WB}}/\overline{\text{WE}}$ (high level) at the end of the read cycle: t_{OFF} is valid
    (2) When $\overline{\text{WB}}/\overline{\text{WE}}$ is set to low level at $\overline{\text{CAS}}$ (low level) and $\overline{\text{DT}}/\overline{\text{OE}}$ (low level) at the end of the read cycle: t_{WEZ} and t_{WPZ} are valid
    (3) When $\overline{\text{DT}}/\overline{\text{OE}}$ is set to high level at $\overline{\text{CAS}}$ (low level) and $\overline{\text{WB}}/\overline{\text{WE}}$ (high level) at the end of the read cycle: t_{OEZ} is valid

13. Control pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{DT}}/\overline{\text{OE}}$, $\overline{\text{WB}}/\overline{\text{WE}}$ to set pin W/IO to high impedance. Because the timings at which $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{DT}}/\overline{\text{OE}}$ are set to high level and $\overline{\text{WB}}/\overline{\text{WE}}$ is set to low level affect the high impedance state, the specifications will change as follows.
When controlling $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$, the output cannot be made high impedance unless both pins are set to high. There is difference between t_{OFC} and t_{OFR}, because $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ control is specified from the rising edge of the slower one.
    (1) When $\overline{\text{RAS}}$ is set to high level after $\overline{\text{CAS}}$ is set to high level at $\overline{\text{DT}}/\overline{\text{OE}}$ (low level) and $\overline{\text{WB}}/\overline{\text{WE}}$ (high level) at the end of the read cycle: t_{OFR} is valid
    (2) When $\overline{\text{CAS}}$ is set to high level after $\overline{\text{RAS}}$ is set to high level at $\overline{\text{DT}}/\overline{\text{OE}}$ (low level) and $\overline{\text{WB}}/\overline{\text{WE}}$ (high level) at the end of the read cycle: t_{OFC} is valid
    (3) When $\overline{\text{WB}}/\overline{\text{WE}}$ is set to low level at $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ (low level) and $\overline{\text{DT}}/\overline{\text{OE}}$ (low level) at the end of the read cycle: t_{WEZ} and t_{WPZ} are valid
    (4) When $\overline{\text{DT}}/\overline{\text{OE}}$ is set to high level at $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ (low level) and $\overline{\text{WB}}/\overline{\text{WE}}$ (high level) at the end of the read cycle: t_{OEZ} is valid

14. The t_{SRS} and t_{SRH} in the hidden refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle (STOP register set cycle and optional reset cycle) are specified to guarantee the serial port operations until the transfer cycle is executed after the STOP register value is changed. When the STOP register value is not to be changed, or when the binary boundary jump function is not used (when the TAP register is empty), t_{SRS} and t_{SRH} will not be specified.

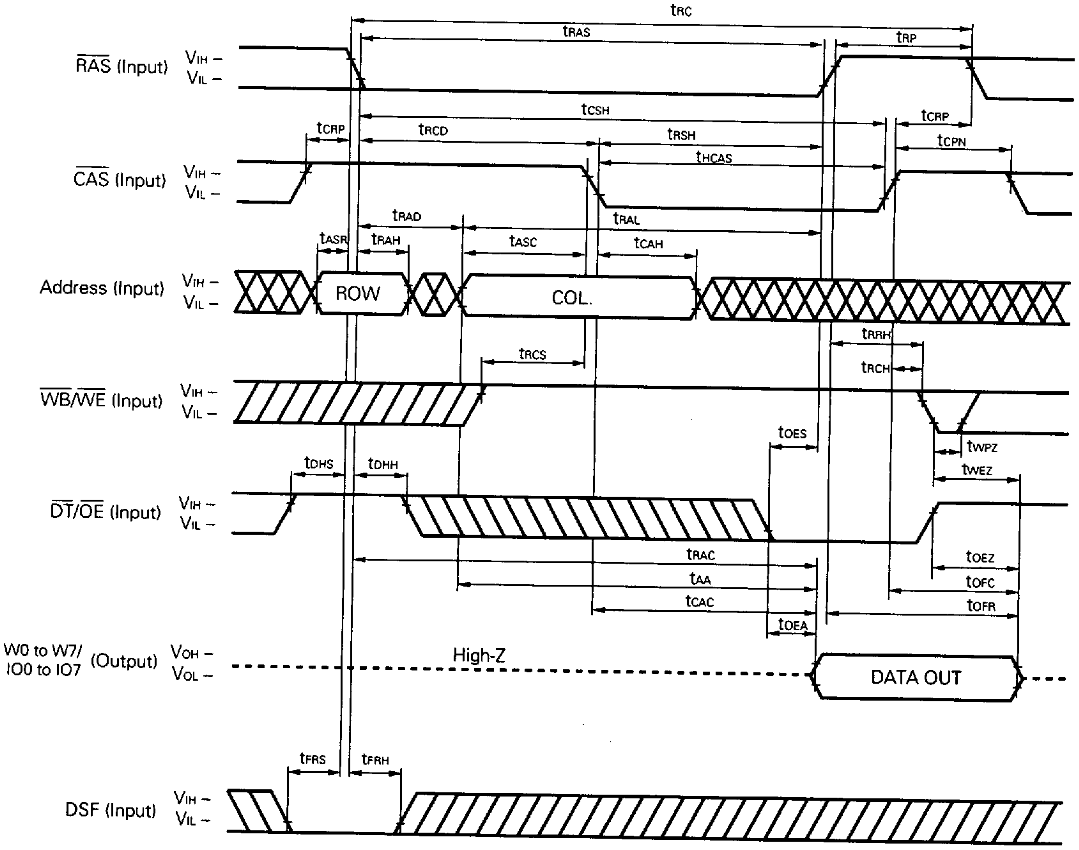
15. t_{SSC} (split read data transfer cycle) and t_{SRS} (split write data transfer cycle) are specified at the rising edge of SC which reads/writes the address of the jump source in the binary boundary jump function. t_{SDHR} (split read data transfer cycle and split write data transfer cycle) is specified at the rising edge of SC which reads/writes the address of the jump destination in the binary boundary jump function. The rising edge of these SCs cannot be input in periods (1) and (2).
    (1) Split read data transfer cycle: Period from the rising edge of the SC specifying t_{SSC} to that of the SC specifying t_{SDHR} (Refer to **Note 2 Split Read/Write Data Transfer Cycle Timing Chart.**)
    (2) Split write data transfer cycle: Period from the rising edge of the SC specifying t_{SRS} to that of the SC specifying t_{SDHR} (Refer to **Note 2 Split Read/Write Data Transfer Cycle Timing Chart.**)
16. Restrictions to the split read data transfer cycle during serial write operation
    (1) If split read data transfer is attempted for an address which is already involved in serial write, normal operation is not guaranteed, except for a period in which no serial write has been performed, that is from when $\overline{SE}$ goes low at the rising edge of SC to just before the serial write begins.
    (2) If split read data transfer is attempted when an address involved in serial write is the boundary address specified by the STOP register, normal operation is not guaranteed, except for a period in which no serial write has been performed, that is from just after the mask write or mask split write transfer cycle is executed to just before the serial write is started by setting $\overline{SE}$ to a low level at the rising edge of SC.
17. In the hyper page mode, the hyper page mode read modify write cycle, the hyper page mode read modify block write cycle, this parameter is valid when the read cycle changes to the write cycle.

Read Cycle (μPD482234)



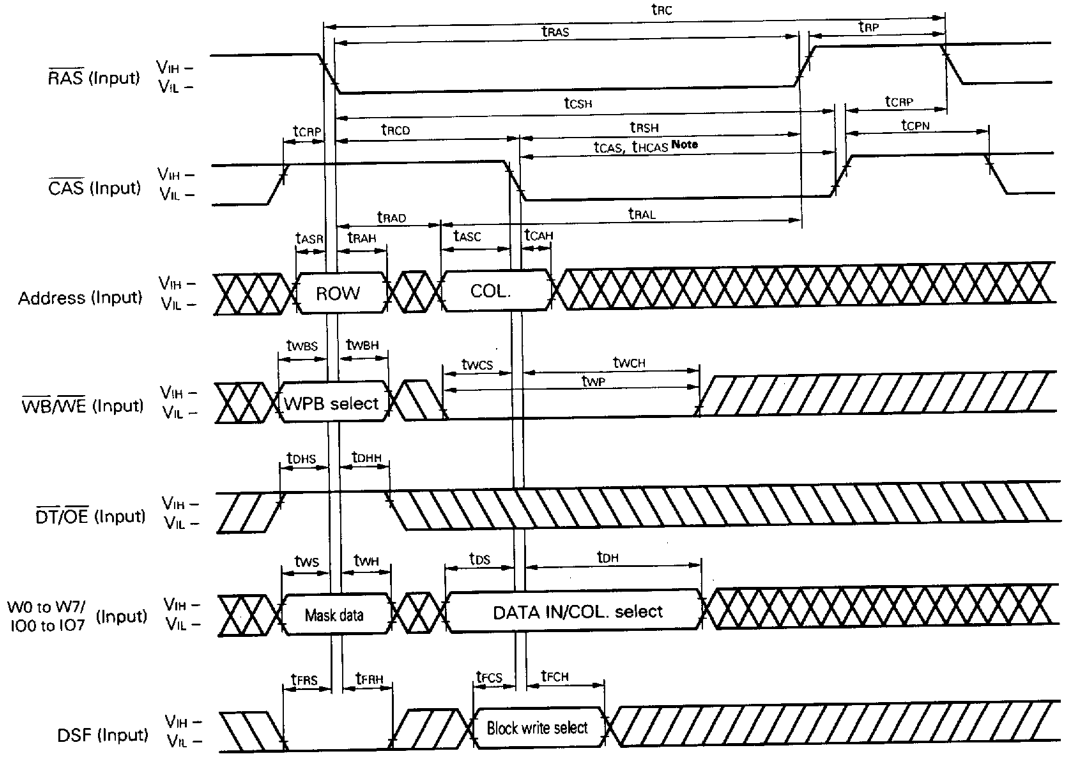
Remark Because the serial access port operates independently of the random access port, there is no need to control the SC, $\overline{\text{SE}}$, SIO pins in this cycle.

Read Cycle (Extended data output: μPD482235)



Remark Because the serial access port operates independently of the random access port, there is no need to control the SC, SE, SIO pins in this cycle.

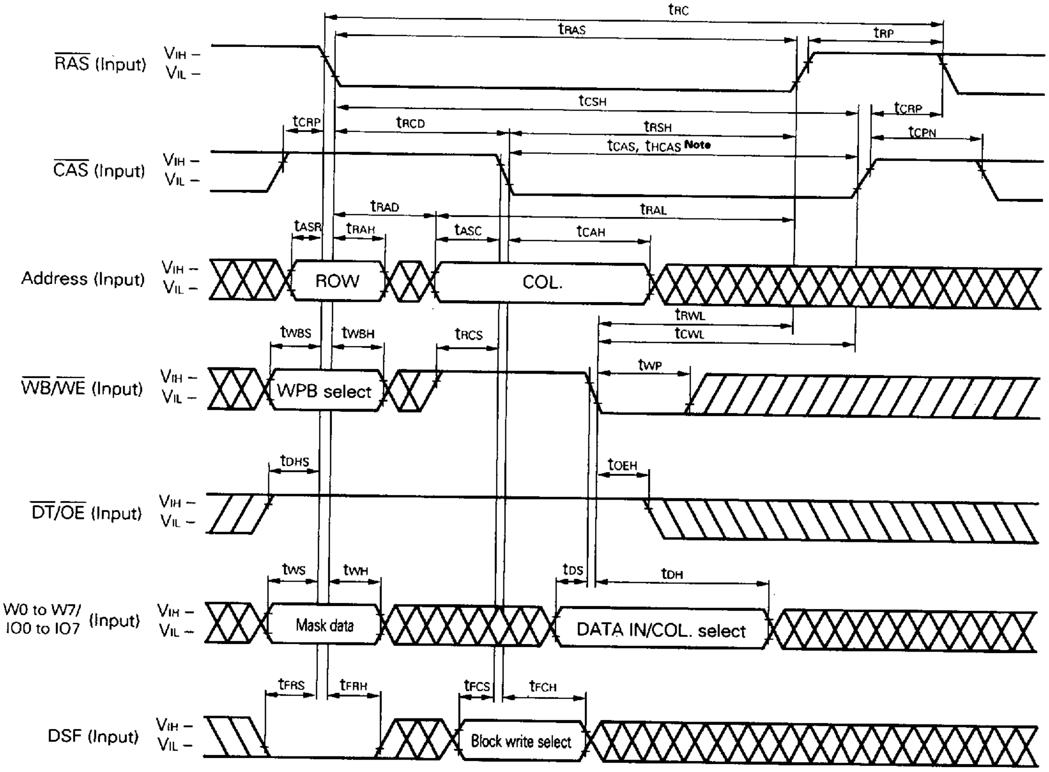
Early Write Cycle/Early Block Write Cycle



Note tCAS for the μPD482234
tHCAS for the μPD482235

Remarks
1. When DSF is high level : Block write cycle
   When DSF is low level : Write cycle
2. WPB : Write-per-bit
3. When block write cycle is selected, input the column selection data to DATA IN.
4. Because the serial access port operates independently of the random access port, there is no need to control the SC, SE, SIO pins in this cycle.

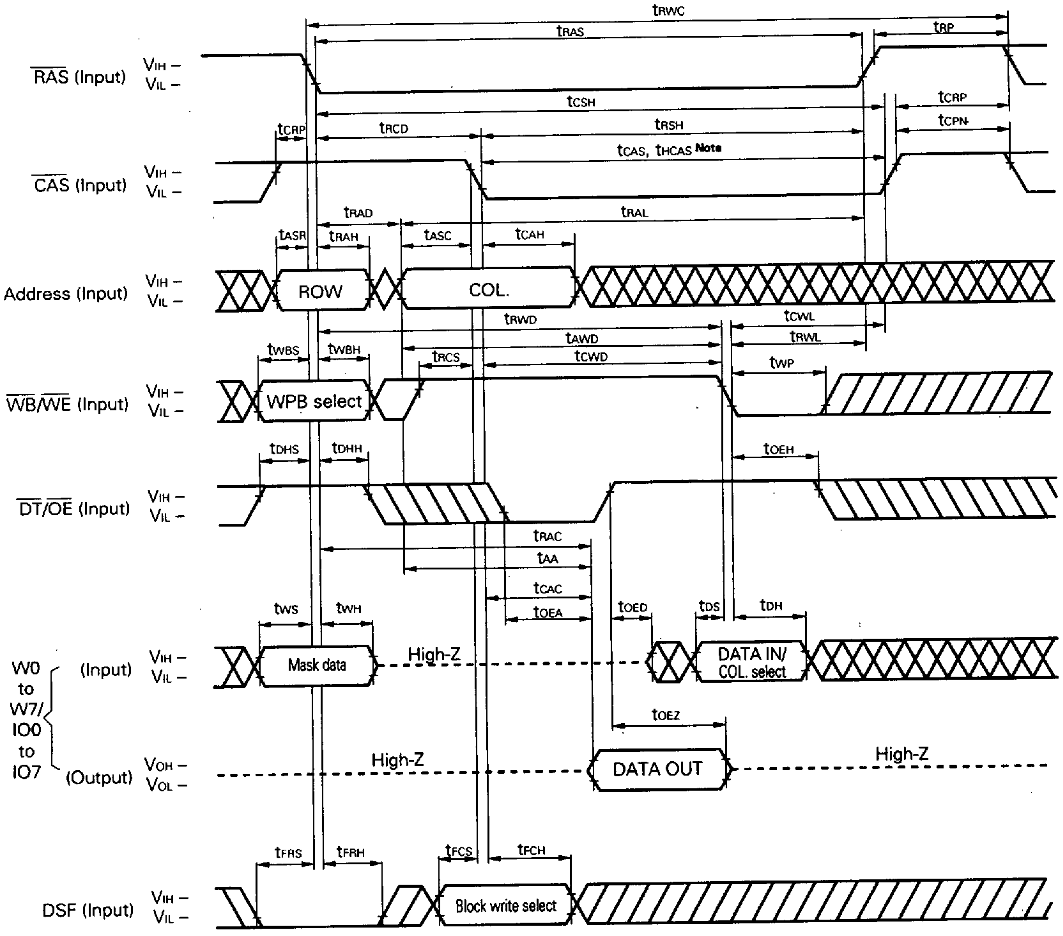
Late Write Cycle/Late Block Write Cycle



Note tCAS for the μPD482234
tHCAS for the μPD482235

Remarks
1. When DSF is high level : Block write cycle
   When DSF is low level : Write cycle
2. WPB : Write-per-bit
3. When block write cycle is selected, input the column selection data to DATA IN.
4. Because the serial access port operates independently of the random access port, there is no need to control the SC, SE, SIO pins in this cycle.

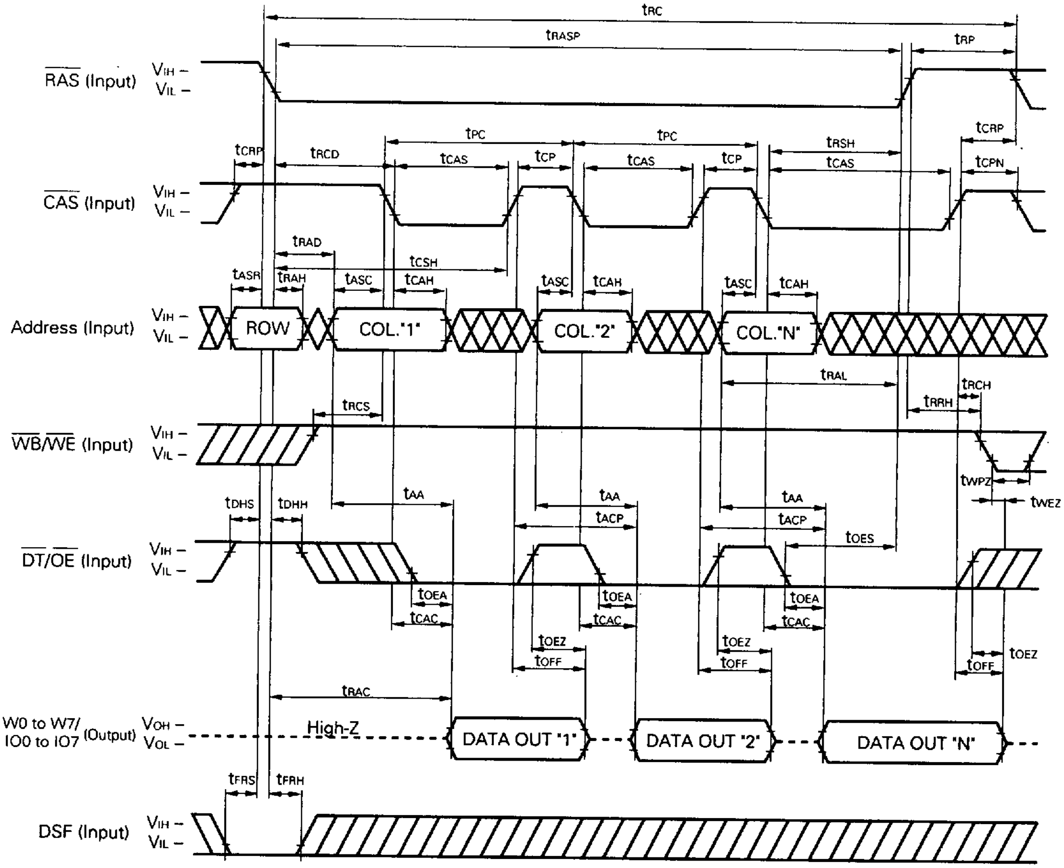
Read Modify Write Cycle/Read Modify Block Write Cycle



Note tCAS for the μPD482234
tHCAS for the μPD482235

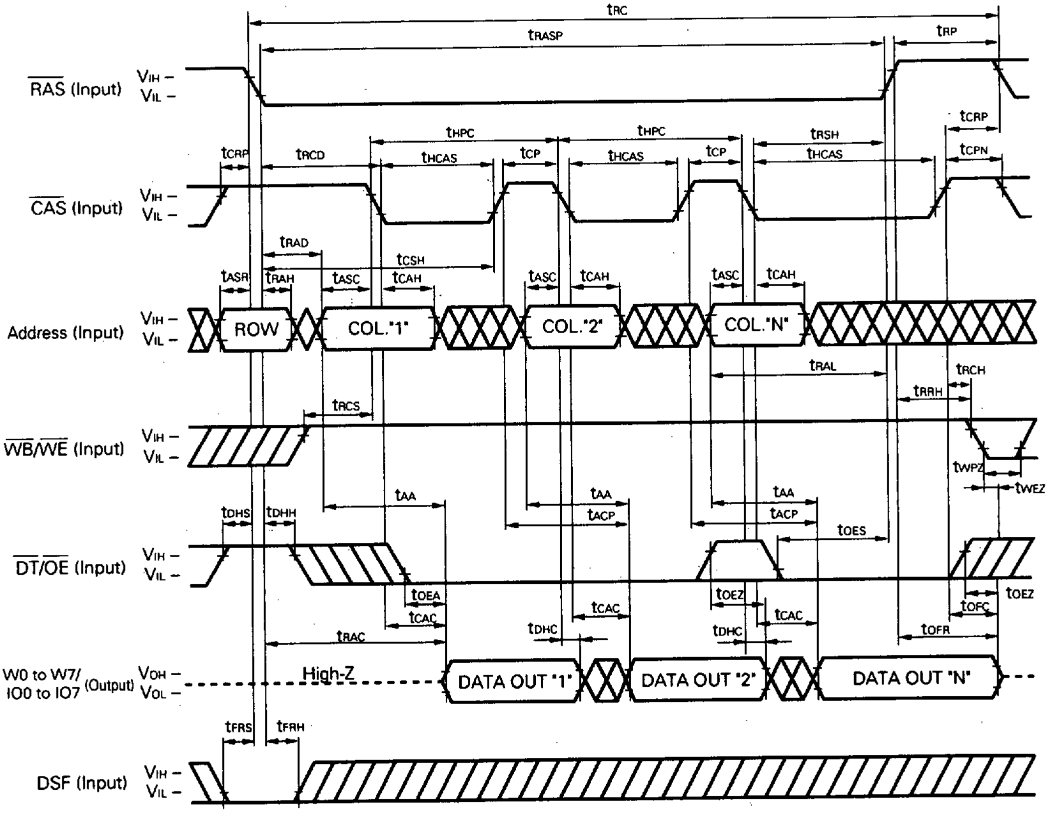
Remarks
1. When DSF is high level : Block write cycle
   When DSF is low level : Write cycle
2. WPB : Write-per-bit
3. When block write cycle is selected, input the column selection data to DATA IN.
4. Because the serial access port operates independently of the random access port, there is no need to control the SC, SE, SIO pins in this cycle.

Fast Page Mode Read Cycle (μPD482234)



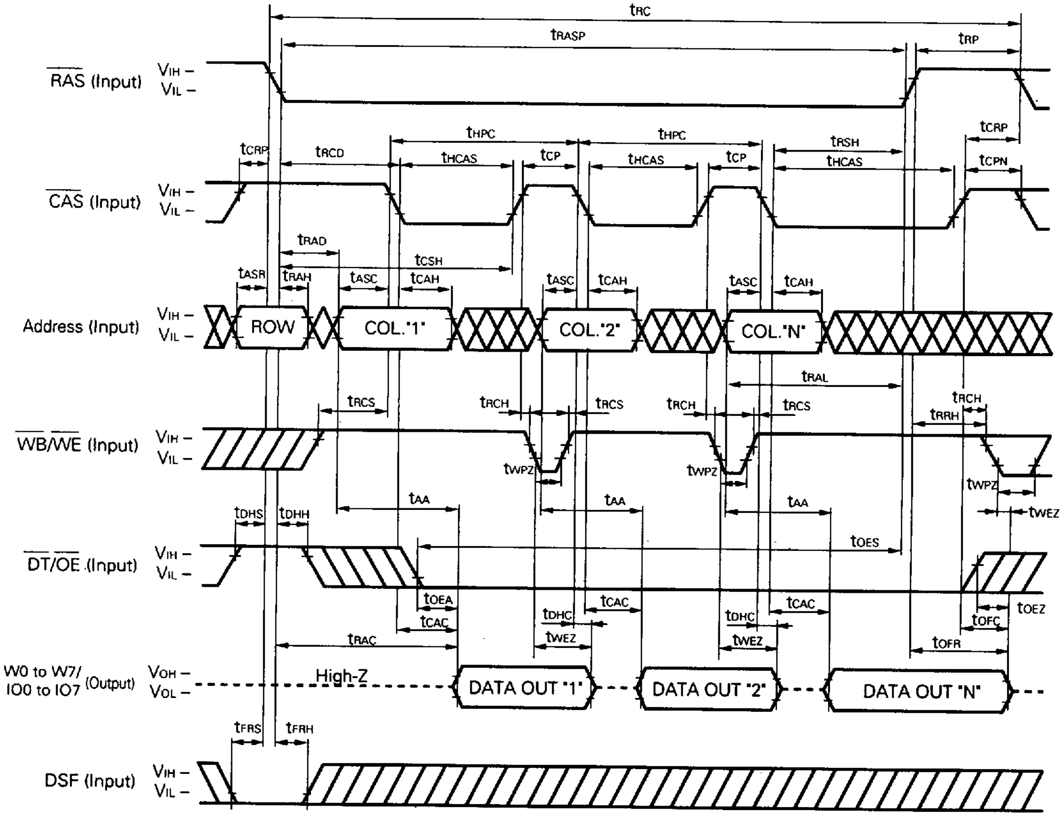
Remark Because the serial access port operates independently of the random access port, there is no need to control the SC, $\overline{\text{SE}}$, SIO pins in this cycle.

Hyper Page Mode Read Cycle (Extended data output: μPD482235)



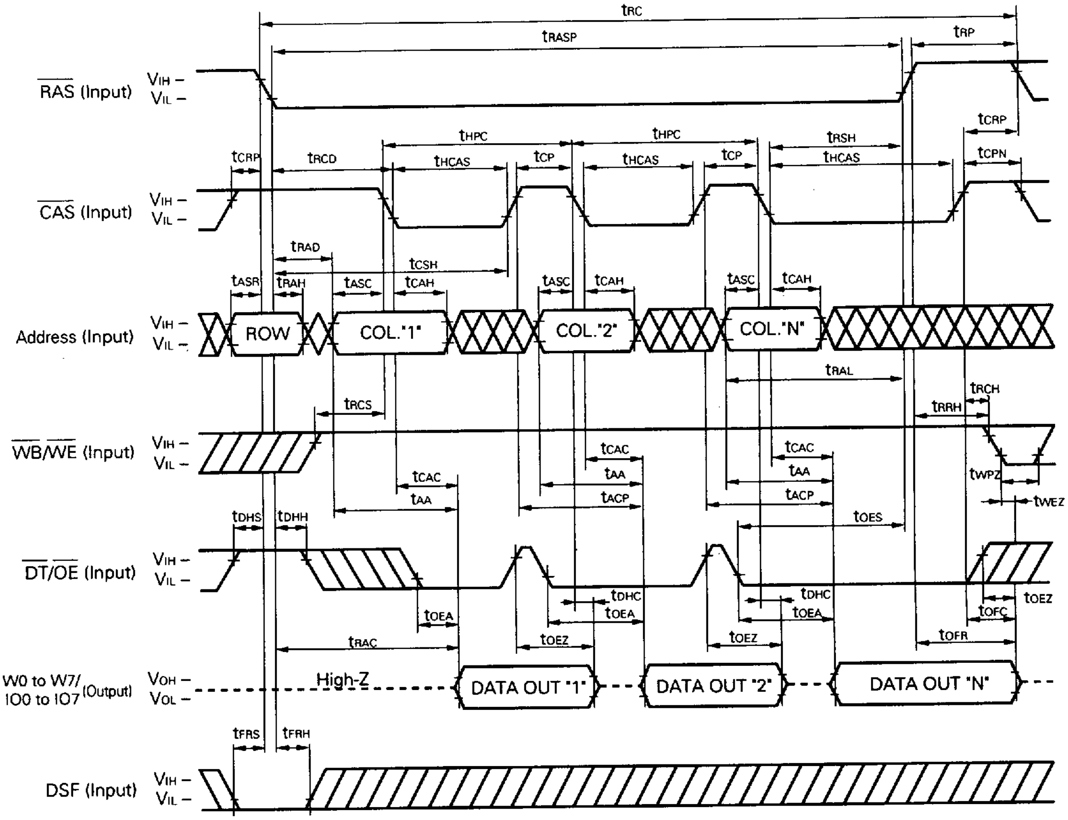
Remark Because the serial access port operates independently of the random access port, there is no need to control the SC, $\overline{\text{SE}}$, SIO pins in this cycle.

Hyper Page Mode Read Cycle ($\overline{\text{WE}}$ controlled)
(Extended data output: μPD482235 (Versions A, F and E))



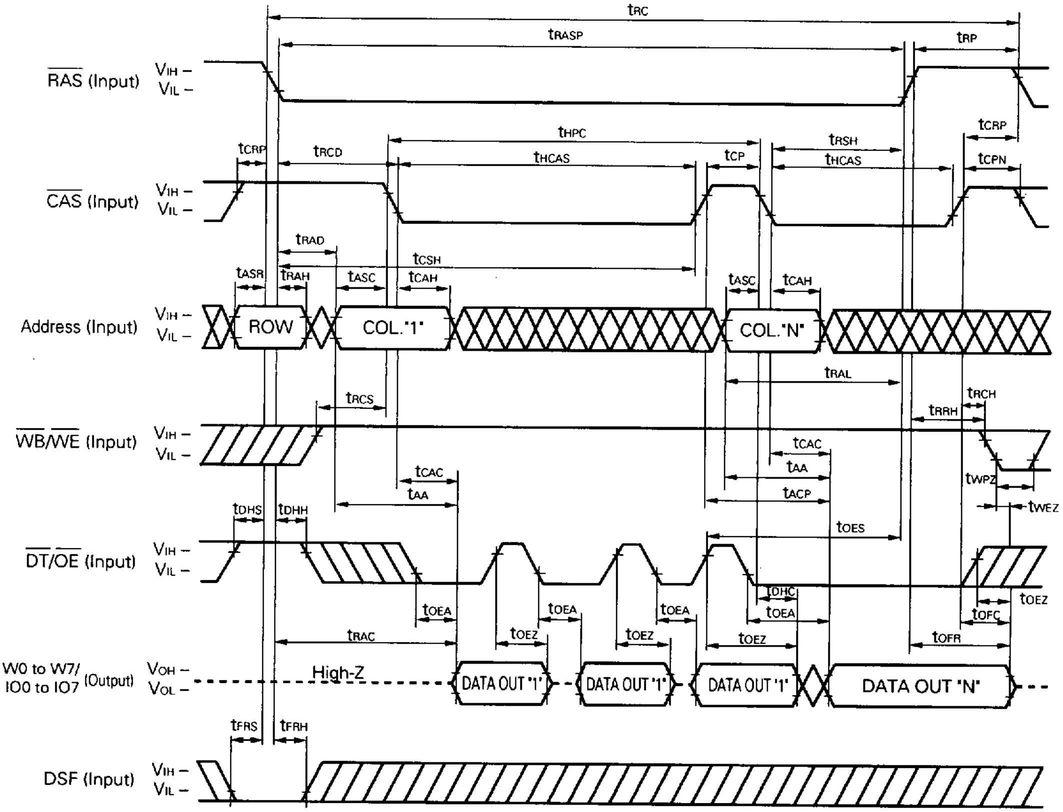
Remark Because the serial access port operates independently of the random access port, there is no need to control the SC, $\overline{\text{SE}}$, SIO pins in this cycle.

Hyper Page Mode Read Cycle ($\overline{OE}$ controlled: Latched control) (Extended data output: μPD482235 (Version A))



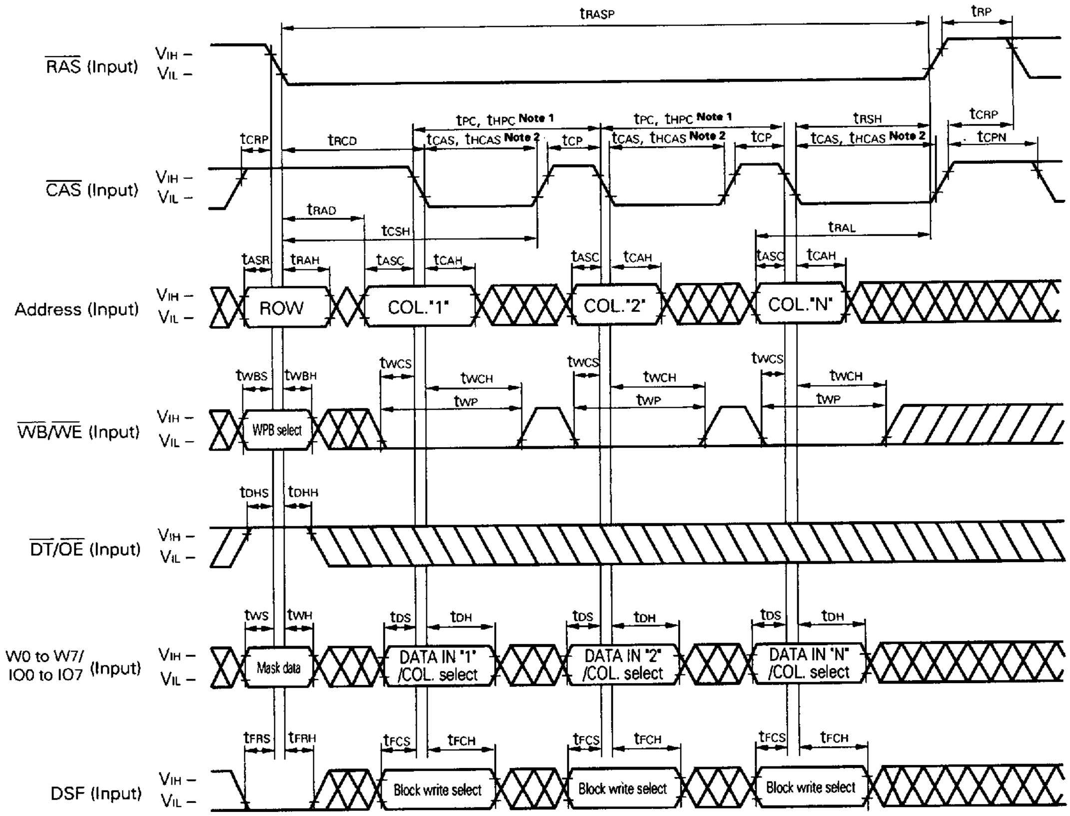
Remark Because the serial access port operates independently of the random access port, there is no need to control the SC, $\overline{SE}$, SIO pins in this cycle.

Hyper Page Mode Read Cycle ($\overline{OE}$ controlled: Non-Latched control) (Extended data output: μPD482235 (Versions F, E))



Remark Because the serial access port operates independently of the random access port, there is no need to control the SC, $\overline{SE}$, SIO pins in this cycle.

Fast Page, Hyper Page Mode Early Write Cycle/Fast Page, Hyper Page Mode Early Block Write Cycle



Notes 1. tPC for the μPD482234
tHPC for the μPD482235

2. tCAS for the μPD482234
tHCAS for the μPD482235

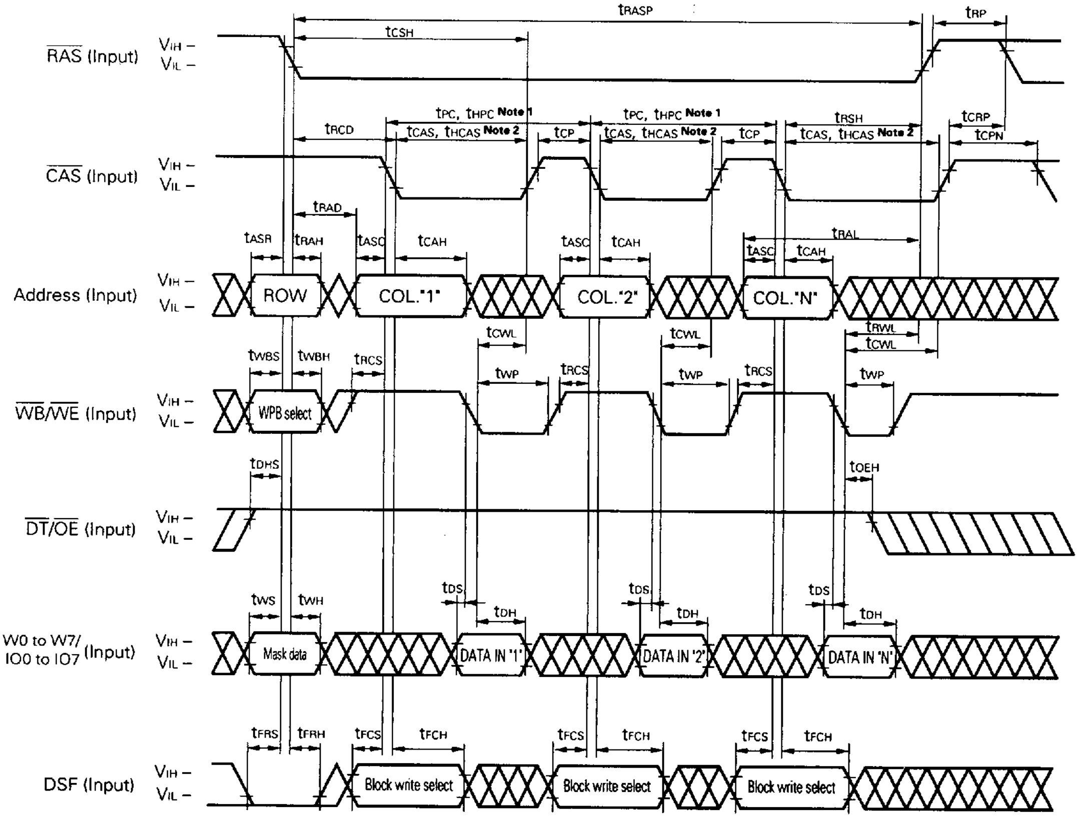
Remarks 1. When DSF is high level : Block write cycle
When DSF is low level : Write cycle

2. WPB : Write-per-bit

3. When block write cycle is selected, input the column selection data to DATA IN.

4. Because the serial access port operates independently of the random access port, there is no need to control the SC, SE, SIO pins in this cycle.

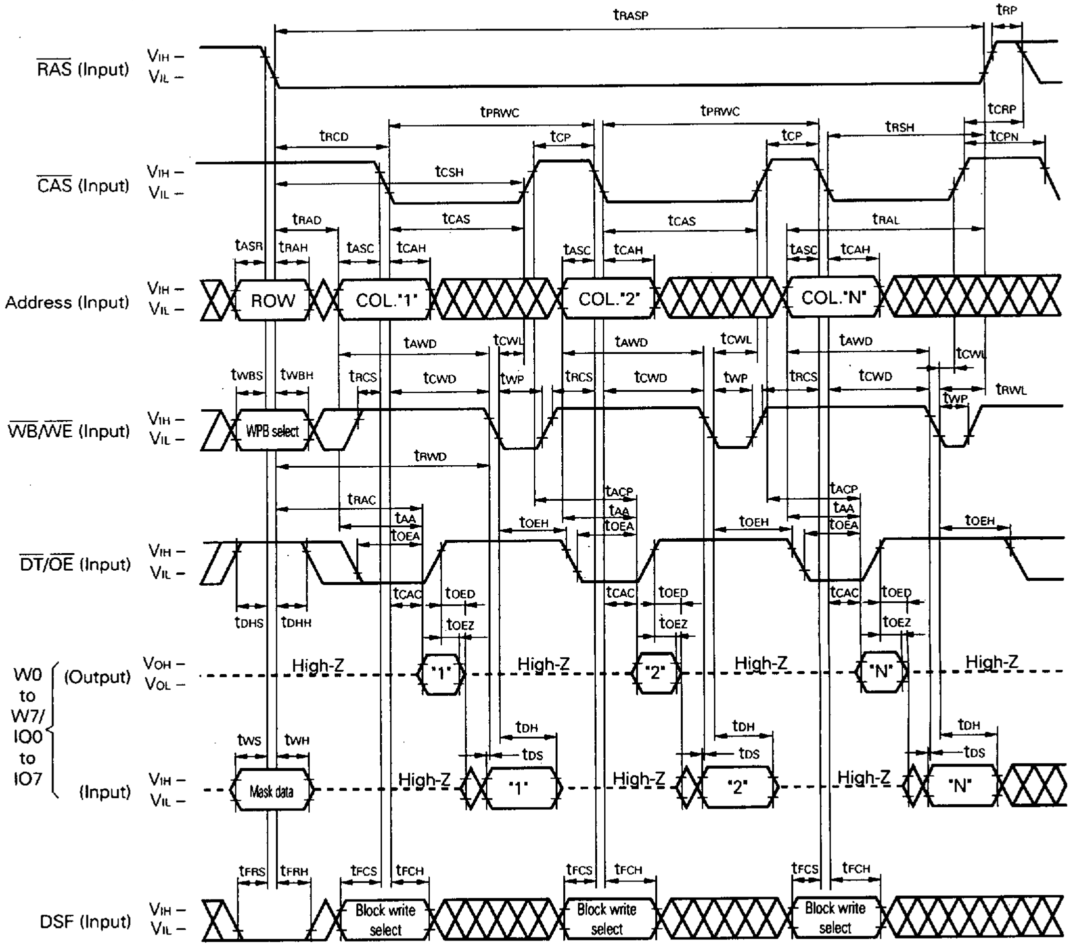
Fast Page, Hyper Page Mode Late Write Cycle/Fast Page, Hyper Page Mode Late Block Write Cycle



Notes 1. tPC for the μPD482234
tHPC for the μPD482235
2. tCAS for the μPD482234
tHCAS for the μPD482235

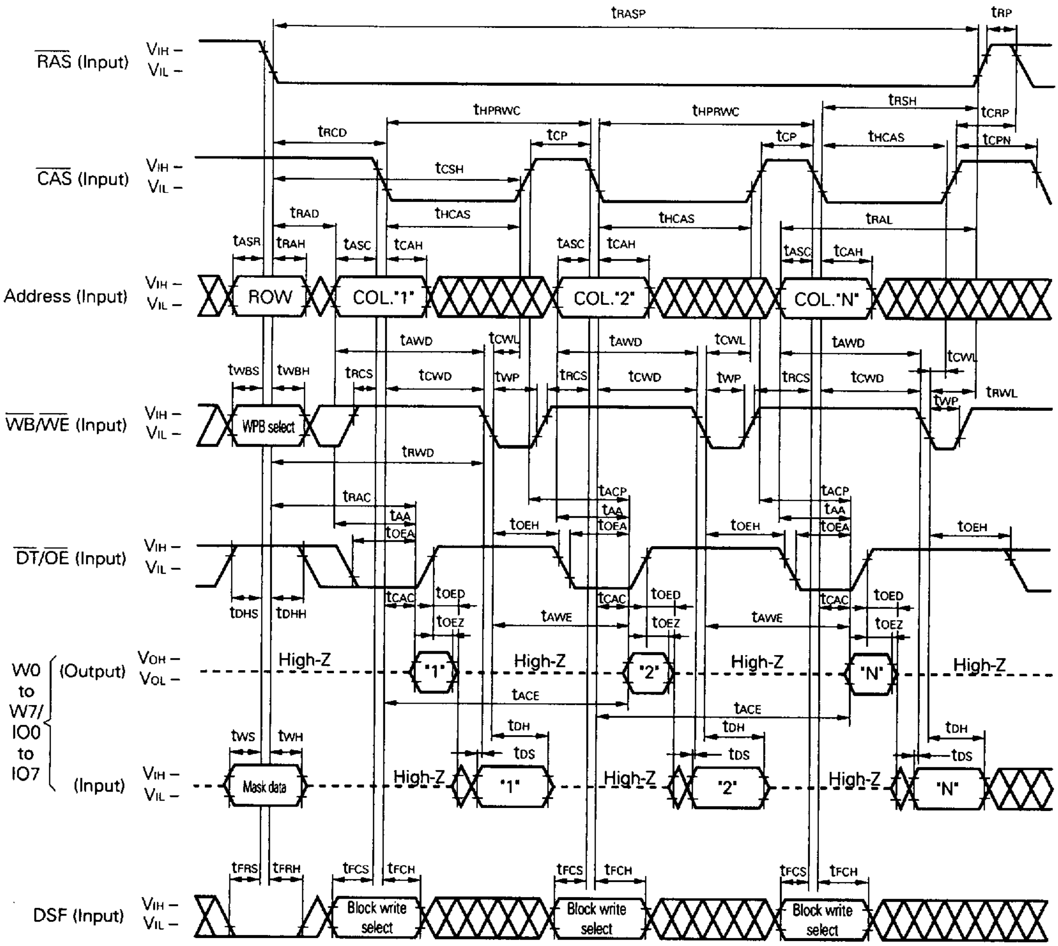
Remarks 1. When DSF is high level : Block write cycle
When DSF is low level : Write cycle
2. WPB : Write-per-bit
3. When block write cycle is selected, input the column selection data to DATA IN.
4. Because the serial access port operates independently of the random access port, there is no need to control the SC, SE, SIO pins in this cycle.

Fast Page Mode Read Modify Write Cycle (μPD482234)/
Fast Page Mode Read Modify Block Write Cycle (μPD482234)



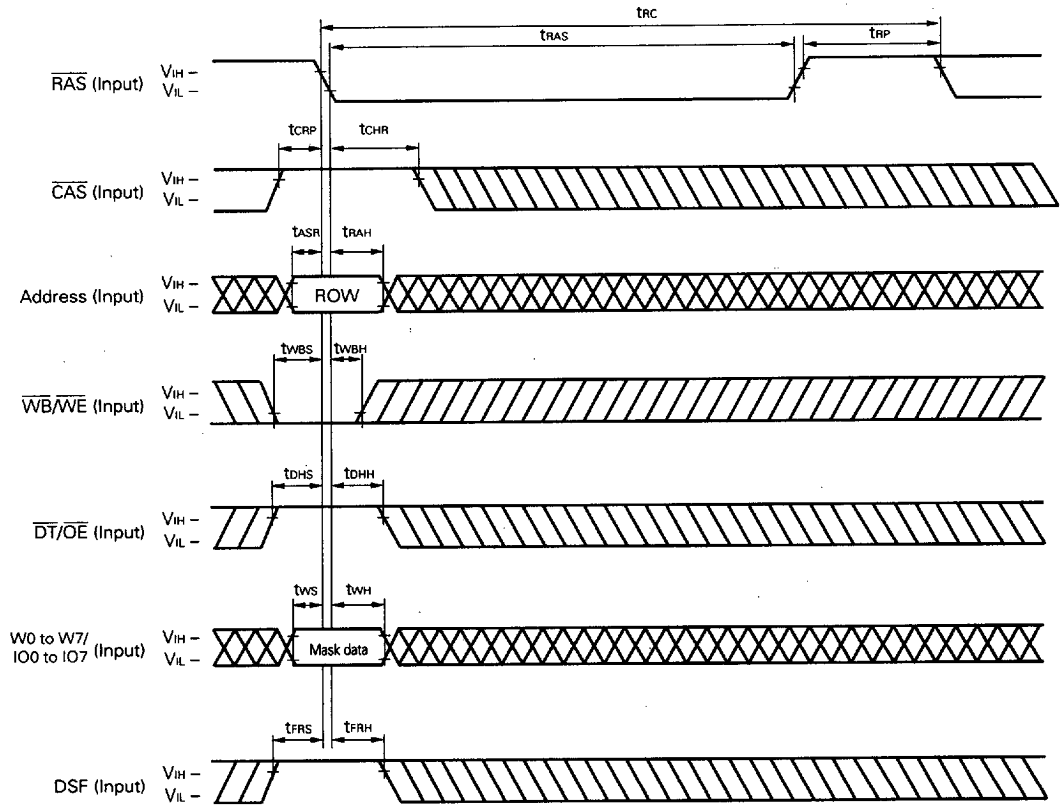
Remarks
1. When DSF is high level : Block write cycle
   When DSF is low level : Write cycle
2. WPB : Write-per-bit
3. When block write cycle is selected, input the column selection data to DATA IN.
4. Because the serial access port operates independently of the random access port, there is no need to control the SC, SE, SIO pins in this cycle.

Hyper Page Mode Read Modify Write Cycle (Extended data output: μPD482235)/ Hyper Page Mode Read Modify Block Write Cycle (Extended data output: μPD482235)



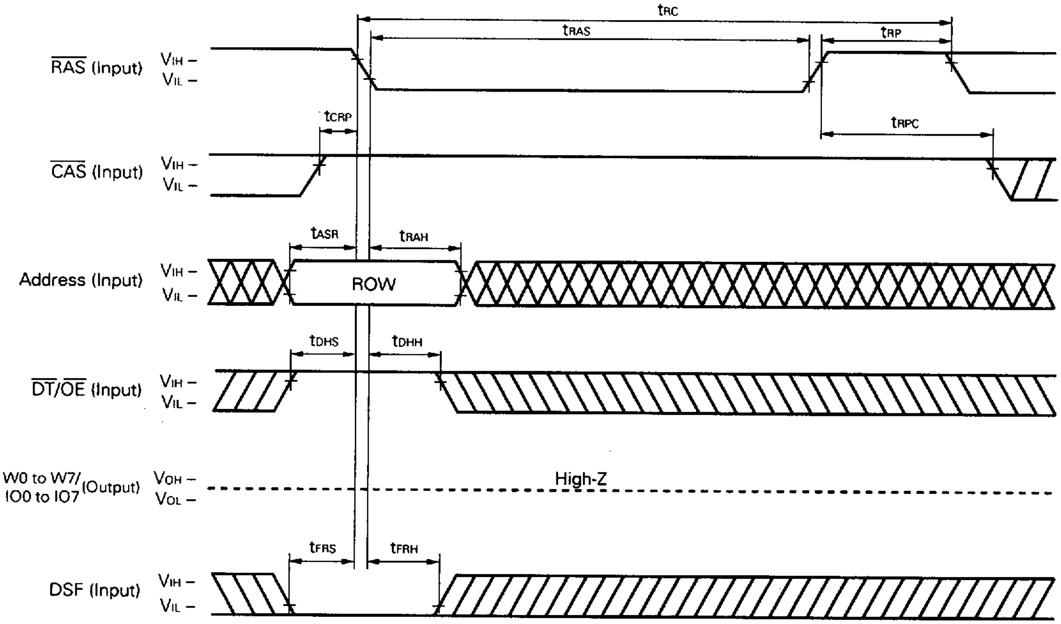
Remarks 1. When DSF is high level : Block write cycle
When DSF is low level : Write cycle
2. WPB : Write-per-bit
3. When block write cycle is selected, input the column selection data to DATA IN.
4. Because the serial access port operates independently of the random access port, there is no need to control the SC, $\overline{\text{SE}}$, SIO pins in this cycle.

Flash Write Cycle



Remark Because the serial access port operates independently of the random access port, there is no need to control the SC, $\overline{SE}$, SIO pins in this cycle.

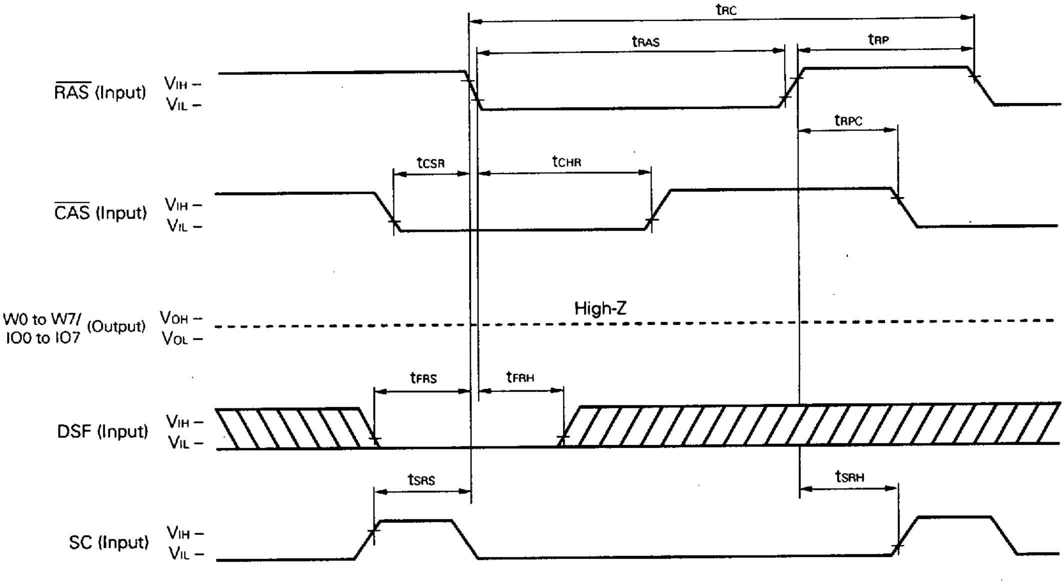
$\overline{\text{RAS}}$ Only Refresh Cycle



Remarks 1. $\overline{\text{WB}}/\overline{\text{WE}}$: Don't care

2. Because the serial access port operates independently of the random access port, there is no need to control the SC, $\overline{\text{SE}}$, SIO pins in this cycle.

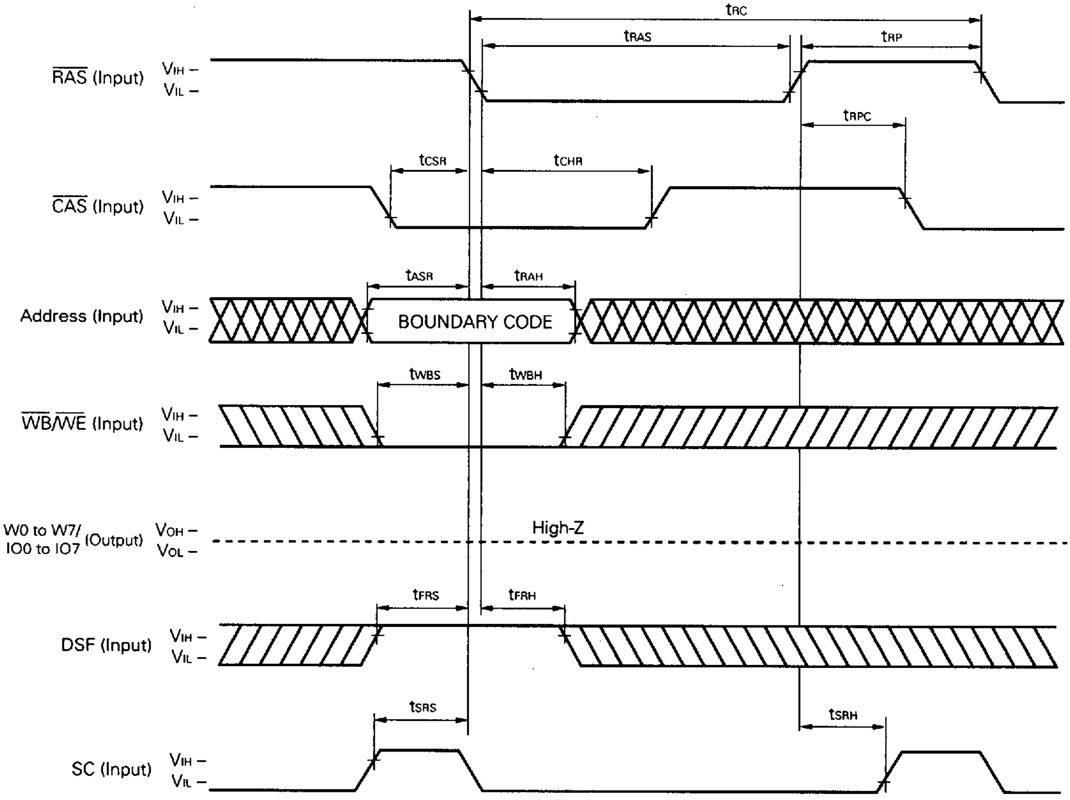
CAS Before RAS Refresh Cycle (Optional Reset)



Remarks 1. Address, WB/WE, DT/OE : Don't care

2. Because the serial access port operates independently of the random access port, there is no need to control the SE, SIO pins in this cycle.

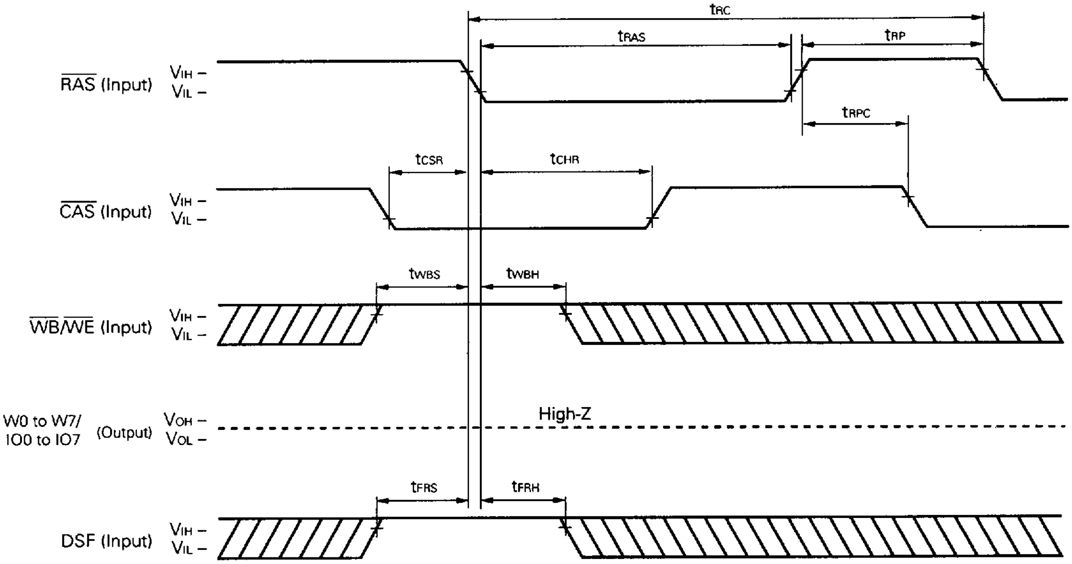
CAS Before RAS Refresh Cycle (STOP Register Set)



Remarks 1. $\overline{\text{DT}}/\overline{\text{OE}}$: Don't care

2. Because the serial access port operates independently of the random access port, there is no need to control the $\overline{\text{SE}}$, SIO pins in this cycle.

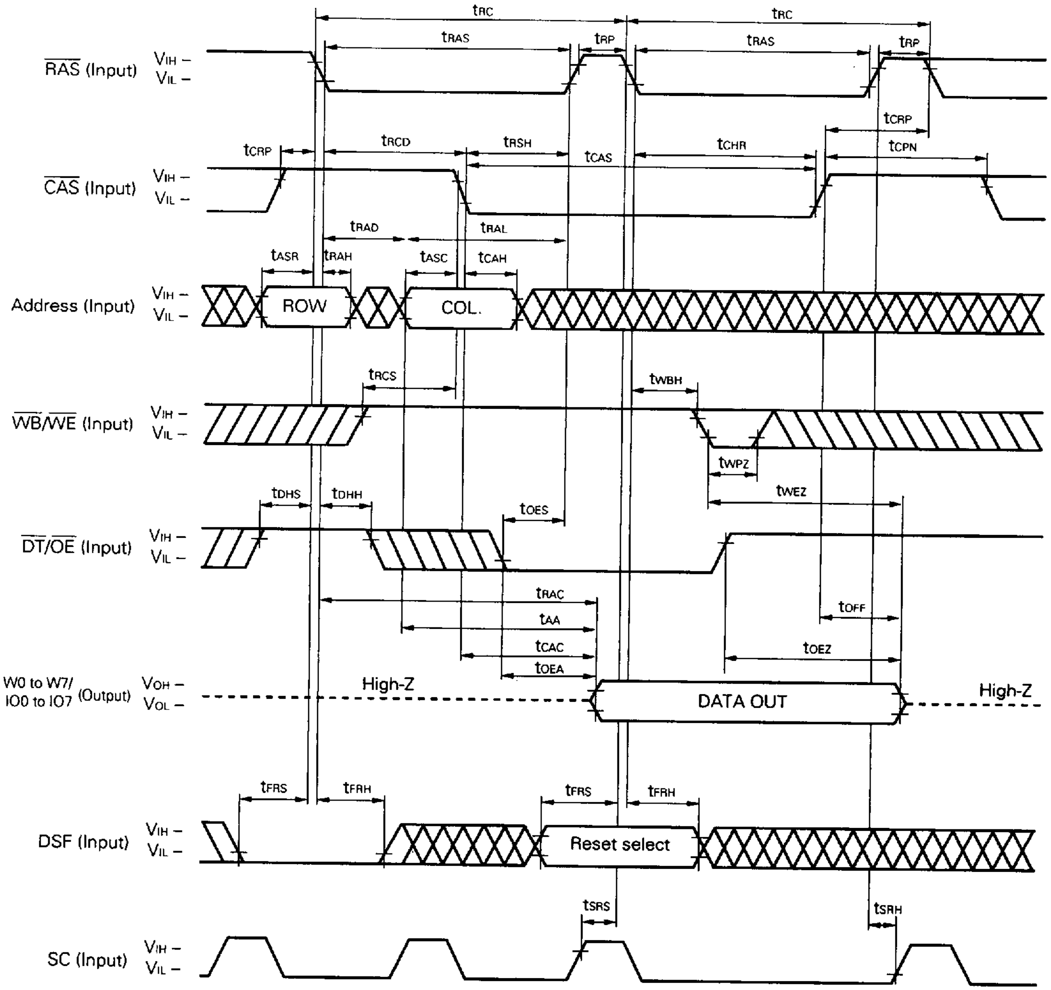
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle (No Reset)



Remarks 1. Address, $\overline{\text{DT}}/\overline{\text{OE}}$: Don't care

2. Because the serial access port operates independently of the random access port, there is no need to control the SC, $\overline{\text{SE}}$, SIO pins in this cycle.

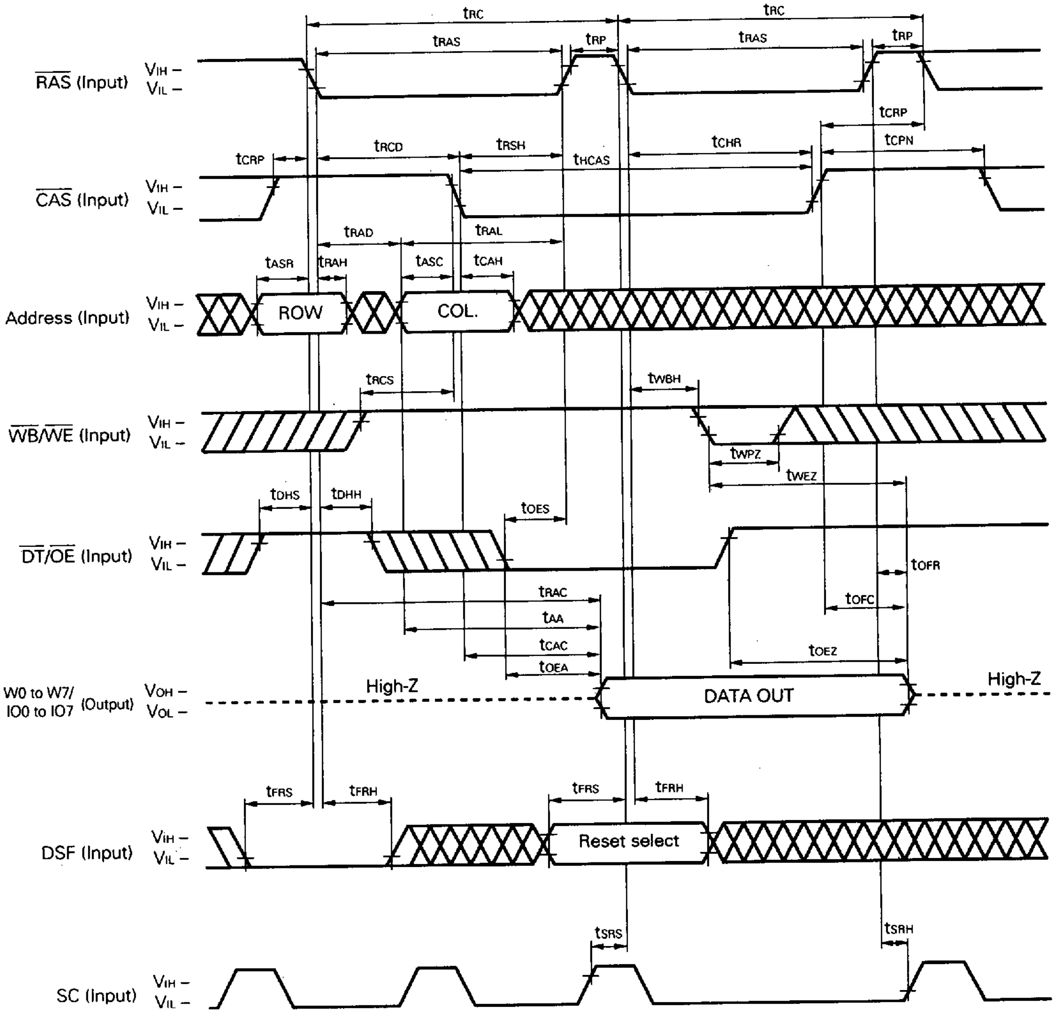
Hidden Refresh Cycle (μPD482234)



Remarks 1. When DSF is high level : Reset select = No Reset
When DSF is low level : Reset select = Optional Reset

2. Because the serial access port operates independently of the random access port, there is no need to control the $\overline{\text{SE}}$, SIO pins in this cycle.

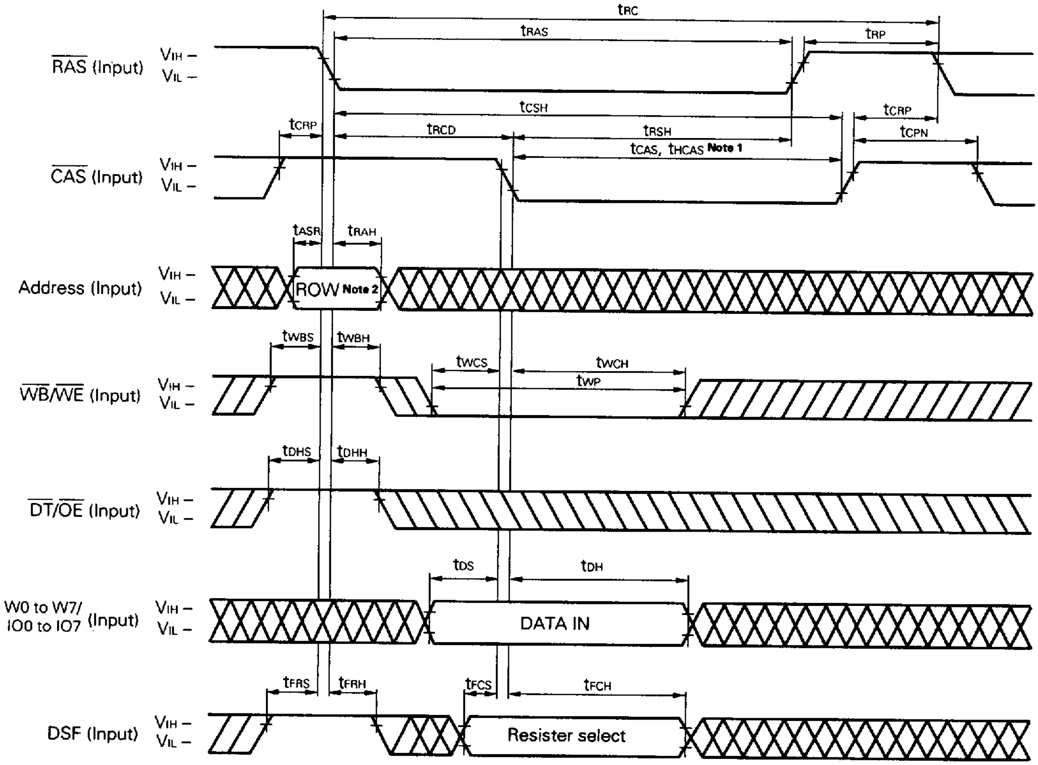
Hidden Refresh Cycle (Extended data output: μPD482235)



Remarks 1. When DSF is high level : Reset select = No Reset
When DSF is low level : Reset select = Optional Reset

2. Because the serial access port operates independently of the random access port, there is no need to control the SE, SIO pins in this cycle.

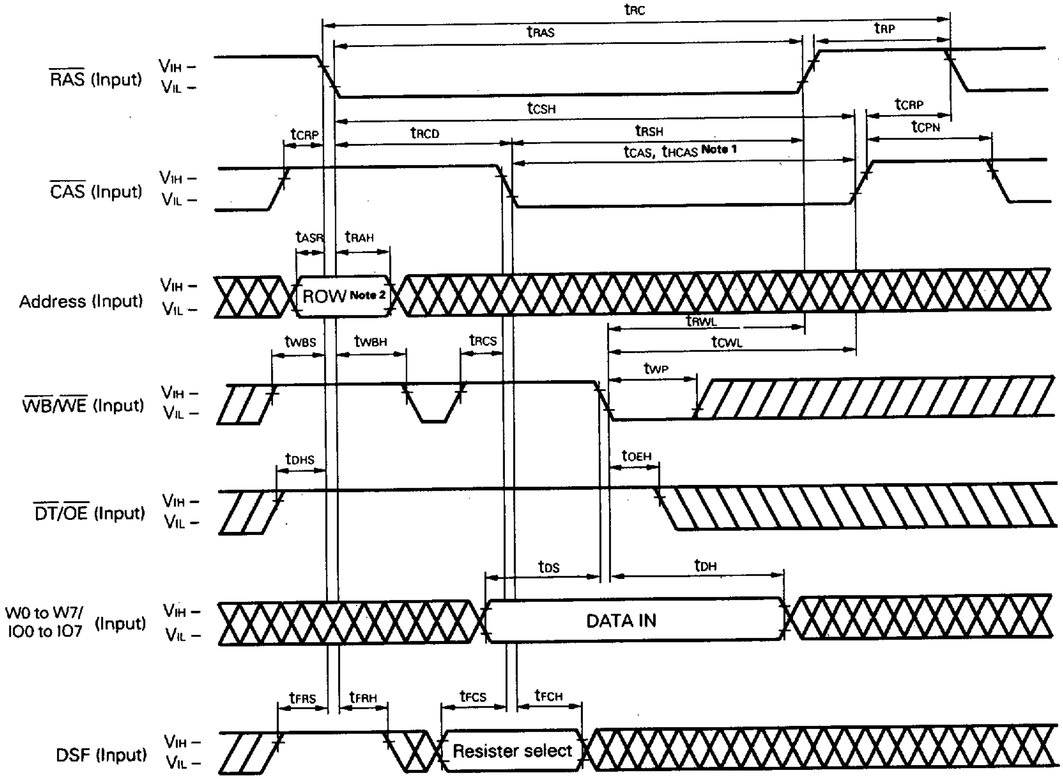
Register Set Cycle (Early Write)



Notes 1. tCAS for the μPD482234
tHCAS for the μPD482235
2. Refresh address (RAS only refresh)

Remarks 1. When DSF is high level : Register select = Color Register Select
When DSF is low level : Register select = Write Mask Register Select
2. Because the serial access port operates independently of the random access port, there is no need to control the SC, SE, SIO pins in this cycle.

Register Set Cycle (Late Write)



Notes 1. t_{CAS} for the μPD482234

t_{HCAS} for the μPD482235

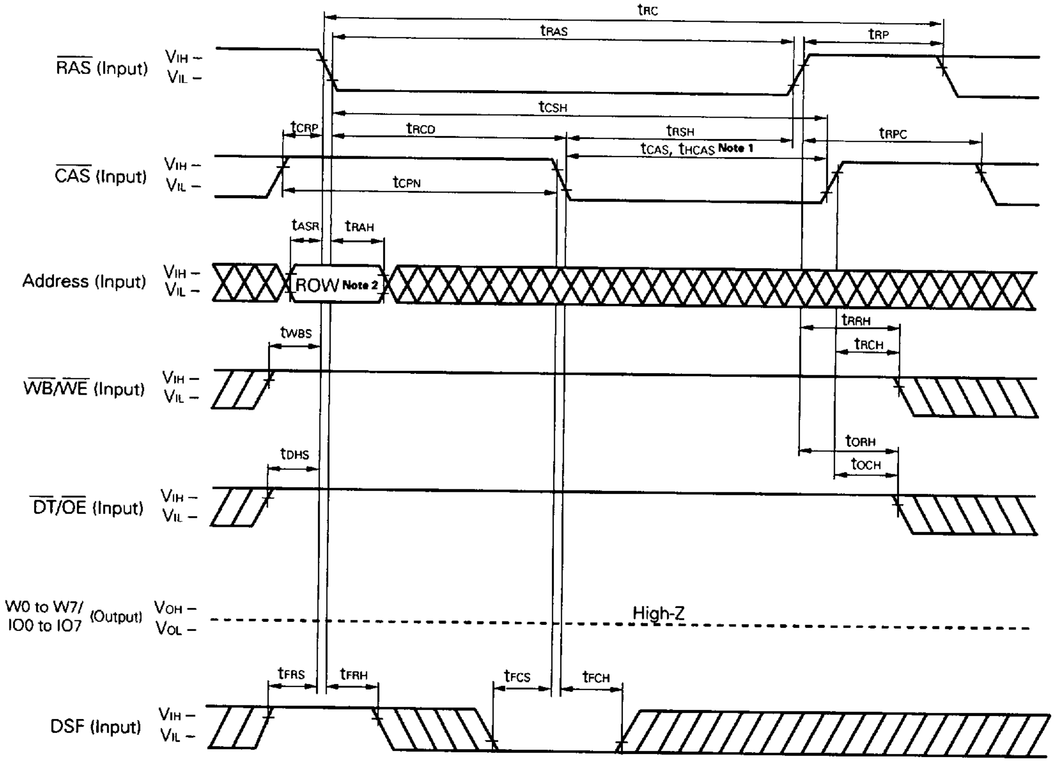
2. Refresh address ($\overline{RAS}$ only refresh)

Remarks 1. When DSF is high level : Register select = Color Register Select

When DSF is low level : Register select = Write Mask Register Select

2. Because the serial access port operates independently of the random access port, there is no need to control the SC, $\overline{SE}$, SIO pins in this cycle.

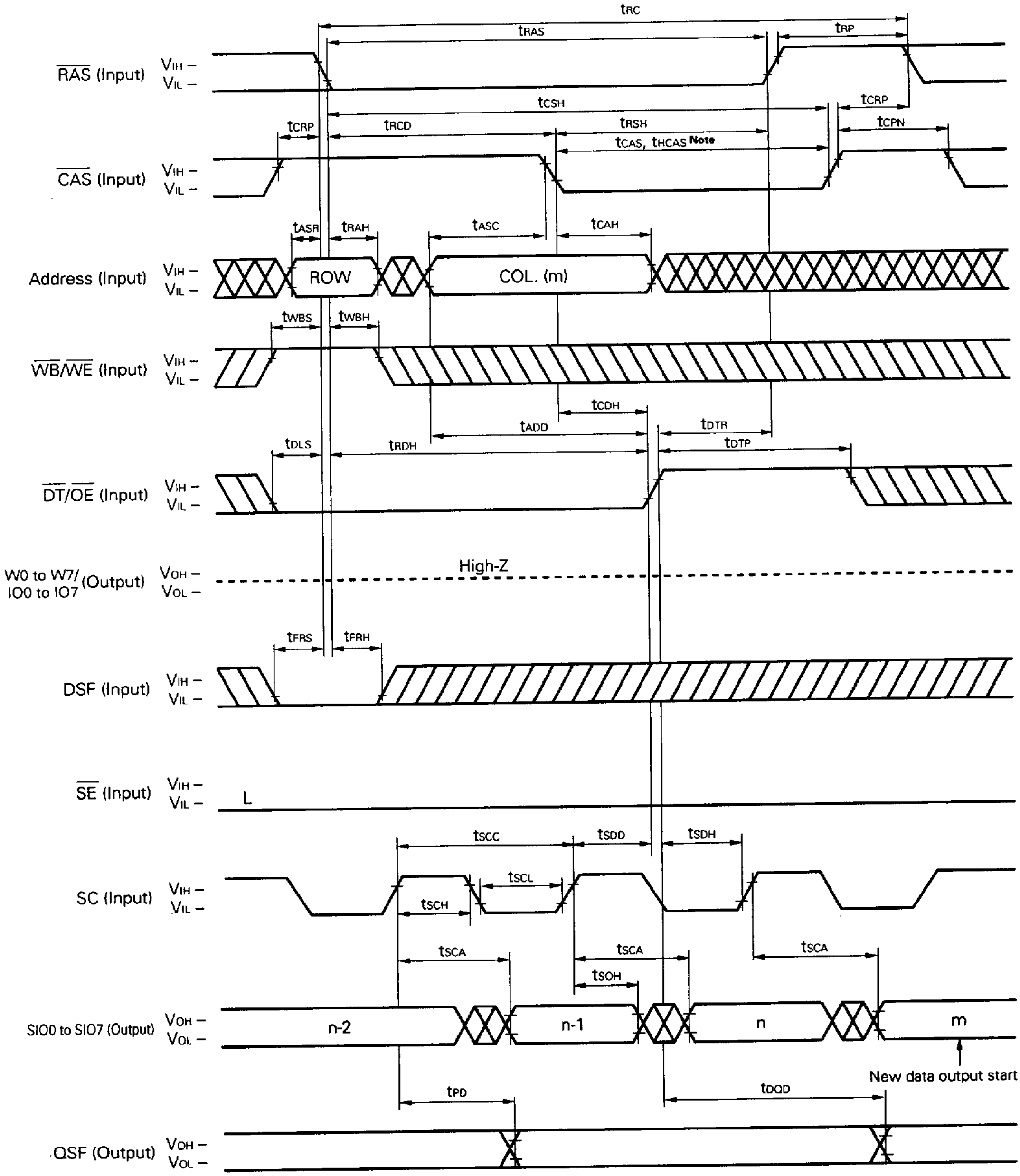
Mask Register Set Cycle (New Mask Selection) (Versions F and E only)



Notes 1. tCAS for the μPD482234
tHCAS for the μPD482235
2. Refresh address ($\overline{\text{RAS}}$ only refresh)

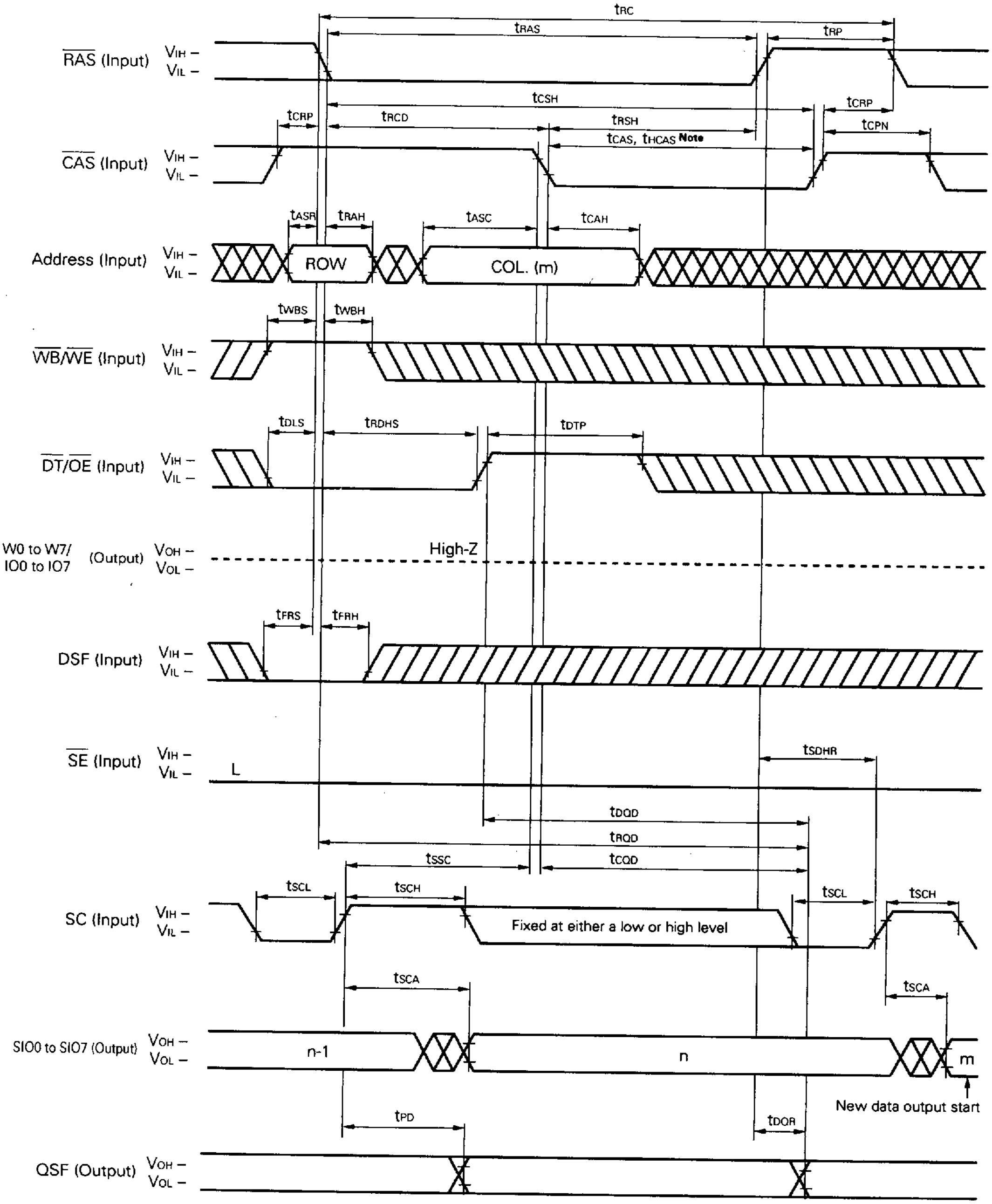
Remark Because the serial access port operates independently of the random access port, there is no need to control the SC, $\overline{\text{SE}}$, SIO pins in this cycle.

Read Data Transfer Cycle (SC Active)



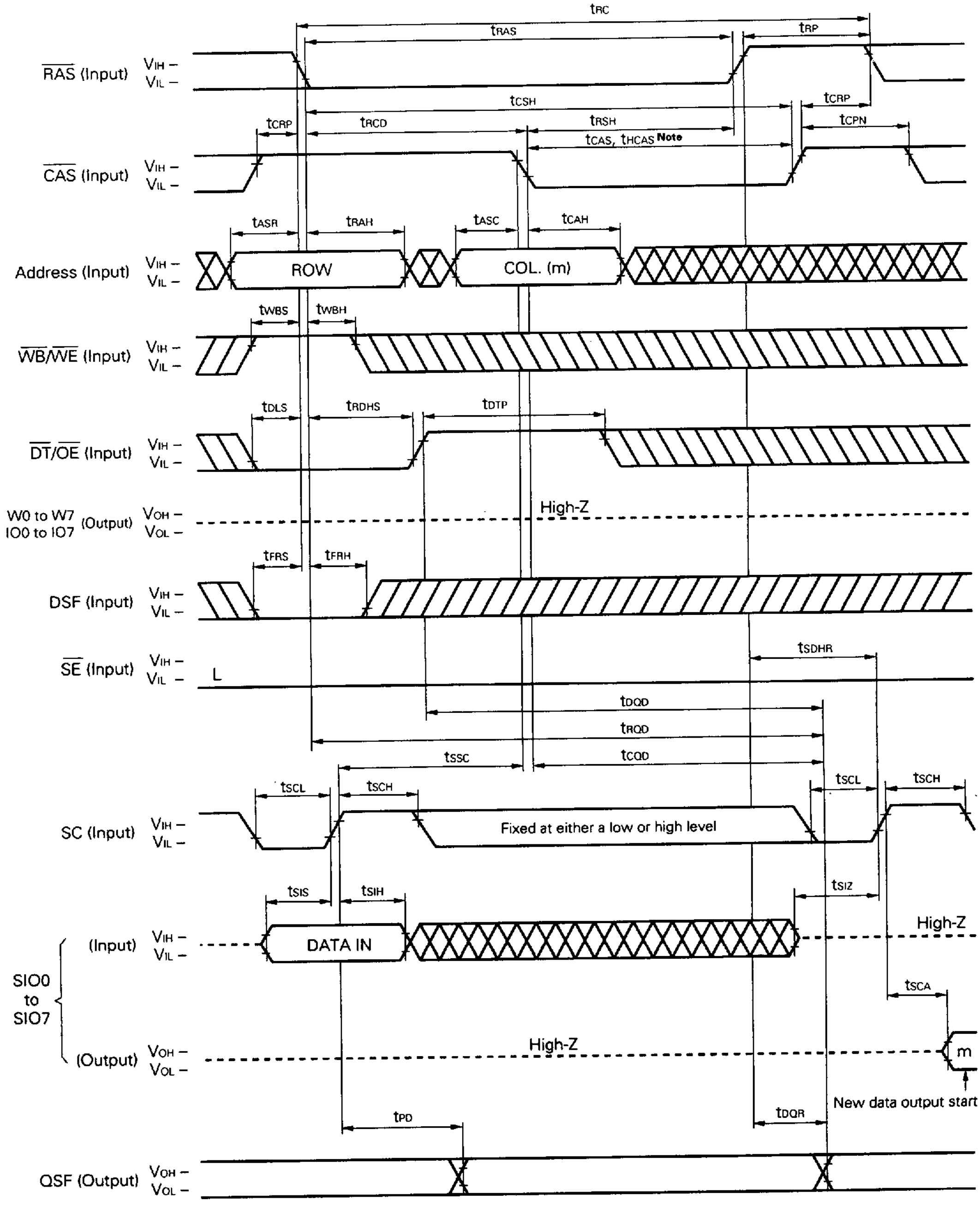
Note t_{CAS} for the μPD482234
t_{HCAS} for the μPD482235

Read Data Transfer Cycle (SC Inactive)



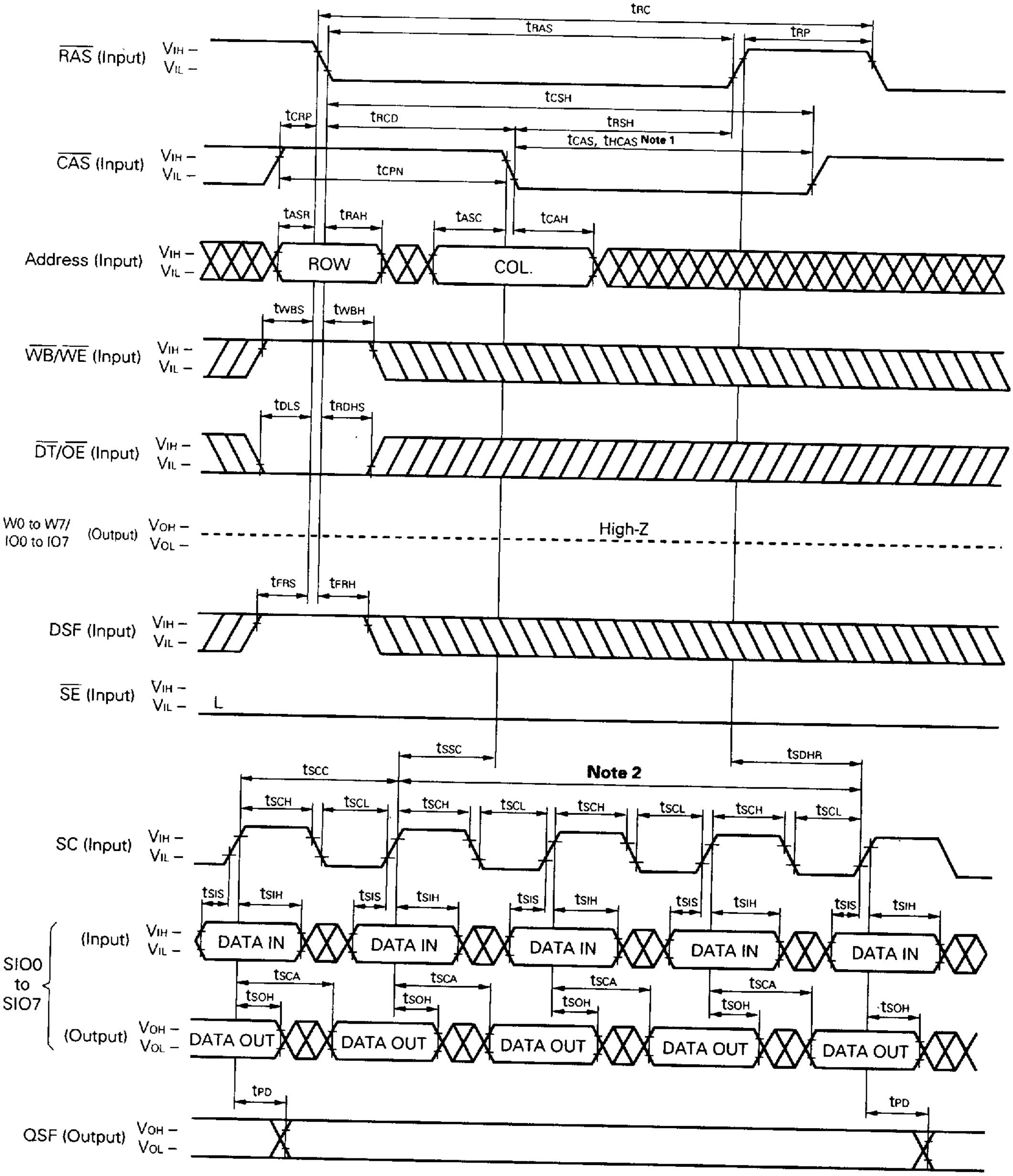
Note tCAS for the μPD482234
tHCAS for the μPD482235

Read Data Transfer Cycle (Serial Write → Serial Read Switching)



Note t_{CAS} for the μPD482234
t_{HCAS} for the μPD482235

Split Read Data Transfer Cycle

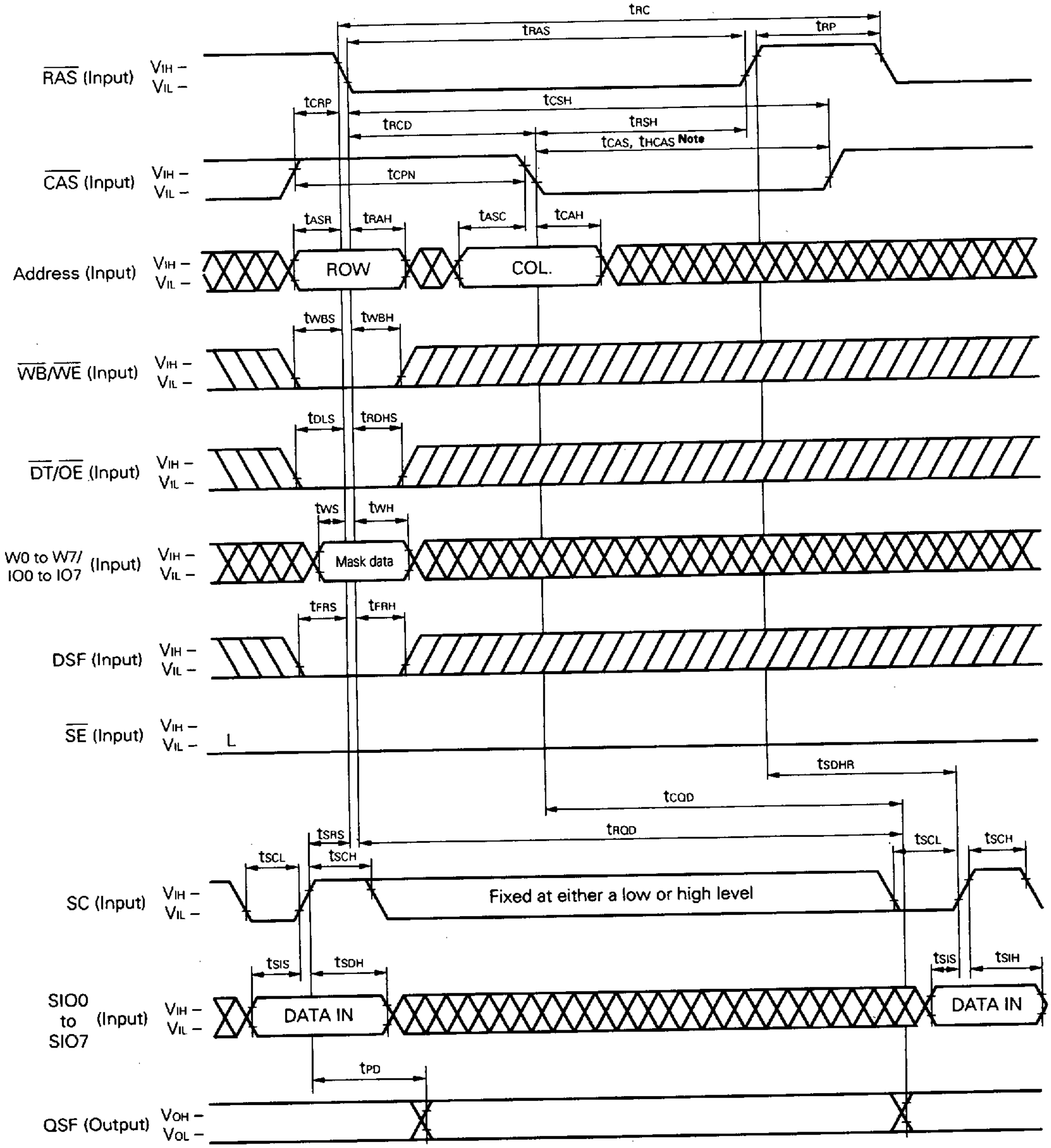


Notes 1. tCAS for the μPD482234

tHCAS for the μPD482235

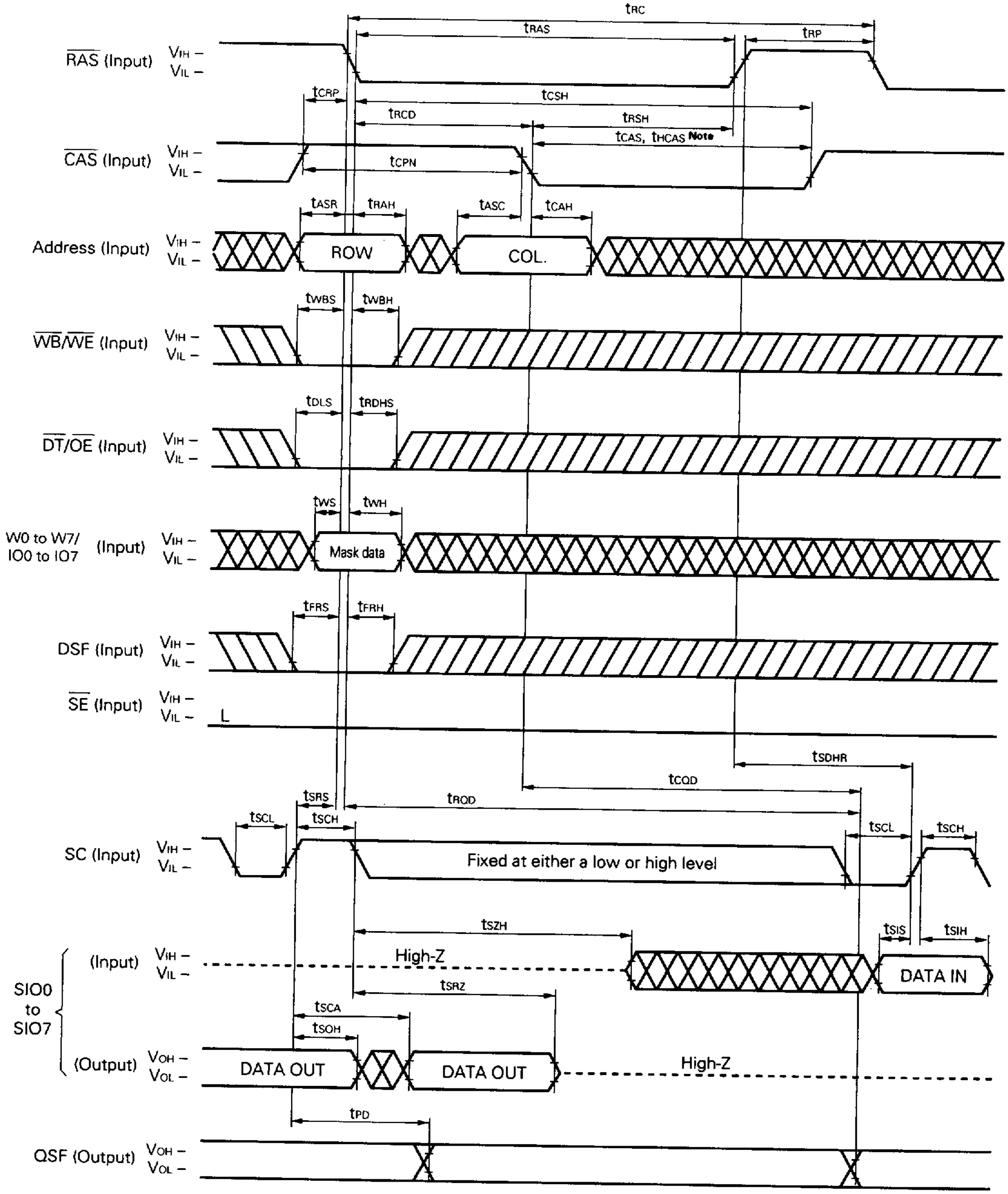
2. Do not perform the following two serial read/write during this period.
   - Serial read/write of jump source address set to the STOP register of the data register which does not perform the data transfer cycle.
   - Serial read/write of last address of data register (Address 255 or 511)
   - Data register serial read for the side to be involved in data transfer cycle (for version E only)

Write Data Transfer Cycle



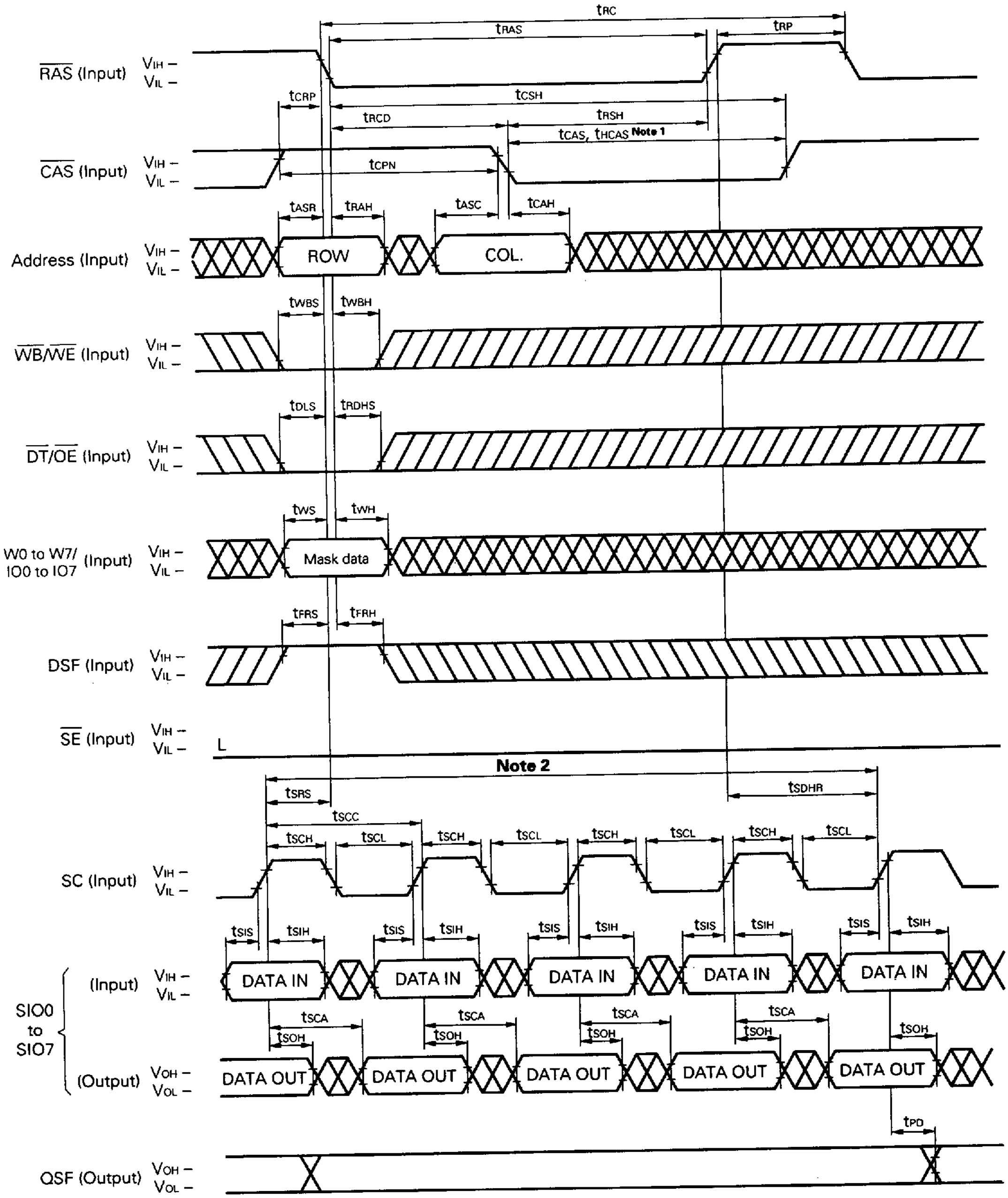
Note tCAS for the μPD482234
tHCAS for the μPD482235

Write Data Transfer Cycle (Serial Read → Serial Write Switching)



Note tCAS for the μPD482234
tHCAS for the μPD482235

Split Write Data Transfer Cycle

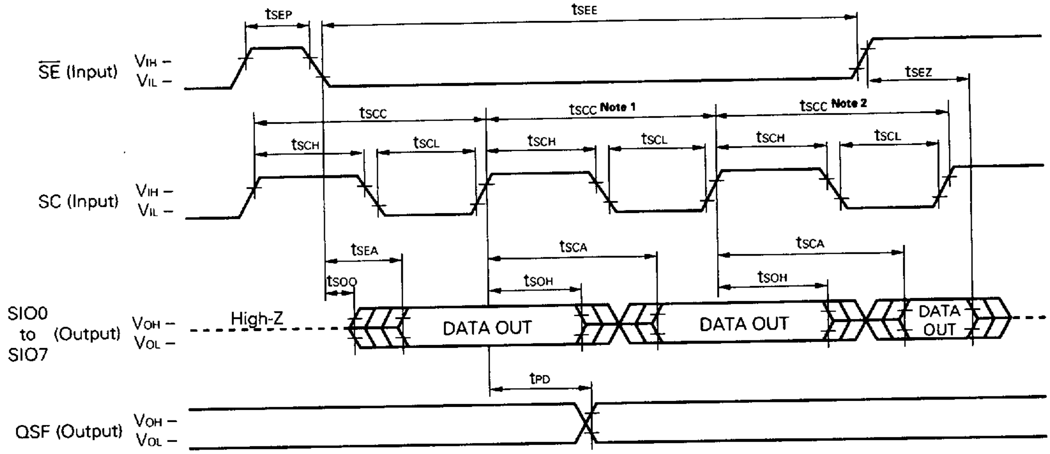


Notes 1. t_{CAS} for the μPD482234

t_{HCAS} for the μPD482235

2. Do not perform the following two serial read/write during this period.
    - Serial read/write of jump source address set to the STOP register of the data register which does not perform the data transfer cycle.
    - Serial read/write of last address of data register (Address 255 or 511)
    - Data register serial read for the side to be involved in data transfer cycle (for version E only)

Serial Read Cycle

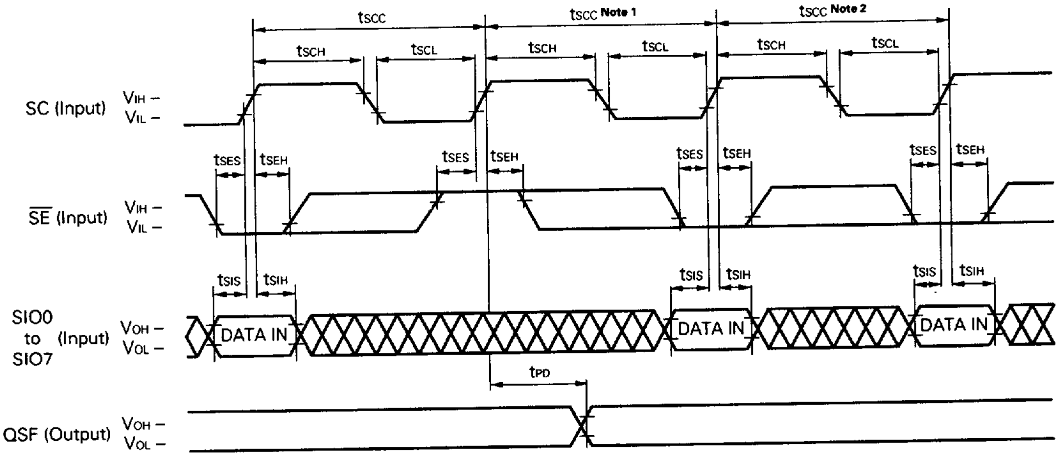


Notes 1. Last address of data register (Address 255 or 511)

2. Starting address of data register newly read (address is specified in the data transfer cycle).

Remark Because the random access port operates independently of the serial access port, there is no need to control the $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address, $\overline{\text{WB}}/\overline{\text{WE}}$, $\overline{\text{DT}}/\overline{\text{OE}}$, WI/O, DSF pins in this cycle.

Serial Write Cycle



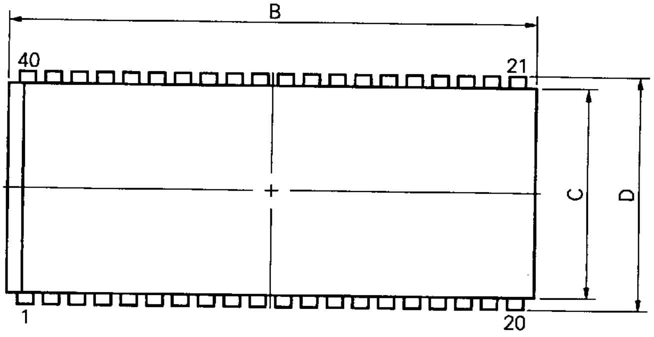
Notes 1. Last address of data register (Address 255 or 511)

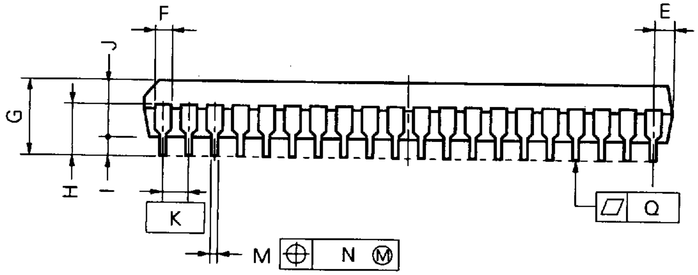
2. Starting address of data register newly read (address is specified in the data transfer cycle).

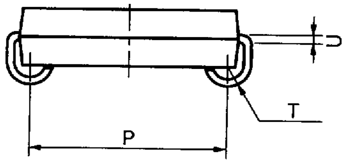
Remark Because the random access port operates independently of the serial access port, there is no need to control the $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address, $\overline{\text{WB}}/\overline{\text{WE}}$, $\overline{\text{DT}}/\overline{\text{OE}}$, WI/O, DSF pins in this cycle.

5. Package Drawings

40 PIN PLASTIC SOJ (400 mil)





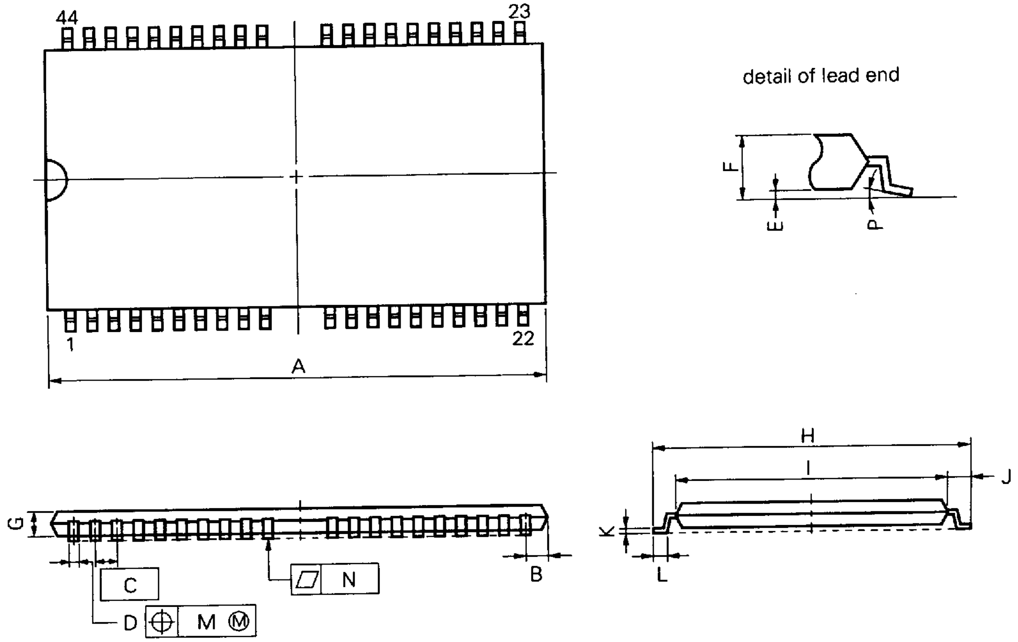


NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$26.29^{+0.2}_{-0.35}$	$1.035^{+0.008}_{-0.014}$
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.7	0.028
G	3.5±0.2	0.138±0.008
H	2.4±0.2	$0.094^{+0.009}_{-0.008}$
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.40±0.20	0.370±0.008
Q	0.15	0.006
T	R0.85	R0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

P40LE-400A-2

44 PIN PLASTIC TSOP(II) (400 mil)



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	0.93 MAX.	0.037 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

S44G5-80-7JF4

6. Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD482234, μPD482235.

Types of Surface Mount Device

μPD482234LE-xx : 40-pin plastic SOJ (400 mil)
μPD482235LE-xx : 40-pin plastic SOJ (400 mil)

μPD482234G5-xx : 44-pin plastic TSOP (II) (400 mil)
μPD482235G5-xx : 44-pin plastic TSOP (II) (400 mil)

7. Example of Stamping

Letter A in the fifth character position in a lot number signifies version A, letter F, version F, and letter E, version E.