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**MSC1200-xx/1200V-xx**

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**30-Bit Duplex Controller/Driver with Digital/Analog Dimming and Keyscan Functions**

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**GENERAL DESCRIPTION**

The MSC1200-xx/1200V-xx is a Bi-CMOS display driver for 1/2-duty vacuum fluorescent display tube. This device consists of a 64-bit shift register, latches, an analog dimming circuit, a digital dimming circuit, a keyscan circuit, and drivers.

The interface with a microcomputer can be done only with four signal lines (CS, DATA I/O, CLOCK, and INT). Also, the DATA I/O and CLOCK signal lines can be shared with other peripherals by using the chip select function.

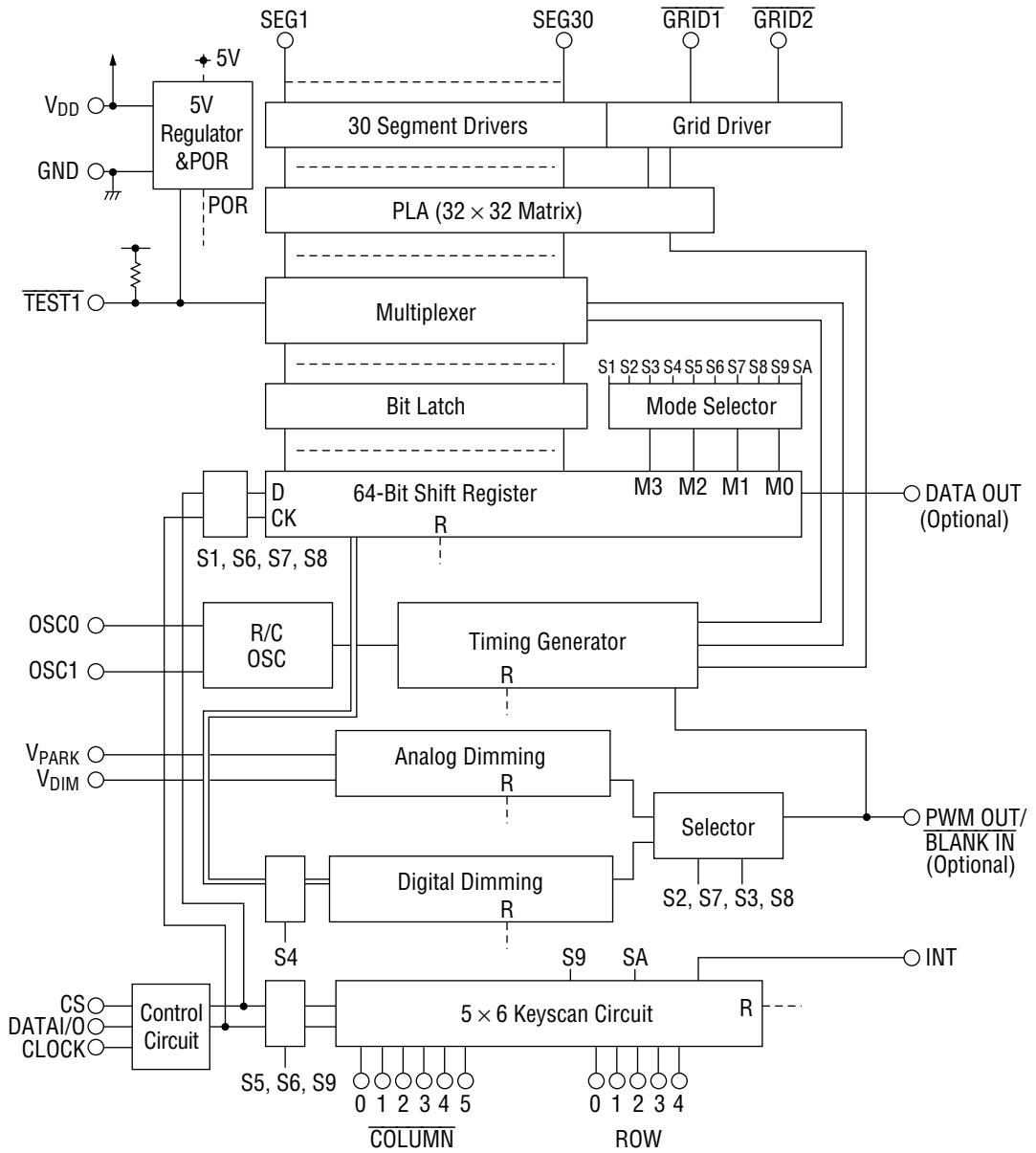
Also available is the MSC1200-01/1200V-01, a model with the general purpose code "-01".

Products with custom code are manufactured according to customer orders.

**FEATURES**

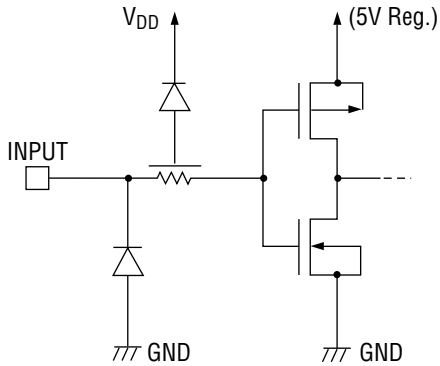
- Power supply voltage : 8V to 18V (built-in 5V regulator for logic)
- Operating temperature range :  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- 30-segment driver outputs ( $I_{OH} = -6\text{mA}$  at  $V_{OH} = V_{DD} - 0.8\text{V}$ )
- Built-in analog dimming circuit (PWM: 12.5% Max at 6-bit resolution)
- Built-in digital dimming circuit (11-bit resolution)
- Built-in 5 x 6 keyscan circuit
- Built-in RC oscillation circuit (external R and C)
- Built-in power-on-reset circuit.
- Shift register outputs and segment outputs can be set arbitrary.  
(32 x 32-bit PLA that is programmable by mask option is built in)
- The product name differs depending on the bonding option pin selected:  
PWM OUT/ $\overline{\text{BLANK IN}}$  : MSC1200-xx  
DATA OUT : MSC1200V-xx
- Package :  
56-pin plastic QFP (QFP56-P-910-0.65-2K) (Product name: MSC1200-xxGS-2K/MS1200V-xxGS-2K)  
xx indicates the code number.

**BLOCK DIAGRAM**

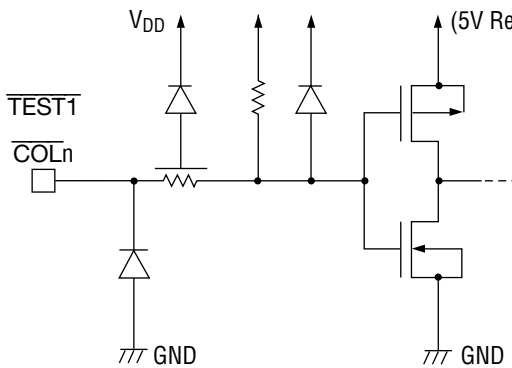


### INPUT AND OUTPUT CONFIGURATION

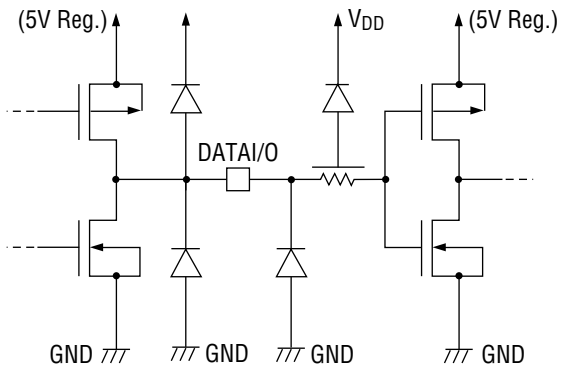
- Schematic Diagrams of Logic Portion Input Circuit



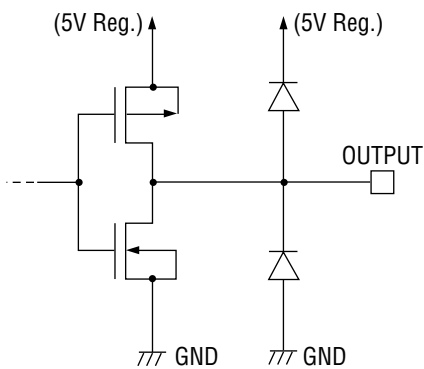
- Schematic Diagrams of Logic Portion Input Circuit 2



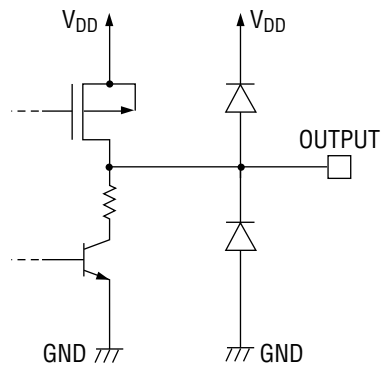
- Schematic Diagrams of Logic Portion Input/Output Circuit



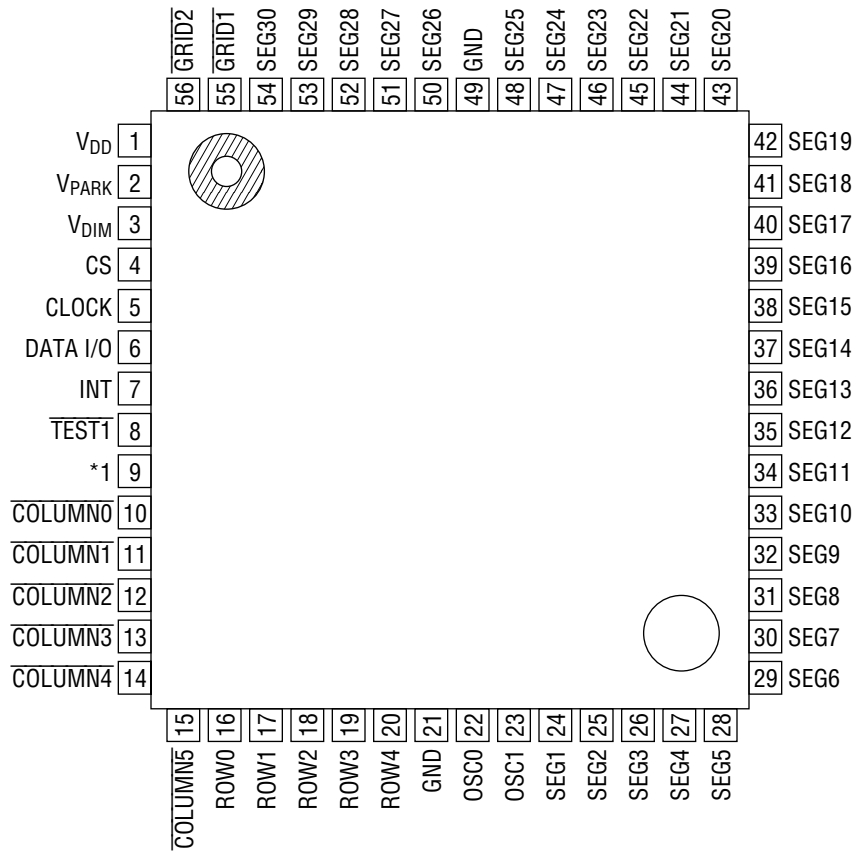
- Schematic Diagrams of Logic Portion Output Circuit



- Schematic Diagrams of Driver Output Circuit



**PIN CONFIGURATION (TOP VIEW)**



**56-Pin Plastic QFP**

\*1 Bonding option pin (DATA OUT or PWM OUT/BLANK IN)

## PIN DESCRIPTIONS

Pin	Symbol	Type	Description
1	V <sub>DD</sub>	—	Power Supply
2	V <sub>PARK</sub>	I	Day/night switching pin. When the high level is input, the IC enters the night mode and the value determined by the analog or digital dimming circuit is used as the output duty. When the low level is input, the IC enters the day mode and the output duty is about 100%.
3	V <sub>DIM</sub>	I	Analog voltage input for determining the analog dimming value. When the analog dimming circuit is used, the output duty is determined by the analog voltage to be input to this pin. When only the digital dimming circuit is used, pull down this pin to GND.
4	CS	I	Chip select input. Only when the high level is input to this pin, interfacing with a microcomputer is available through "CLOCK" and "DATA I/O" pins. Therefore, 2 signal lines of "CLOCK" and "DATA I/O" can be shared with other peripherals.
5	CLOCK	I	Serial clock input. Data is input-output through "DATA I/O" pin at the rising edge of the serial clock.
6	DATA I/O	I/O	Serial data input-output. This pin enters output mode only when the keyscan mode is selected. It enters input mode when other mode is selected.
7	INT	O	Interrupt signal output to microcomputer. When any key is pressed or released, key scanning is started. After the completion of the one cycle, this pin goes to the high level and keeps the high level until keyscan stop mode is selected.
8	$\overline{\text{TEST1}}$	I	Test signal input. As this pin has a built-in pull-up resistor, it must be left open or pulled up in the normal operation mode. When the low level is input to this pin, SEG1-30 go to the high level, and $\overline{\text{GRID1}}$ and $\overline{\text{GRID2}}$ go to the low level. (All segments go on.)
9	DATA OUT (Option)	O	Serial data output. Selecting this pin specifies the MSC1200V-xx. The data from DATA I/O is shifted out on the rising edge of the shift clock with a delay of 64 bits in the shift register. This pin can be used for connecting the IC with a LED driver in series.
9	PWM OUT/ BLANK IN (Option)	I/O	When the V <sub>PARK</sub> pin is at the high level, the pulse with the duty ratio determined by the analog or digital dimming circuit is output through this pin. When this pin is at the low level, the pulse with the duty ratio determined by external circuit is input to this pin. This pin has an internal active pull-up resistor, which becomes active only when the V <sub>PARK</sub> pin is at the low level. When the V <sub>PARK</sub> pin is at the low level, this pin receives blanking signal from external circuits, so that output duty cycle can be controlled. Selecting this pin specifies the MSC1200-xx.

Pin	Symbol	Type	Description
10-15	$\overline{\text{COLUMN}}_{0-5}$	I	Return inputs from key matrix switch. A pull-up resistor is internally connected to each of these pins so that they are at the high level except when the low level is input by depression of a key. These pins are "L" active.
16-20	ROW0-4	O	Key switch scanning outputs. Normally the low level is output through these pins. When any key is depressed or released, keyscanning is started and is continued until keyscan stop mode is selected. When the keyscan stop mode is selected and then keyscanning is stopped, all outputs of ROW0-4 go back to the low level.
21, 49	GND	—	Ground
22, 23	OSC0 OSC1	I/O	Connecting pins for RC oscillation circuit. Connect a resistor between OSC1 and OSC0, and a capacitor between OSC0 and ground.
24-48, 50-54	SEG1-30	O	Segment signal output. Signals for driving VF display tube are output through these pins.
55, 56	$\overline{\text{GRID}}_{1,2}$	O	Grid signal output. Signals for driving VF display tube are output through these pins. Signals inverted with respect to grid signals are output. Normally, these pins are connected to the external grid driver (PNP transistor etc.) inputs.

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	$V_{DD}$	—	-0.3 to +20	V
Input Voltage (1)	$V_{IN1}$	All inputs except $V_{PARK}$	-0.3 to +6	V
Input Voltage (2)	$V_{IN2}$	$V_{PARK}$	-0.3 to $V_{DD} + 0.3$	V
Storage Temperature	$T_{STG}$	—	-65 to +150	°C
Power Dissipation	$P_D$	$T_a = 85^\circ\text{C}$	400	mW

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	$V_{DD}$	—	8	—	18	V
High Level Input Voltage (1)	$V_{IH1}$	All inputs except $V_{PARK}$ & OSC0	3.8	—	5.5	V
High Level Input Voltage (2)	$V_{IH2}$	$V_{PARK}$	3.8	—	$V_{DD}$	V
High Level Input Voltage (3)	$V_{IH3}$	OSC0	4.5	—	5.5	V
Low Level Input Voltage (1)	$V_{IL1}$	All inputs except OSC0	0	—	0.8	V
Low Level Input Voltage (2)	$V_{IL2}$	OSC0	0	—	0.5	V
Clock Frequency	$f_C$	—	—	—	250	kHz
OSC Frequency	$f_{OSC}$	$R = 4.7\text{k}\Omega, C = 10\text{pF}$	—	3.3	—	MHz
Frame Frequency	$f_{FR}$	$f_{OSC} = 3\text{MHz}$	—	201	—	Hz
Operating Temperature	$T_{op}$	—	-40	—	+85	°C

## ELECTRICAL CHARACTERISTICS

## DC Characteristics

(Ta = -40 to +85°C, V<sub>DD</sub> = 8 to 18V)

Parameter	Symbol	Condition	Min.	Max.	Unit
High Level Input Voltage (1) *1	V <sub>IH1</sub>	—	3.8	5.5	V
High Level Input Voltage (2) *9	V <sub>IH2</sub>	—	3.8	V <sub>DD</sub>	V
High Level Input Voltage (3) *2	V <sub>IH3</sub>	—	4.5	5.5	V
Low Level Input Voltage (1) *10	V <sub>IL1</sub>	—	0	0.8	V
Low Level Input Voltage (2) *2	V <sub>IL2</sub>	—	0	0.5	V
High Level Input Current (1) *3	I <sub>IH1</sub>	V <sub>IH1</sub> = 5.0V	-5	5	μA
High Level Input Current (2) *4	I <sub>IH2</sub>	V <sub>IH2</sub> = 5.0V	-30	30	μA
High Level Input Current (3) *5	I <sub>IH3</sub>	V <sub>IH3</sub> = 5.0V	-80	80	μA
Low Level Input Current (1) *3	I <sub>IL1</sub>	V <sub>IL1</sub> = 0V	-5	-5	μA
Low Level Input Current (2) *4	I <sub>IL2</sub>	V <sub>IL2</sub> = 0V	-160	-15	μA
Low Level Input Current (3) *5	I <sub>IL3</sub>	V <sub>IL3</sub> = 0V	-0.6	0.1	mA
Input Leakage Current *6	I <sub>IL</sub>	V <sub>I</sub> = 0 to 5.5V	-10	10	μA
High Level Output Voltage (1) *7	V <sub>OH1</sub>	V <sub>DD</sub> = 9.5V, I <sub>OH1</sub> = -6mA	V <sub>DD</sub> -0.8	—	V
High Level Output Voltage (2) *8	V <sub>OH2-1</sub>	V <sub>DD</sub> = 9.5V, I <sub>OH2</sub> = -200μA	4	6	V
	V <sub>OH2-2</sub>	V <sub>DD</sub> = 9.5V, Output Open	4.5	6	V
Low Level Output Voltage (1) *7	V <sub>OL1-1</sub>	V <sub>DD</sub> = 9.5V, I <sub>OL1-1</sub> = 500μA	—	2	V
	V <sub>OL1-2</sub>	V <sub>DD</sub> = 9.5V, I <sub>OL1-2</sub> = 200μA	—	1	V
	V <sub>OL1-3</sub>	V <sub>DD</sub> = 9.5V, I <sub>OL1-3</sub> = 2μA	—	0.3	V
Low Level Output Voltage (2) *8	V <sub>OL2</sub>	V <sub>DD</sub> = 9.5V, I <sub>OL2</sub> = 200μA	—	0.8	V
Power Supply Current	I <sub>DD</sub>	f <sub>OSC</sub> = 3.3MHz, No load	—	20	mA

\*1 Applicable to all input pins (except V<sub>PARK</sub> and OSC0 pins)

\*2 Applicable to OSC0 pin

\*3 Applicable to CLOCK, DATA I/O, CS, and V<sub>PARK</sub> pins\*4 Applicable to COLUMN0 to COLUMN5 and PWM OUT/BLANK IN pins\*5 Applicable to TEST1 pin\*6 Applicable to V<sub>DIM</sub> pin\*7 Applicable to SEG1 to SEG30, GRID1, and GRID2 pins\*8 Applicable to ROW0 to ROW4, DATA I/O, PWMOUT/BLANK IN, DATAOUT, and INT pins.\*9 Applicable to V<sub>PARK</sub> pin

\*10 Applicable to all input pins (except OSC0)



## AC Characteristics

(Ta = -40 to +85°C, V<sub>DD</sub> = 8 to 18V)

Parameter	Symbol	Condition	Min.	Max.	Unit
Oscillation Frequency	f <sub>OSC</sub>	R = 4.7kΩ±1%, C = 10pF±5%	2	4.66	MHz
Input Frequency to OSC0 from Outside	f <sub>OSCI</sub>	External input only	2.4	3.7	MHz
Frame Frequency	f <sub>FR</sub>	—	122	284	Hz
PWM OUT Frequency	f <sub>PWM</sub>	—	244	568	Hz
Clock Frequency	f <sub>C</sub>	—	—	250	kHz
Clock Pulse Width	t <sub>CW</sub>	—	1.3	—	μs
Data Setup Time	t <sub>DS</sub>	—	1	—	μs
Data Hold Time	t <sub>DH</sub>	—	200	—	ns
CS Pulse Width	t <sub>CSW</sub>	—	68	—	μs
CS Off Time	t <sub>CSL</sub>	—	30	—	μs
CS Setup Time CS – Clock Time	t <sub>CSH</sub>	—	2	—	μs
CS Hold Time Clock – CS Time	t <sub>CSH</sub>	—	2	—	μs
Data Output Delay Clock – Data output Time	t <sub>PD</sub>	—	—	1	μs
SEG & $\overline{\text{GRID}}$ Output Delay from CS	t <sub>ODS</sub>	CI = 100pF	—	8	μs
Slew Rate (All Drivers)	t <sub>R</sub>	CI = 100pF, t = 20% to 80% or 80% to 20% of V <sub>DD</sub>	—	5	μs
CS Time at Power-on	t <sub>PCS</sub>	—	300	—	μs
Hold Time at Power-off	t <sub>POF</sub>	When mounted on the unit V <sub>DD</sub> =0.0V	5	—	ms
Rise Time at Power-on	t <sub>PRZ</sub>	When mounted on the unit	—	100	μs

## Dimming Characteristics

### • DC characteristics

(Ta = -40 to +85°C, V<sub>DD</sub> = 8 to 18V)

Parameter	Condition	Min.	Typ.	Max.	Unit
D/A Output Voltage Error	—	—	—	±3	%
Reference Voltage Accuracy	Note 1	—	—	±6	%

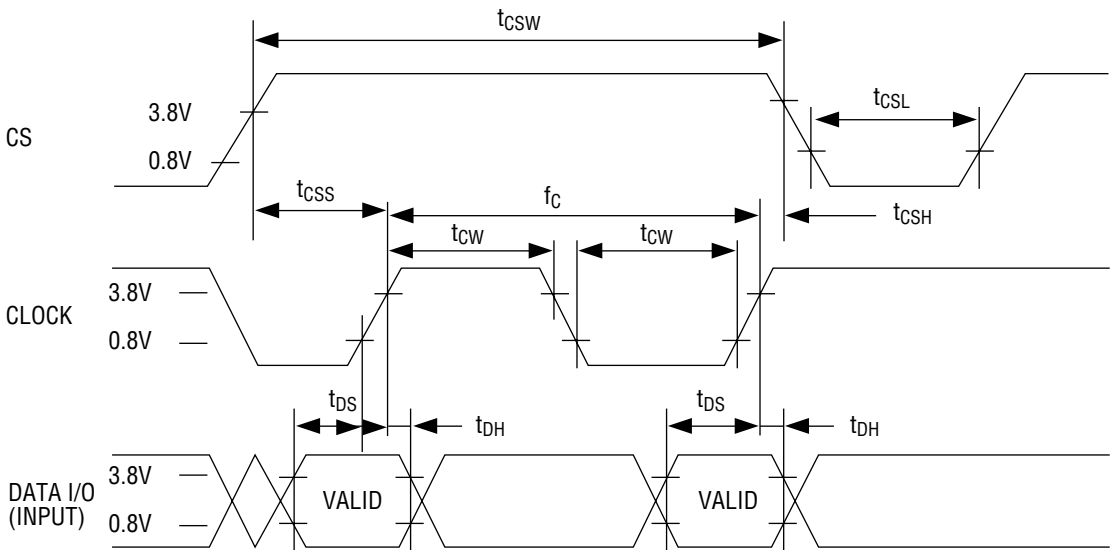
Note: 1. Reference voltage is 6.6V typical.

## Keyscan Characteristics

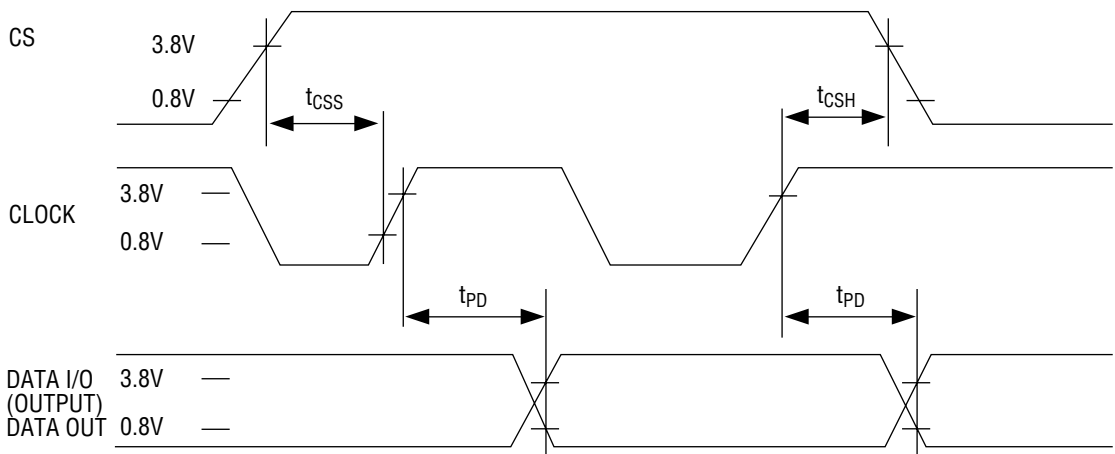
(Ta = -40 to +85°C, V<sub>DD</sub> = 8 to 18V)

Parameter	Condition	Min.	Typ.	Max.	Unit
Keyscan Cycle Time	f <sub>OSC</sub> =3.3 MHz	275	390	640	μs
Keyscan Pulse Width	f <sub>OSC</sub> =3.3 MHz	55	78	128	μs

**TIMING DIAGRAM**

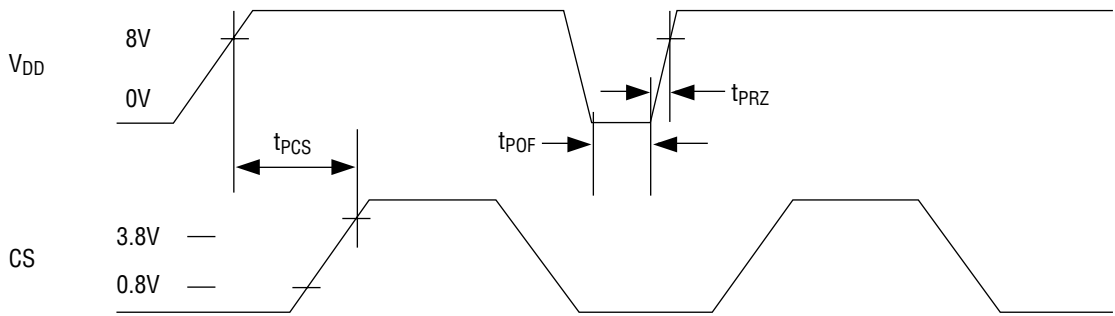


**Figure 1 Data Input Timing**

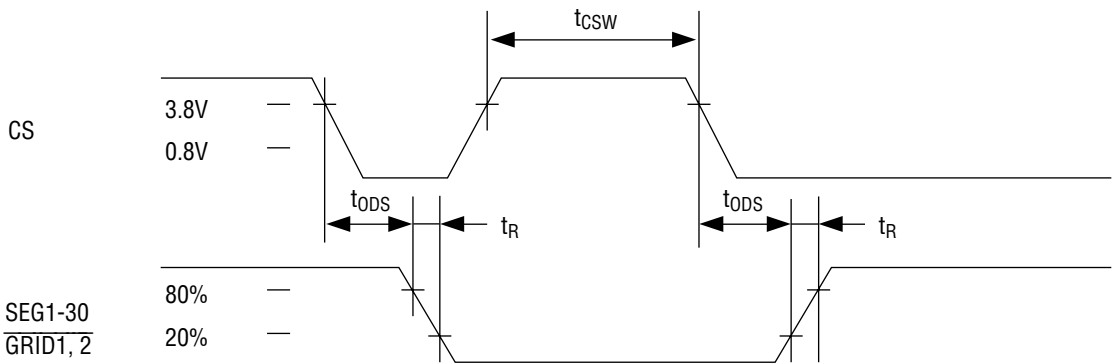


**Figure 2 Data Output Timing**

**TIMING DIAGRAM (Continued)**



**Figure 3 Power-On Timing**



**Figure 4 SEG &  $\overline{GRID}$  Output Timing**

## FUNCTIONAL DESCRIPTION

### Power-on Reset

The IC is initialized by the built-in power-on reset circuit at power-on. The status of the internal circuit after initialization is as follows;

- 1) Shift registers and latches are reset.
- 2) Analog dimming is selected.
- 3) Digital dimming data register is reset.
- 4) Display data input mode is selected.

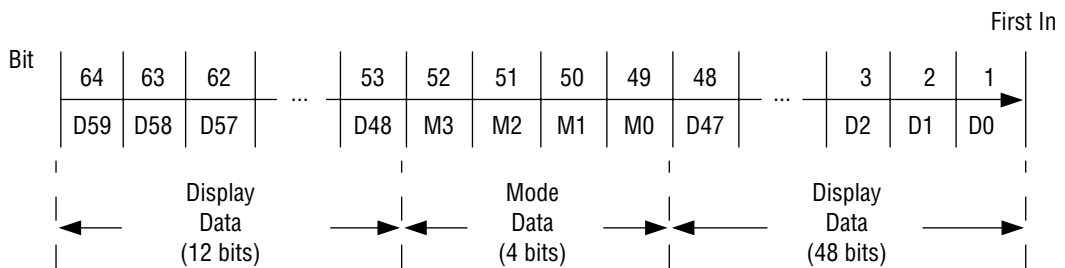
### Data Input

Data input is valid only when the high level is applied to the "CS" pin. Input data is input into the shift register through "DATA I/O" pin at the rising edge of CLOCK. The data is automatically loaded to latches at the falling edge of "CS" signal.

[Data Format]

#### 1) Display Data Input Mode

- Input data : 64 bits
- VF display data : 60 bits
- Mode select data : 4 bits



#### 2) Correspondence between segment outputs and shift register bits

The correspondence differs depending on the PLA code.

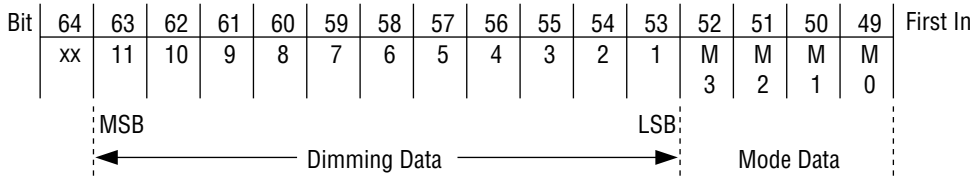
This table shows an example when using the product with general purpose code "-01".

By changing the PLA code, the segment output position can be changed but the bit correspondence cannot be changed.

	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	SEGN
Bit	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	GRID1
	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	GRID2

3) Digital Dimming Data Input Mode

Input data : 16 bits  
 Digital dimming data : 11 bits  
 Mode select data : 4 bits



(MSB)	INPUT DATA											(LSB)	DUTY CYCLE	
X	0	0	0	0	0	0	0	0	0	0	0	0	0	0/2048
X	0	0	0	0	0	0	0	0	0	0	0	1	1	1/2048
X	1	1	1	1	1	1	1	0	0	0	0	0	2032/2048	
X	1	1	1	1	1	1	1	1	1	1	1	1	2032/2048	

## 4) Function Mode

Mode	M3	M2	M1	M0	Function
S1	0	0	0	0	Display Data Input
S2	0	0	1	1	Analog Dimming Select
S3	0	1	0	1	Digital Dimming Select
S4	0	0	0	1	Digital Dimming Data Input & Digital Dimming Select
S5	0	1	1	1	Keyscan Data Output
S6	0	1	1	0	Display Data Input & Keyscan Data Output
S7	0	0	1	0	Display Data Input & Analog Dimming Select
S8	0	1	0	0	Display Data Input & Digital Dimming Select
S9	1	0	0	0	Keyscan Data Output & Keyscan Stop
SA	1	0	0	1	Keyscan S <sub>TOP</sub>

Note: Other combinations are used for test modes.

## 5) Analog Dimming Mode

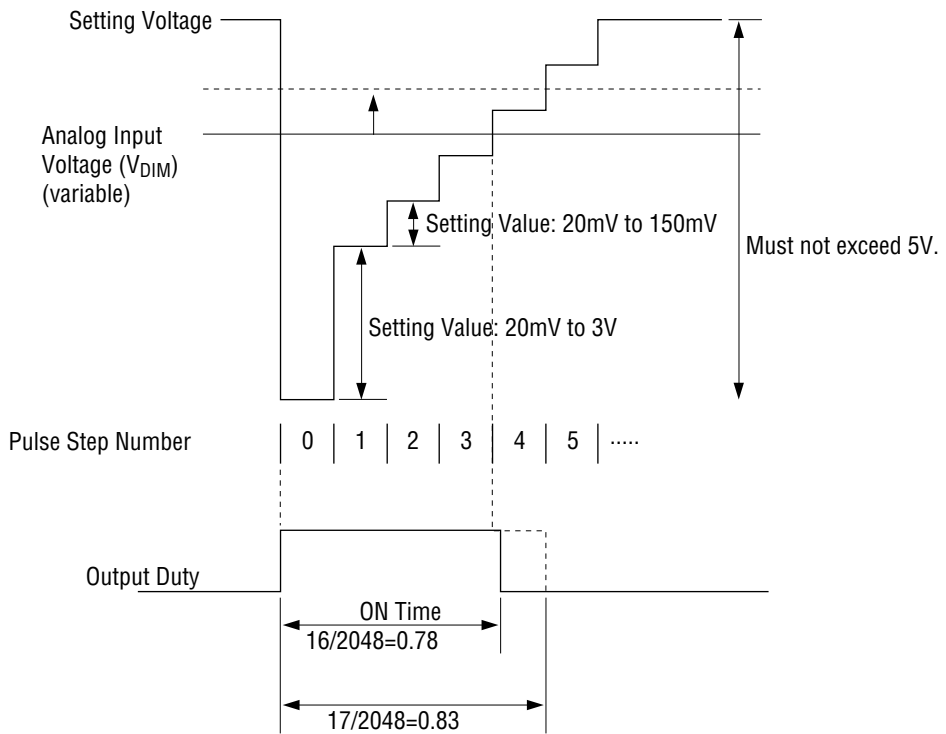
Analog dimming is automatically selected when the V<sub>PARK</sub> pin is set to the high level after power-on. Therefore, when digital dimming is used, mode setting is required before the V<sub>PARK</sub> pin is set to the high level.

The output duty ratio for analog dimming is 12.5% maximum. The correspondence between threshold voltage and output duty ratio is programmed by the mask.

A table is given later as a model, showing the correspondence between threshold dimming voltage and pulse width modulation (PWM) duty cycle when using the product with general purpose code "-01".

Note the following when setting analog dimming with a new general purpose code:

1. The number of steps is 52 when the output duty ratio is a maximum of 12.5%.
2. The setting value for threshold voltage (input voltage to V<sub>DIM</sub>) must not exceed 5V. If a voltage greater than 5V is input, the IC may not operate normally.
3. The setting voltage for each step ranges from 20mV to 150mV. However, only step No. 1 has the different range of 20mV to 3V.

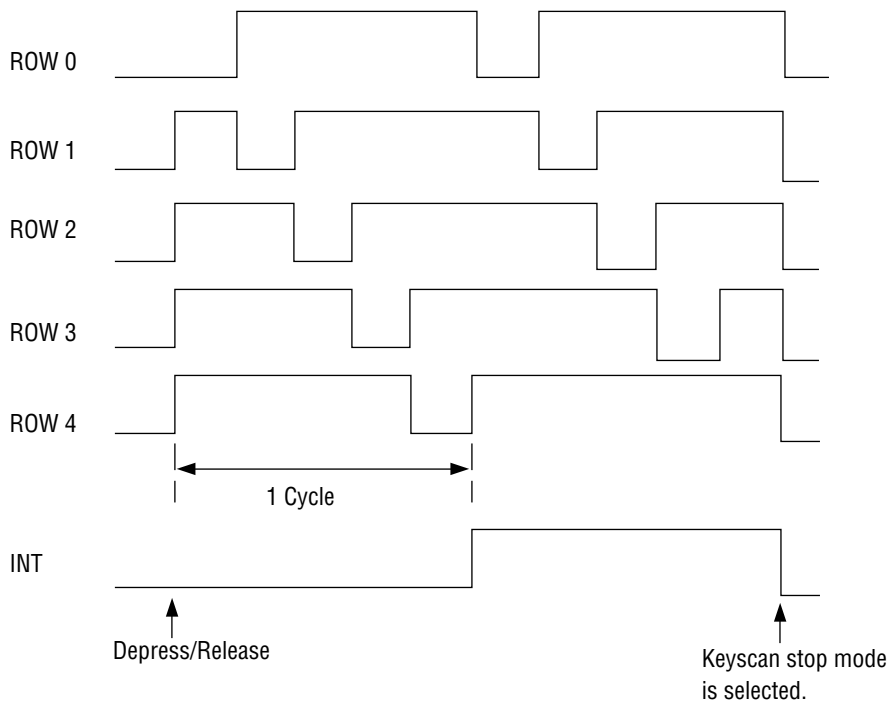




### Keyscan

Keyscanning is started only when depression or release of any key is detected in order to minimize noise caused by scanning signal. Then, keyscanning is continued until the keyscan stop mode signal is sent from a microcomputer. The INT pin goes to the high level at the completion of 1-cycle scanning after the keyscan start, so the (high level) signal sent from the INT pin can be used as an interrupt signal.

[Keyscan Timing]



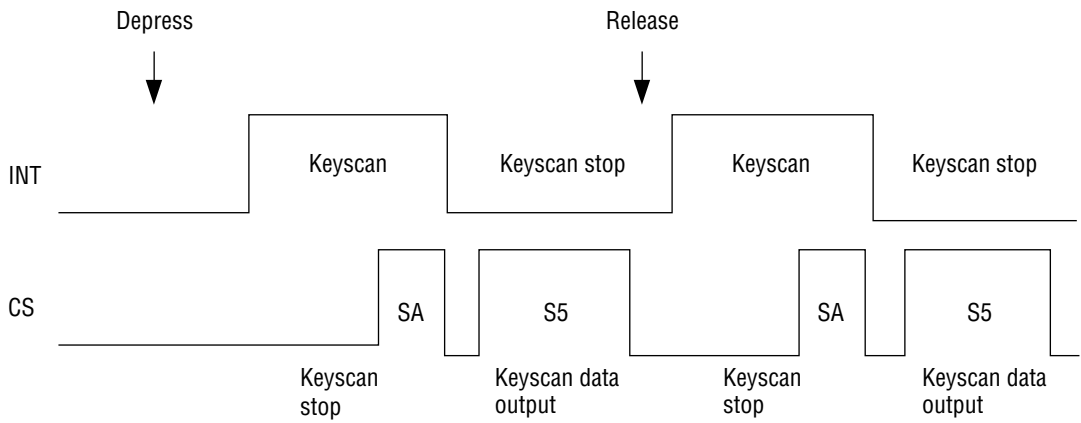
Note: Keyscanning cannot be stopped by selecting the keyscan stop mode only once if:

- keyscanning is started after depression or release of any key is detected, and then
- a key is depressed or released again before the keyscan stop mode is selected.

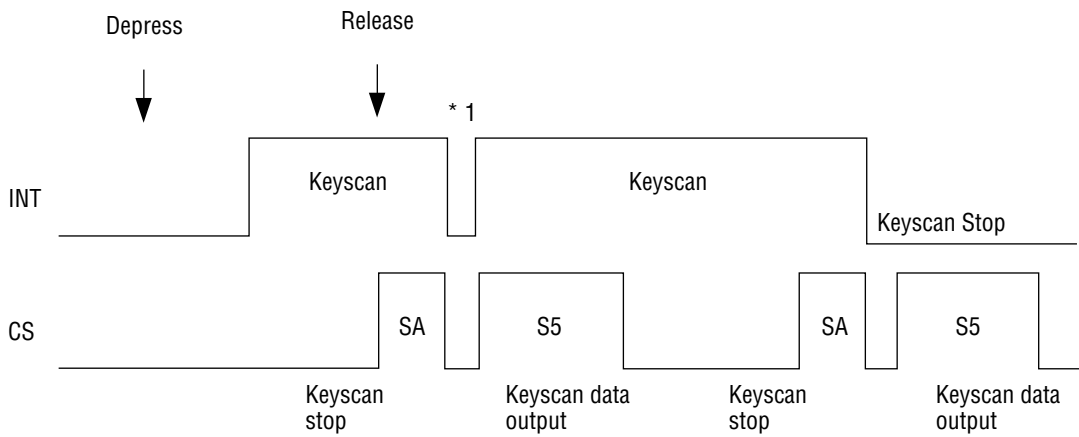
To stop keyscanning, it is required to select the keyscan stop mode once again.

[Example]

A) When Key Input Status is Changed



B) When Key Input Status is Changed before Keyscan Stop Mode Select



\*1: Keyscanning resumes after short period of keyscan stop.

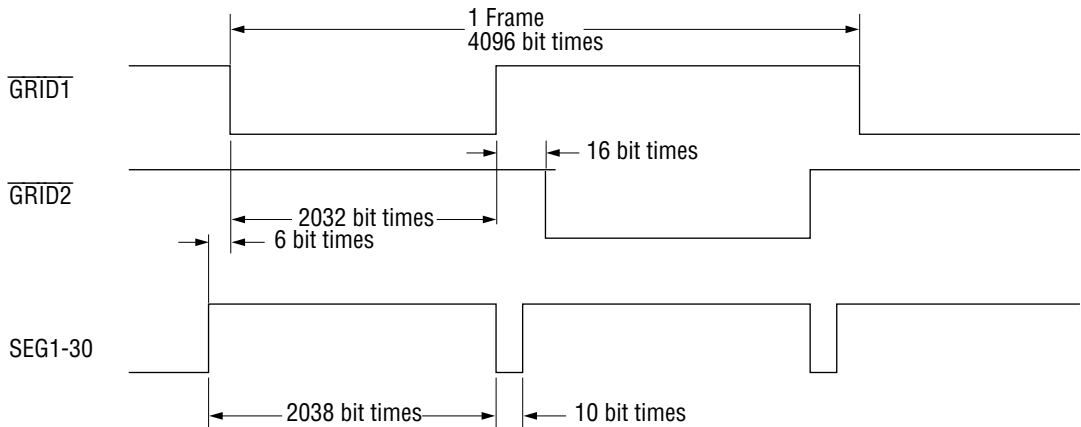


**GRID/SEG Driver Operation and Digital/Analog Dimming Operation**

Figure 5 shows the output timing of the GRID and SEG driver when the  $V_{PARK}$  is the "H" level.

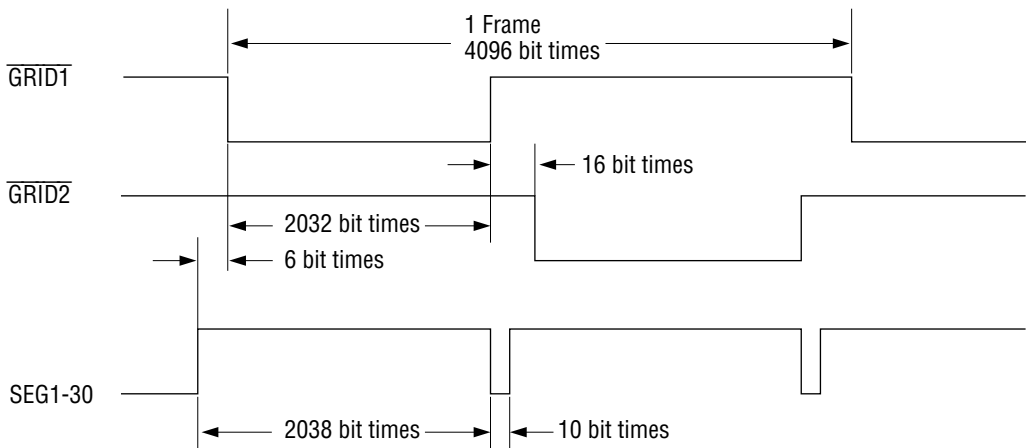
Figure 6 shows the output timing of the GRID and SEG drivers for the digital dimming mode operation.

Figure 7 shows the output timing of the GRID and SEG drivers for the analog dimming mode operation.



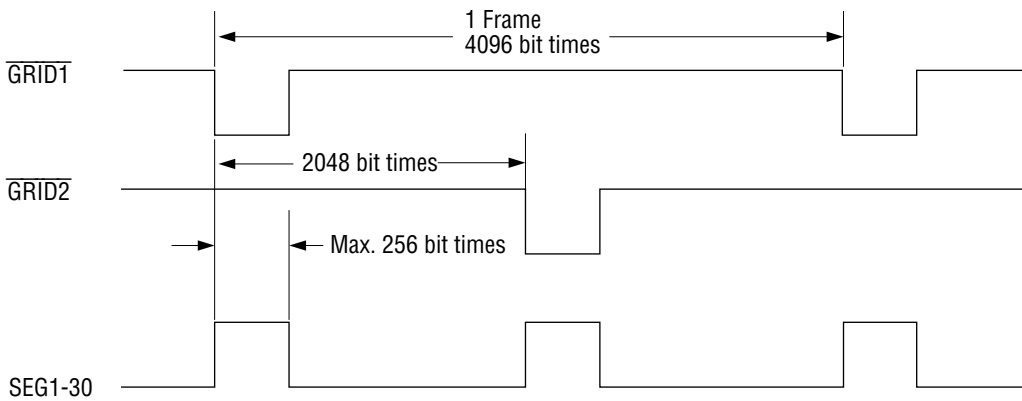
**Figure 5 GRID and SEG Output Timing ( $V_{PARK}$ ="H")**

Note: 1 bit time =  $T_{OSC} (4/f_{OSC}) = 1.2\mu s$  (typ.)



**Figure 6 GRID and SEG Output Timing (Digital Dimming Mode)**

- Notes: 1. Shown above is the timing in the digital dimming mode with the duty cycle of 2032/2048 at  $V_{PARK}$  = "L".
- 2. The length of time that the grids and the segments are turned on is specified with respect to 11 bits of the digital dimming data.
- 3. 1 bit time =  $T_{OSC} (4/f_{OSC}) = 1.2\mu s$  (typ.)

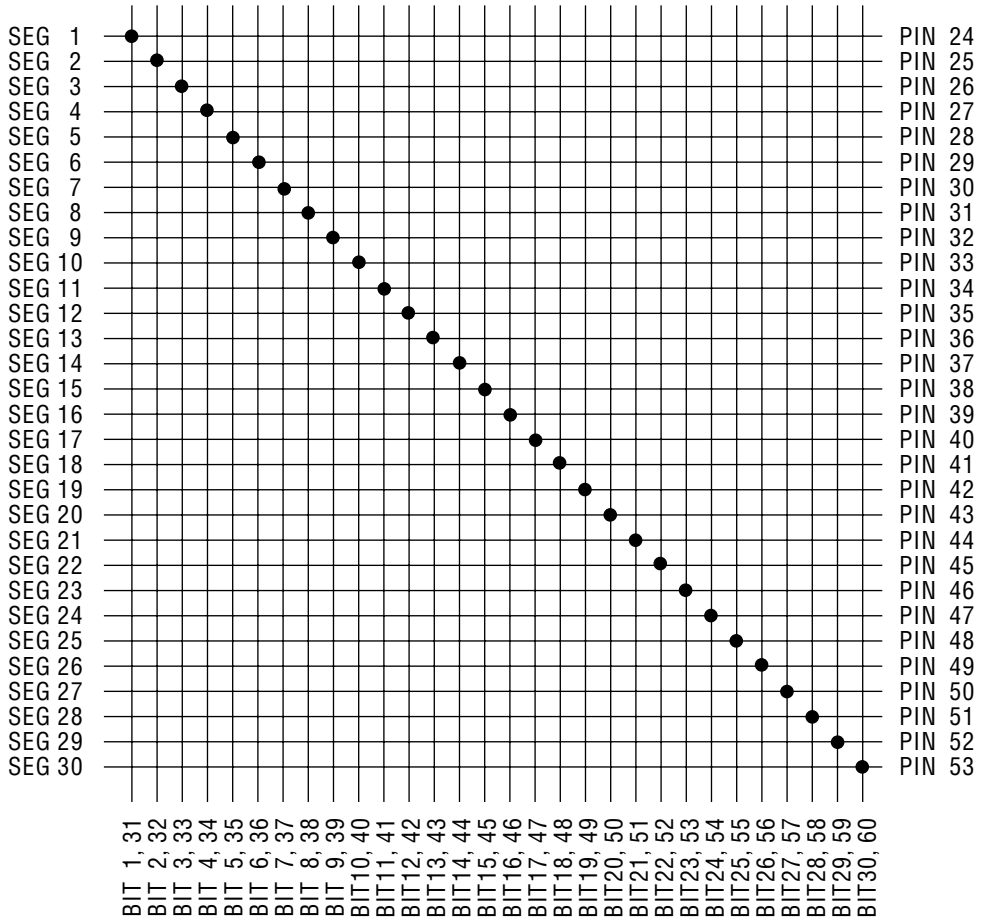


**Figure 7 GRID and SEG Output Timing (Analog Dimming Mode)**

- Notes: 1. Shown above is the timing for the GRID and SEG Drivers in the analog dimming mode at  $V_{PARK} = "L"$ .  
 2. 1 bit time =  $T_{OSC} (4/f_{OSC}) = 1.2\mu s$  (typ.)

PLA Code Table

MSC1200-01  
MSC1200V-01



PIN NAME	OUTPUT	PIN NAME	OUTPUT	PIN NAME	OUTPUT
SEG1	BIT 1, 31	SEG11	BIT 11, 41	SEG21	BIT 21, 51
SEG2	BIT 2, 32	SEG12	BIT 12, 42	SEG22	BIT 22, 52
SEG3	BIT 3, 33	SEG13	BIT 13, 43	SEG23	BIT 23, 53
SEG4	BIT 4, 34	SEG14	BIT 14, 44	SEG24	BIT 24, 54
SEG5	BIT 5, 35	SEG15	BIT 15, 45	SEG25	BIT 25, 55
SEG6	BIT 6, 36	SEG16	BIT 16, 46	SEG26	BIT 26, 56
SEG7	BIT 7, 37	SEG17	BIT 17, 47	SEG27	BIT 27, 57
SEG8	BIT 8, 38	SEG18	BIT 18, 48	SEG28	BIT 28, 58
SEG9	BIT 9, 39	SEG19	BIT 19, 49	SEG29	BIT 29, 59
SEG10	BIT 10, 40	SEG20	BIT 20, 50	SEG30	BIT 30, 60

**V<sub>DIM</sub> Threshold Dimming Voltage VS. PWM Duty Cycle (Typical Value)**

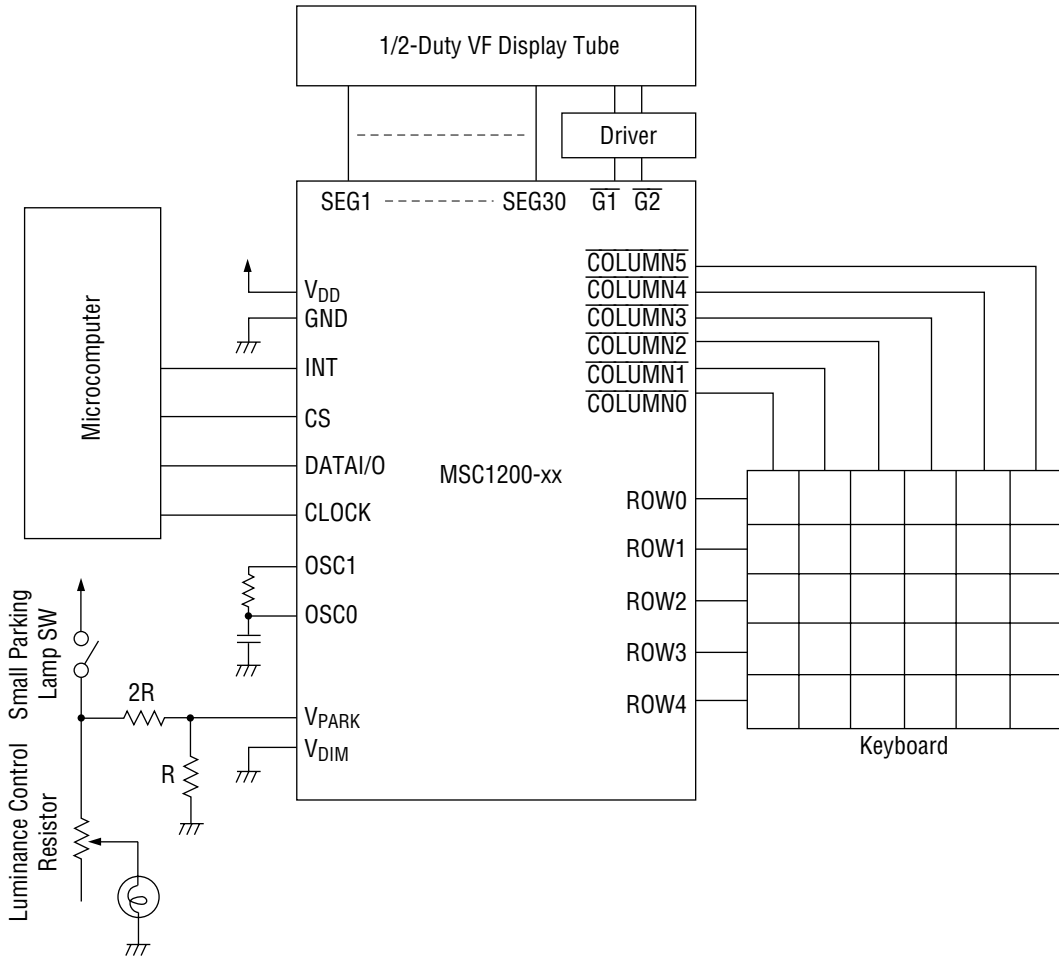
V<sub>DD</sub>=12.8V

Pulse Step Number	PWM Duty Cycle		Threshold Voltage	Pulse Step Number	PWM Duty Cycle		Threshold Voltage
	Pulse Count	%			Pulse Count	%	
			Vref				3.000
52	256/2048	12.5	4.200	26	56/2048	2.73	2.950
51	240/2048	11.7	4.130	25	52/2048	2.54	2.900
50	224/2048	10.9	4.070	24	48/2048	2.34	2.850
49	208/2048	10.2	4.000	23	46/2048	2.25	2.820
48	192/2048	9.38	3.930	22	44/2048	2.15	2.800
47	184/2048	8.98	3.890	21	42/2048	2.05	2.770
46	176/2048	8.59	3.850	20	40/2048	1.95	2.740
45	168/2048	8.20	3.810	19	38/2048	1.86	2.710
44	160/2048	7.81	3.770	18	36/2048	1.76	2.680
43	152/2048	7.42	3.725	17	34/2048	1.66	2.650
42	144/2048	7.03	3.680	16	32/2048	1.56	2.615
41	136/2048	6.64	3.625	15	30/2048	1.46	2.580
40	128/2048	6.25	3.580	14	28/2048	1.37	2.540
39	120/2048	5.86	3.525	13	26/2048	1.27	2.500
38	112/2048	5.47	3.460	12	24/2048	1.17	2.470
37	104/2048	5.08	3.400	11	23/2048	1.12	2.450
36	96/2048	4.69	3.340	10	22/2048	1.07	2.430
35	92/2048	4.49	3.305	9	21/2048	1.03	2.410
34	88/2048	4.30	3.270	8	20/2048	0.98	2.390
33	84/2048	4.10	3.240	7	19/2048	0.93	2.370
32	80/2048	3.91	3.200	6	18/2048	0.88	2.340
31	76/2048	3.71	3.160	5	17/2048	0.83	2.320
30	72/2048	3.52	3.120	4	16/2048	0.78	2.295
29	68/2048	3.32	3.080	3	15/2048	0.73	2.270
28	64/2048	3.13	3.040	2	14/2048	0.68	2.245
27	60/2048	2.93	2.93	1	13/2048	0.63	0.000
				0			

Note: A threshold voltage more than 5V cannot be set.

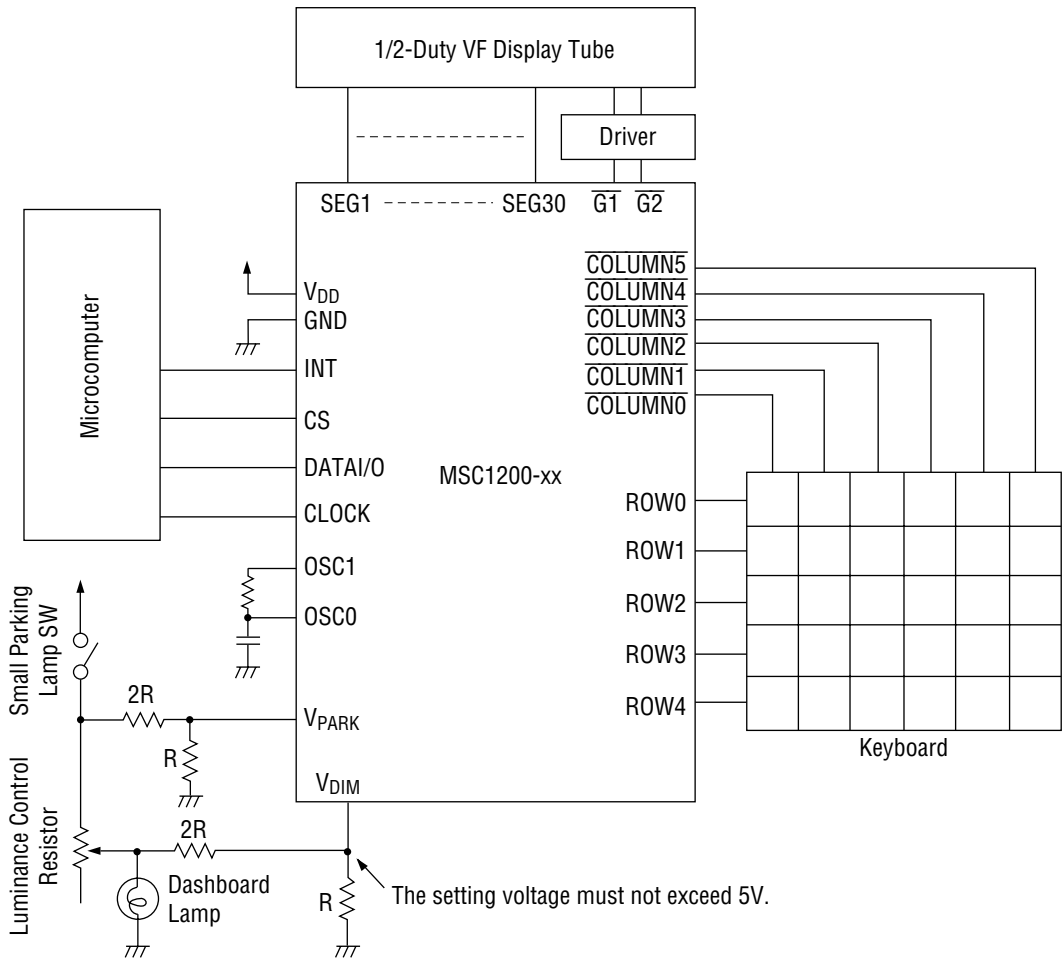
APPLICATION CIRCUITS

(A) Digital Dimming



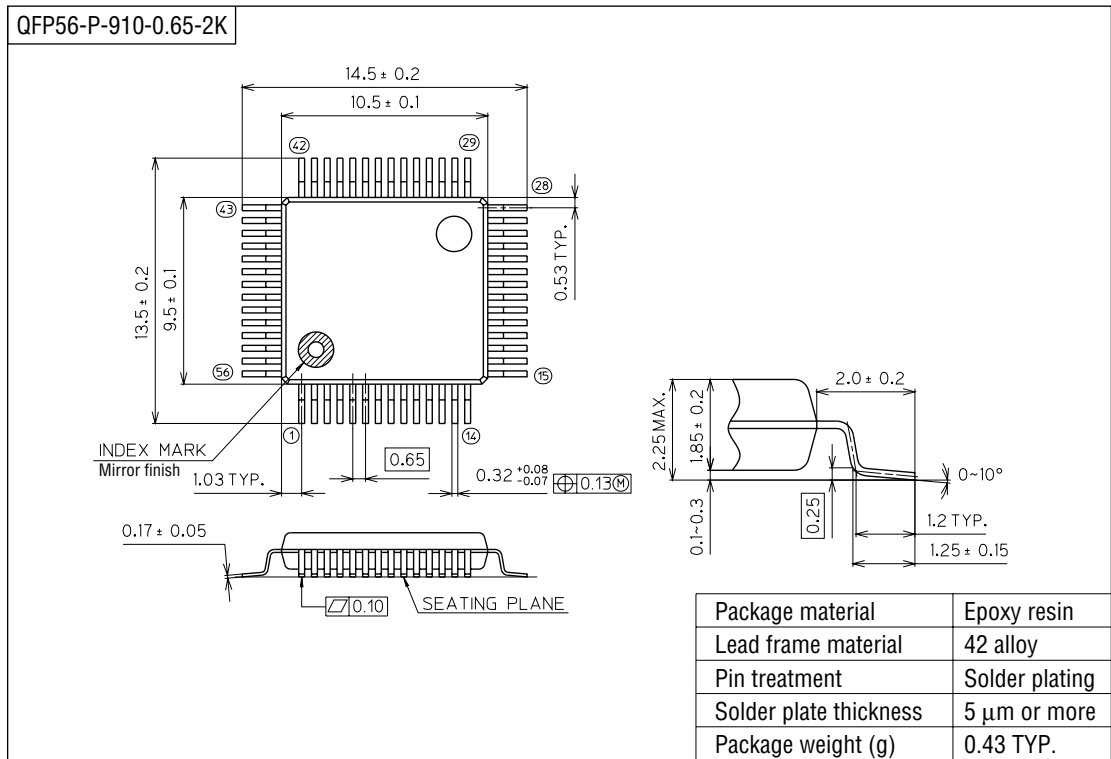


(B) Analog Dimming



**PACKAGE DIMENSIONS**

(Unit : mm)



**Notes for Mounting the Surface Mount Type Package**

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki’s responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).