TRI-STATE Dual 2/4 Demultiplexers

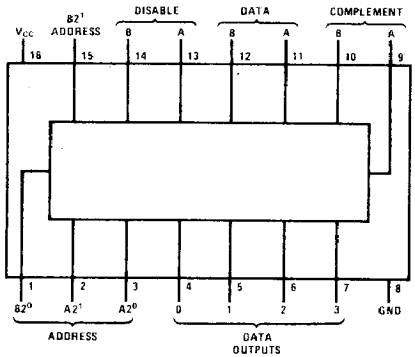
General Description

These circuits route both a data input, as well as its complement, to two of four output lines, depending upon the binary code applied to the address lines. There are two separate data lines, separate address lines for each, as well as the complement of each data line. Which set of address lines is active depends upon which disable line has a low logic level applied. The disable inputs have the additional feature that when both have a high logic level applied, the outputs go to the third (high-impedance) state.

Features

- Separate input disables
- Data complement capability
- Typical propagation delay 20 ns
- Low output impedance — high drive capability

Connection Diagram



7230(J), (W); 8230(J), (N), (W)

Truth Table

DATA A	COMP A	DATA B	COMP B	ADDRESS A 2^1	ADDRESS A 2^0	ADDRESS B 2^1	ADDRESS B 2^0	DIS A	DIS B	OUT 0	OUT 1	OUT 2	OUT 3
L	L	X	X	L	L	X	X	L	H	L	H	H	H
L	H	X	X	L	L	X	X	L	H	H	H	H	H
H	L	X	X	L	L	X	X	L	H	H	H	H	H
H	H	X	X	L	L	X	X	L	H	L	H	H	H
L	L	X	X	L	H	X	X	L	H	H	L	H	H
L	H	X	X	L	H	X	X	L	H	H	H	H	H
H	L	X	X	L	H	X	X	L	H	H	H	H	H
H	H	X	X	L	H	X	X	L	H	H	L	H	H
L	L	X	X	H	L	X	X	L	H	H	H	L	H
L	H	X	X	H	L	X	X	L	H	H	H	H	H
H	L	X	X	H	L	X	X	L	H	H	H	H	H
H	H	X	X	H	L	X	X	L	H	H	H	L	H
L	L	X	X	H	H	X	X	L	H	H	H	H	L
L	H	X	X	H	H	X	X	L	H	H	H	H	H
H	L	X	X	H	H	X	X	L	H	H	H	H	H
H	H	X	X	H	H	X	X	L	H	H	H	H	L
X	X	L	L	X	X	L	L	H	L	L	H	H	H
X	X	L	H	X	X	L	L	H	L	H	H	H	H
X	X	H	L	X	X	L	L	H	L	H	H	H	H
X	X	H	H	X	X	L	L	H	L	L	H	H	H
X	X	L	L	X	X	L	H	H	L	H	L	H	H
X	X	L	H	X	X	L	H	H	L	H	H	H	H
X	X	H	L	X	X	L	H	H	L	H	H	H	H
X	X	H	H	X	X	L	H	H	L	H	L	H	H
X	X	L	L	X	X	H	L	H	L	H	H	L	H
X	X	L	H	X	X	H	L	H	L	H	H	H	H
X	X	H	L	X	X	H	L	H	L	H	H	H	H
X	X	H	H	X	X	H	L	H	L	H	H	L	H
X	X	L	L	X	X	H	H	H	L	H	H	H	L
X	X	L	H	X	X	H	H	H	L	H	H	H	H
X	X	H	L	X	X	H	H	H	L	H	H	H	H
X	X	H	H	X	X	H	H	H	L	H	H	H	L
X	X	X	X	X	X	X	X	H	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM72 30 MIN	DM72 30 TYP(1)	DM72 30 MAX	DM82 30 MIN	DM82 30 TYP(1)	DM82 30 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA, T_A = 25°C				−1.5			−1.5	V
I_{OH}	High Level Output Current					−2.0			−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max		2.4	3.5		2.4	3.5		V
I_{OL}	Low Level Output Current					16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA			0.2	0.4		0.2	0.4	V
$I_{O(OFF)}$	Off-State (High-Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V, V_{IL} = 0.8V	V_O = 0.4V			−40			−40	μA
			V_O = 2.4V			40			40	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Disable			80			80	μA
			Other			40			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Disable		−2.0	−3.2		−2.0	−3.2	mA
			Other		−1.0	−1.6		−1.0	−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−30		−70	−28		−70	mA
I_{CC}	Supply Current	V_{CC} = Max			48	75		48	75	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM	TO	CONDITIONS		DM72/82 30 MIN	DM72/82 30 TYP	DM72/82 30 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Output	Inverting	C_L = 50 pF, R_L = 400Ω		20	36	ns
				Non-Inverting			13	24	
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Output	Inverting			18	26	ns
				Non-Inverting			18	26	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Address(3)	Output				20	36	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Address(3)	Output				20	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Disable(4)	Output				13	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Disable(4)	Output				16	25	ns
t_{ZH}	Output Enable Time to High Level						15	23	ns
t_{ZL}	Output Enable Time to Low Level						18	27	ns
t_{HZ}	Output Disable Time from High Level				C_L = 5 pF, R_L = 400Ω		7	14	ns
t_{LZ}	Output Disable Time from Low Level						15	27	ns

Notes

(3) The only conditions under which a t_{PHL} from the Address inputs can be observed is when an output goes from being nonselected to being selected and the information being routed to that output is a logical "0." If the information had been a logical "1," no change would have occurred and no measurement could have been made. Similarly, the only time a t_{PLH} from the Address inputs can be observed, is when an output goes from being selected to being nonselected and the information that had been routed to that output was a logical "0." If the information had been a logical "1," no change would have occurred and no measurement could have been made.

(4) Information in Note 3 concerning t_{PLH} and t_{PLH} from the address inputs are applicable here also.

Logic Diagram