REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added device type 02; Editorial and technical changes throughout	94-04-19	M. A. FRYE

REV																			
SHEET																			
REV																			
SHEET																			

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
93-06-22

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, MICROPROCESSOR SUPERVISORY CIRCUIT, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-93125**

SHEET 1 OF 14

DESC FORM 193
JUL 91

5962-E211-94

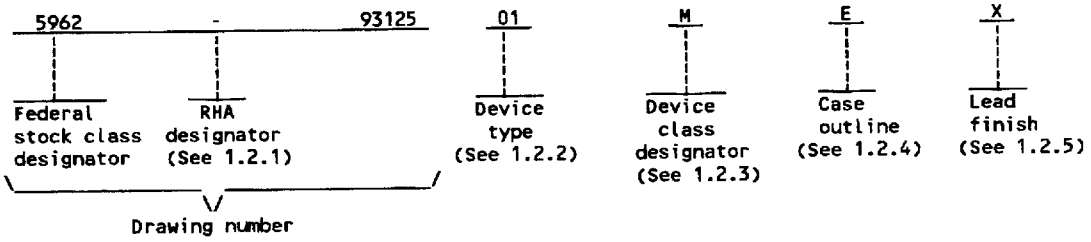
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0002738 790

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device class M RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	MAX697	Microprocessor supervisory circuit
02	MAX696	Microprocessor supervisory circuit with battery backup switching

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage range:	
V_{CC}	-0.3 V to +6.0 V
V_{BATT} (device type 02)	-0.3 V to +6.0 V
All other inputs	-0.3 V dc to (V_{OUT} + 0.5 V)
Input current:	
V_{CC}	+200 mA
V_{BATT} (device type 02)	+50 mA
GND	+20 mA
Output current:	
V_{OUT}	Short circuit protected
All other outputs	+20 mA
Rate-of-rise:	
V_{CC}	100 V/µs
V_{BATT} (device type 02)	100 V/µs
Storage temperature range	-65°C to +160°C
Power dissipation (P_D):	
Case outline E 2/	800 mW
Case outline 2 3/	727 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	+50°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case outline E	+100°C/W
Case outline 2	+110°C/W

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	3.0 V dc to 5.5 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Derate 10 mW/°C above +85°C.
3/ Derate 9.09 mW/°C above +70°C.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/ Min	Limits 2/ Max	Unit
Operating voltage range	V_{CC}		1,2,3	01	3.0	5.5	V
				02	3.2	5.5	
Operating voltage range	V_{BATT}		1,2,3	02	2.0	4.0	V
Supply current	I_{CC}		1,2,3	01		400	µA
BATTERY BACKUP SWITCHING							
Output voltage	V_{OUT}	I_{OUT} = 1 mA	1,2,3	02	V_{CC}-0.3		V
		I_{OUT} = 50 mA			V_{CC}-0.5		
Output voltage in battery backup mode	$BATT_{OUT}$	I_{OUT} = 250 µA $V_{CC} < V_{BATT}$ - 0.2 V	1,2,3	02	V_{BATT} -0.1		V
Supply current (excludes I_{OUT})	I_{CC}	I_{OUT} = 1 mA	1	02		4	mA
			2,3			7	
		I_{OUT} = 50 mA	1			7	
			2,3			10	
Supply current in battery backup mode	I_{BATT}	V_{CC} = 0 V, V_{BATT} = 2.8 V	1	02		1	µA
			2,3			10	
Battery standby leakage current	BATTLkg	5.5 V > V_{CC} > V_{BATT} + 1 V	1	02	-0.1	0.02	µA
			2,3		-1.0	0.02	
Battery switchover threshold (V_{CC} - V_{BATT})	$BATTSW_{TH}$		1,2,3	02	-200	200	mV
BATT on output voltage	BATT ON_{OUT}	I_{SINK} = 1.6 mA	1,2,3	02		0.4	V
BATT on output short circuit current	BATT ON_{IOS}	BATT ON = V_{OUT}	1,2,3	02		60	mA
		BATT ON = 0 V, V_{CC} = 0 V			0.5	25	µA
RESET AND WATCHDOG TIMING							
Low line voltage threshold	LL_{IN}	V_{CC} = +5 V, +3 V	1,2,3	All	1.25	1.35	V
Reset timeout delay	R_{DEL}	OSC SEL HIGH, V_{CC} = 5 V	9	All	35	70	ms
			10,11		31	78	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/ Min	Limits 2/ Max	Unit
RESET AND WATCHDOG TIMING							
Watchdog timeout period, internal oscillator	WD_{INT}	Long period, V_{CC} = 5 V	9	All	1.0	2.25	s
			10,11		0.9	2.42	
		Short period, V_{CC} = 5 V	9		70	140	ms
			10,11		62	154	
Watchdog timeout period external clock	WD_{EXT}	Long period	9,10,11	All	3840	4097	Clock cycles
		Short period			768	1025	
Minimum WDI input pulse width	WDI_{PW}	V_{IL} = 0.4 V, V_{IH} = 4.0 V V_{CC} = 5 V	9	All	200		ns
			10,11		300		
$\overline{\text{RESET}}$ output voltage	$\overline{R}_{VOH}$	I_{SOURCE} = 1 µA, V_{CC} = 5 V	1,2,3	All	3.5		V
	$\overline{R}_{VOL}$	I_{SINK} = 1.6 mA,				0.4	
		I_{SINK} = 400 µA, V_{CC} = 0 V		02		0.4	
$\overline{\text{LOW LINE}}$ output voltage	$\overline{LL}_{VOL}$	I_{SINK} = 800 µA	1,2,3	All		0.4	V
	$\overline{LL}_{VOH}$	I_{SOURCE} = 1 µA, V_{CC} = 5.0 V			3.5		
RESET output voltage	R_{VOH}	I_{SOURCE} = 1 µA, V_{CC} = 5 V	1,2,3	All	3.5		V
	R_{VOL}	I_{SINK} = 1.6 mA				0.4	
$\overline{\text{WDO}}$ output voltage	$\overline{WDO}_{VOH}$	I_{SOURCE} = 1 µA, V_{CC} = 5 V	1,2,3	All	3.5		V
	$\overline{WDO}_{VOL}$	I_{SINK} = 800 µA	2,3			0.4	
Output short circuit current	I_{OS}	$\overline{\text{RESET}}$, RESET, WDO, $\overline{\text{LOW LINE}}$	1,2,3	All	1	25	µA
WDI input threshold logic low	WDI_{VIL}	V_{CC} = 5 V 3/ 4/	1	All		0.8	V
			2,3			0.4	
WDI input threshold logic high	WDI_{VIH}	V_{CC} = 5 V 3/ 4/	1	01	3.8		V
				02	3.5		
			2,3	All	4.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/ Min	Limits 2/ Max	Unit
RESET AND WATCHDOG TIMING							
WDI input current	WDI_{IN}	WDI = V_{CC}	1	01		50	µA
			2,3			80	
		WDI = 0 V	1		-50		
			2,3		-80		
		WDI = V_{OUT}	1	02		50	
			2,3			80	
		WDI = 0 V	1		-50		
			2,3		-80		
POWER FAIL DETECTOR							
PFI input threshold	PFI_{VTH}	V_{CC} = +3 V, +5 V 3/	1,2,3	All	1.2	1.4	V
PFI-LL_{IN} threshold difference	$PFILL_{IN}$	V_{CC} = +3 V, +5 V	1	All	-50	+50	mV
PFI input current	PFI_{IN}		1,2,3	All	-25	+25	nA
LL_{IN} input current	LL_{IN}		1,2,3	01	-25	+25	nA
				02	-500	+25	
$\overline{PFO}$ output voltage	$\overline{PFO}_{VOH}$	I_{SOURCE} = 1 µA, V_{CC} = 5 V	1,2,3	All	3.5		V
	$\overline{PFO}_{VOL}$	I_{SINK} = 1.6 mA				0.4	
$\overline{PFO}$ short circuit source current	$\overline{PFO}_{IOS}$	PFI = V_{IH}, $\overline{PFO}$ = 0 V	1,2,3	All	1	25	µA
CHIP ENABLE GATING							
$\overline{CE}_{IN}$ thresholds logic low	$\overline{CE}_{VIL}$		1	01		0.8	V
			2,3			0.4	
$\overline{CE}_{IN}$ thresholds logic high	$\overline{CE}_{VIH}$	V_{CC} = +5 V	1	01	3.0		V
			2,3		3.5		
$\overline{CE}_{IN}$ pullup current	$\overline{CEIN}_{PI}$		1,2,3	01	1	25	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/ Min	Limits 2/ Max	Unit
CHIP ENABLE GATING							
$\overline{CE}_{OUT}$ output voltage	$\overline{CE}_{VOH}$	I_{SOURCE} = 800 µA,	1,2,3	01	V_{OUT} -0.5		V
		I_{SOURCE} = 1 µA			V_{OUT} -0.05		
	$\overline{CE}_{VOL}$	I_{SINK} = 1.6 mA				0.4	
$\overline{CE}$ propagation delay	t_{PDCE}	V_{CC} = 5 V	9	01		150	ns
			10,11			250	
OSCILLATOR							
OSC IN input current	$OSCIN_{IN}$		1,2,3	All		25	µA
OSC SEL input pullup current	$OSCSEL_{IN}$	V_{CC} = 5 V	1,2,3	All	1	25	µA
OSC IN frequency range	$OSCIN_{FRQ}$	OSC SEL = 0 V, V_{CC} = 5 V	9,10,11	All	0	250	kHz
OSC IN frequency with external capacitor	OSCIN	OSC SEL = 0 V, COSC = 47 pF, T_A = +25°C 5/	9	All	4		kHz

1/ V_{CC} = 3.0 V to 5.5 V, V_{BATT} = 2.8 V unless otherwise specified.

2/ The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

3/ The input voltage limits on PFI and WDI may be exceeded provided the input current is limited to less than 10 mA.

4/ WDI is guaranteed to be in the mid-level (inactive) state if WDI is floating and V_{CC} is in the operating voltage range. WDI is internally biased to 38 percent of V_{CC} with an impedance of approximately 125 kΩ.

5/ Design characteristic, not tested.

Device type	01		02	
Case outline	E	2	E	2
Terminal number	Terminal symbol			
1	TEST	NC	V_{BATT}	NC
2	NC	TEST	V_{OUT}	V_{BATT}
3	V_{CC}	NC	V_{CC}	V_{OUT}
4	LL_{IN}	V_{CC}	GND	V_{CC}
5	GND	LL_{IN}	BATT ON	GND
6	$\overline{\text{LOW LINE}}$	NC	$\overline{\text{LOW LINE}}$	NC
7	OSC_{IN}	GND	OSC_{IN}	BATT ON
8	OSC SEL	$\overline{\text{LOW LINE}}$	OSC SEL	$\overline{\text{LOW LINE}}$
9	PFI	OSC IN	PFI	OSC_{IN}
10	$\overline{\text{PFO}}$	OSC SEL	$\overline{\text{PFO}}$	OSC SEL
11	WDI	NC	WDI	NC
12	$\overline{CE}_{OUT}$	PFI	NC	PFI
13	$\overline{CE}_{IN}$	$\overline{\text{PFO}}$	LL_{IN}	$\overline{\text{PFO}}$
14	$\overline{\text{WDO}}$	WDI	$\overline{\text{WDO}}$	WDI
15	$\overline{\text{RESET}}$	$\overline{CE}_{OUT}$	$\overline{\text{RESET}}$	NC
16	RESET	NC	RESET	NC
17	---	$\overline{CE}_{IN}$	---	LL_{IN}
18	---	$\overline{\text{WDO}}$	---	$\overline{\text{WDO}}$
19	---	$\overline{\text{RESET}}$	---	$\overline{\text{RESET}}$
20	---	RESET	---	RESET

NC = No connect

FIGURE 1. Terminal connections.

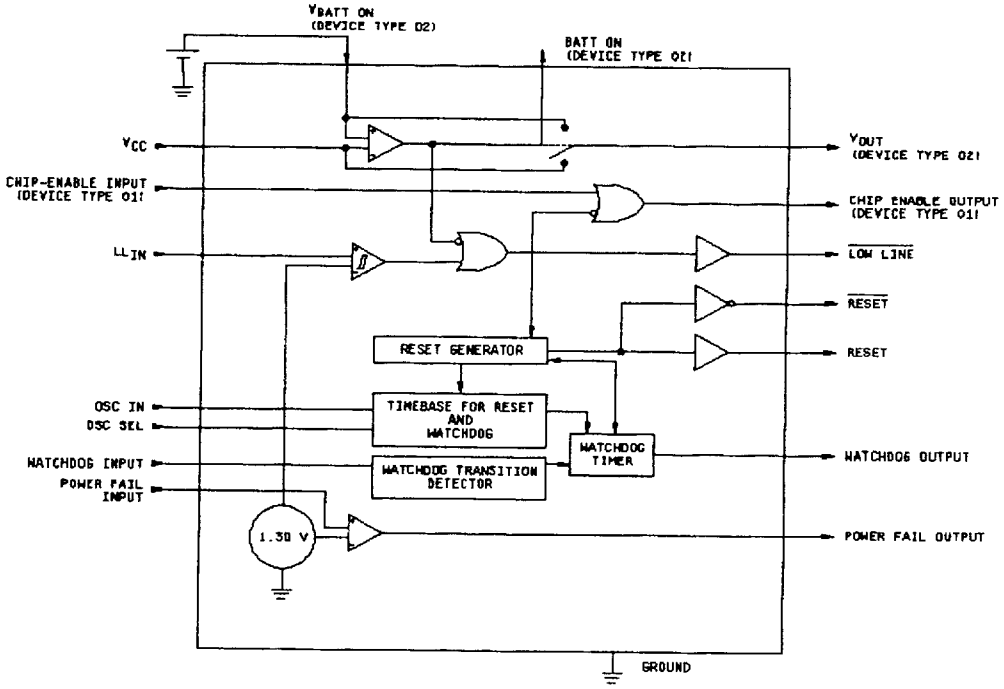


FIGURE 2. Block diagram.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1,2,3, 1/ 9,10,11	1,2,3, 1/ 9,10,11	1,2,3, 1/ 9,10,11
Group A test requirements (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 9	1, 9	1,2,3,9, 10,11
Group D end-point electrical parameters (see 4.4)	1, 9	1, 9	1, 9
Group E end-point electrical parameters (see 4.4)	- - -	- - -	- - -

1/ PDA applies to subgroup 1.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA environment and level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.