MX16C450 – MX82C50A – MX82C50

T-75-37-05

ASYNCHRONOUS COMMUNICATIONS ELEMENT

FEATURES

- Easily interfaces to most popular microprocessors
- Adds or deletes standard asynchronous communication bits (start, stop and parity) to or from serial data stream
- Full double-buffering eliminates need for precise synchronization
- Independently controlled transmit, receive, line status and data set interrupts
- Programmable baud generator allows division of any input clock by 1 to ($2^{16}-1$) and generates the internal 16x clock
- Independent receiver clock input
- Modern control functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$ and $\overline{DCD}$)
- Fully programmable serial-interface characteristics:
  - 5-, 6-, 7- or 8-bit characters
  - Even-, odd- or no-parity bit generation and detection
  - 1-, 1.5- or 2-stop bit generation
  - Baud generation (DC to 56K baud)
- False start bit detection
- Complete status reporting capabilities
- 3-state TTL drive capabilities for bidirectional
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
- Fully prioritized interrupt system controls
- Compatible with PS/2 system speed data bus and control bus
- Line break generation and detection

DESCRIPTION

The MX16C450 is an improved specification version of the MX82C50A Asynchronous Communications Element (ACE). The improved specifications ensure compatibility with state-of-the-art CPUs. Functionally, the MX16C450 is equivalent to the MX82C50A.

The MX16C450, MX82C50A, and MX82C50 each function as a serial data input/output interface in a microcomputer system. The functional configuration of the ACEs is programmed by the system software via a 3-state 8-bit bidirectional data bus; this includes the on-board baud rate generator.

The ACE performs serial-to-parallel conversion on data characters received from a peripheral device or a modem, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the ACE at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the ACE, as well as any error conditions (parity, overrun, framing or break interrupt).

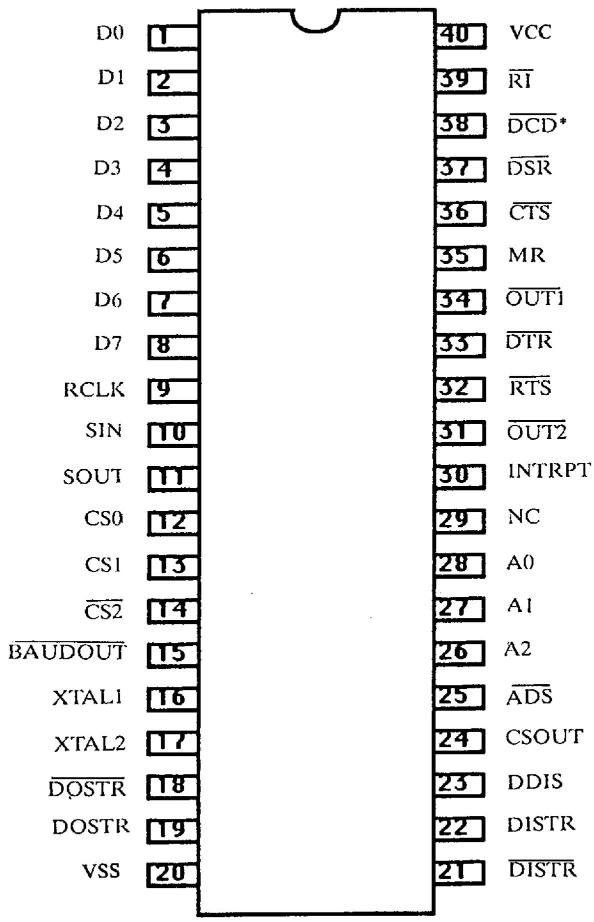
The ACE includes a programmable baud generator that is capable of dividing the timing reference clock input by a divisor between 1 and ($2^{16}-1$), and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE is a complete modem-control capability, and a processor-interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

In additional, the MX16C450/ MX82C50A can run at a maximum speed of 16 MHz.

MX16C450 – MX82C50A – MX82C50

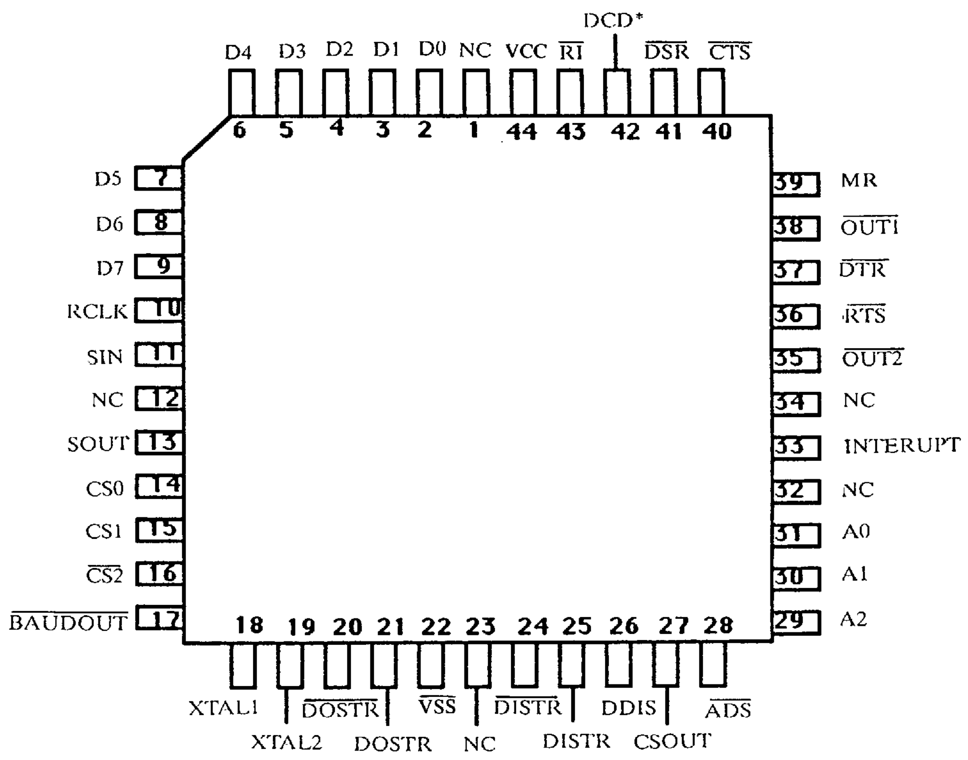
PIN CONFIGURATIONS

MX16C450
MX82C50A
MX82C50

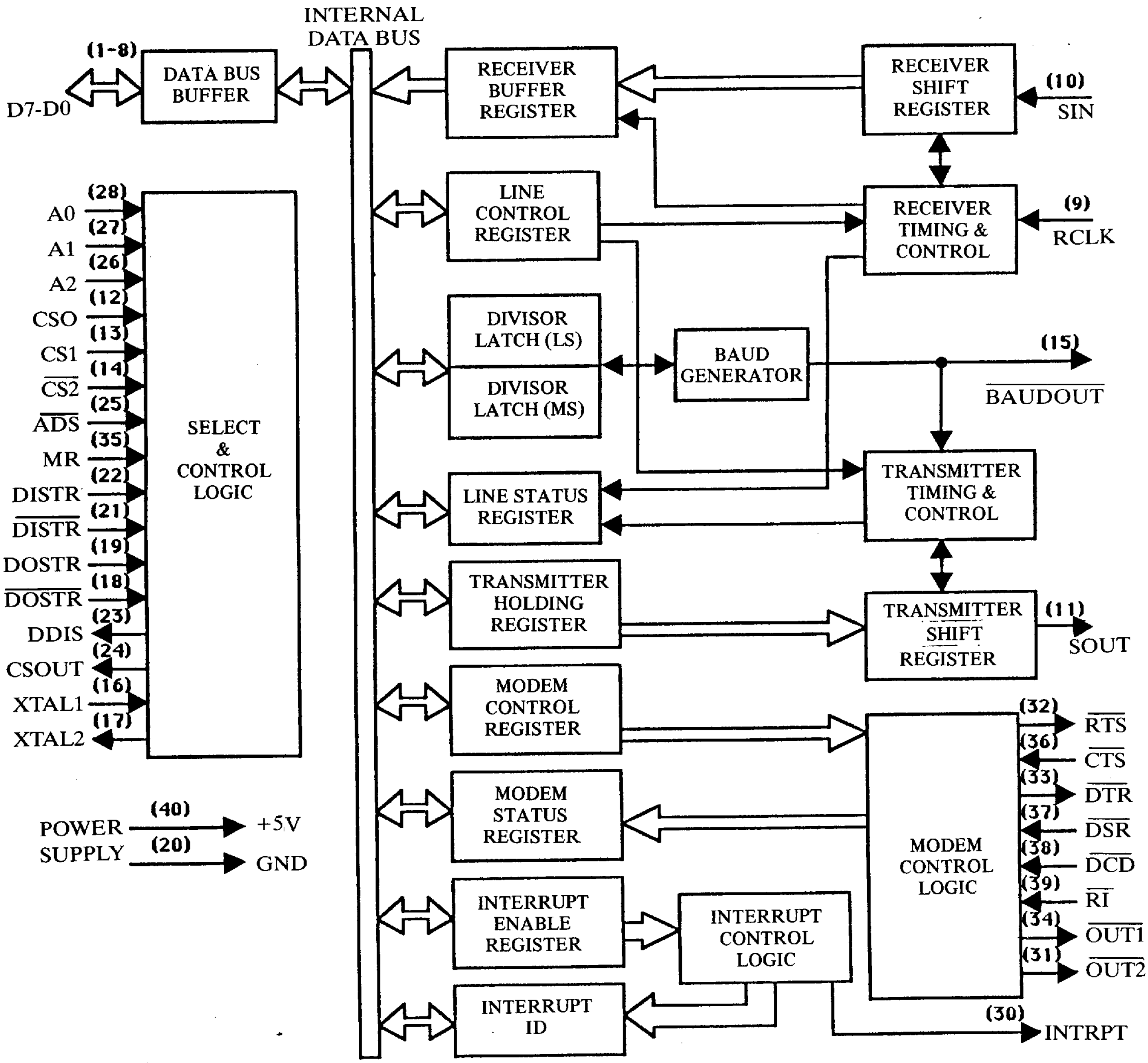


* ON THE MX82C50, PIN 30 (PIN 42 ON THE PLCC PACKAGE) IS ALSO CALLED $\overline{RLSD}$

MX16C450
MX82C50A
MX82C50



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias 0°C to +70°C

Storage Temperature −65°C to +150°C

Voltage on any I/O pin with Respect to Ground −0.5V to +7.0V

Power Dissipation 700 mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only.Functional operation of this device at these or any other condition above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TA = 0°C to +70°C, VCC = 5V ± 5%, VSS = OV, unless otherwise specified

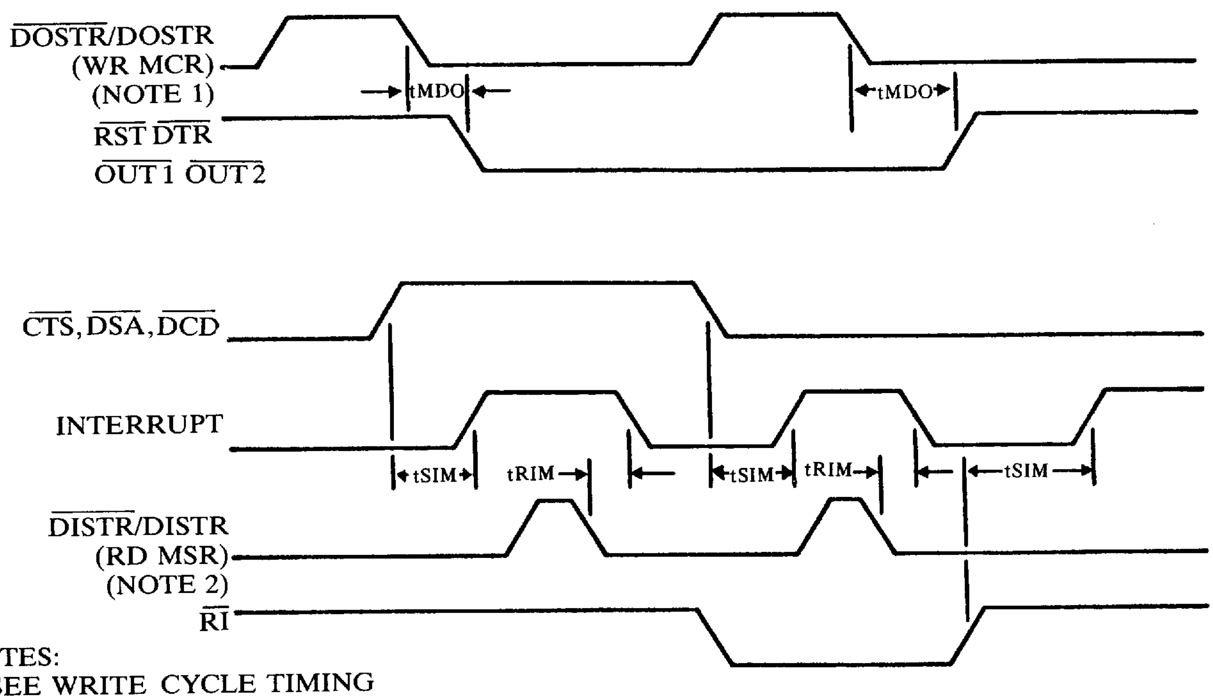
Symbol	Parameter	MX16C450		MX82C50A		MX82C50		Units	Conditions
		Min	Max	Min	Max	Min	Max		
VILX	Clock input LOW Voltage	−0.5	0.8	−0.5	0.8	−0.5	0.8	V	
VIHX	Clock input HIGH Voltage	2.0	VCC	2.0	VCC	2.0	VCC	V	
VIL	Input LOW Voltage	−0.5	0.8	−0.5	0.8	−0.5	0.8	V	
VIH	Input HIGH Voltage	2.0	VCC	2.0	VCC	2.0	VCC	V	
VOL	Output LOW Voltage		0.4		0.4		0.4	V	IOL = 1.6 mA on all Note 1
VOH	Output HIGH Voltage	2.4		2.4		2.4		V	IOH = −1.0 mA Note 1
ICC (Average)	Average Power Supply Current (VCC)		10		10		10	mA	Refer to * *
IIL	Input Leakage		±10		±10		±10	μA	VCC = 5.25V, VSS = OV All other pins floating.
ICL	Clock Leakage		±10		±10		±10	μA	VIN = OV, 5.25V
IOZ	3-state Leakage		±20		±20		±20	μA	VCC = 5.25V, VSS= OV VOUT= OV, 5.25V 1) Chip deselected 2) Chip and write mode selected
VILMR	MR Schmitt VIL		0.8		0.8		N/A	V	
VIHMR	MR Schmitt VH	2.0		2.0		N/A		V	

**: VCC = 5.25V, No loads on SIN, $\overline{DSR}$, $\overline{RLSD}$, $\overline{CTS}$, $\overline{DCD}$. $\overline{RI}$ = 2.0V.
All other inputs = 0.8V. Baud rate generator at 4MHz. Baud rate at 56K.

CAPACITANCE TA = 25°C, f = 1.0 MHz, VCC = VSS = OV

Symbol	Parameter	Min	Typ	Max	Units	Conditions
CXTAL2	Clock Input Capacitance		15	20	pF	fc = 1 MHz
CXTAL1	Clock Output Capacitance		20	30	pF	Unmeasured pins returned to VSS
C1	Input Capacitance		6	10	pF	
C0	Output Capacitance		10	20	pF	

TIMING DIAGRAM
MODEM CONTROLS



NOTES:
1. SEE WRITE CYCLE TIMING
2. SEE READ CYCLE TIMING

PIN DESCRIPTIONS

The following describes the function of all UARTpins. Some of these descriptions reference internal circuits.

In the following descriptions, a low represents a logic O (OVnominal) and a high represents a logic 1 (+2.4V nominal).

• • INPUT SIGNALS

• Chip Select (CSO, CS1, $\overline{CS2}$), Pins 12-14: When CSO and CS1 are high and $\overline{CS2}$ is low, the chip is selected. This enables communication between the UART and the CPU. The positive edge of an active Address Strobe signal latches the decoded chip select signals, completing chip selection. If $\overline{ADS}$ is always low, valid chip selects should stabilize according to the tCSW parameter.

• Read (RD, $\overline{RD}$), Pins 22 and 21: When RD is high or $\overline{RD}$ is low while the chip is selected, the CPU can read status information or data from the selected UART register.
Note: Only an active RD or $\overline{RD}$ input is required to transfer data from UART during a read operation. Therefore, tie either the RD input permanently low or the $\overline{RD}$ input permanent high, when it is not used.

• Write (WR, $\overline{WR}$), Pins 19 and 18: When WR is high or $\overline{WR}$ is low while the chip is selected, the CPU can write control words or data into the selected UART register.
Note: Only an active WR or $\overline{WR}$ input is required to transfer data to the UART during a write operation. Therefore, tie either the WR input permanently low or the $\overline{WR}$ input permanently high, when it is not used.

• Address Strobe ($\overline{ADS}$), Pin 25: The positive edge of an active Address Strobe ($\overline{ADS}$) signal latches the Register Select (A0, A1, A2) and Chip Select (CSO, CS1, $\overline{CS2}$) signals.
Note: An Active $\overline{ADS}$ input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{ADS}$ input permanently low.

•Register Select (A0, A1, A2), Pins 26-28: Address signals connected to these 3 inputs select a UART register for the CPU to read from or write to during data transfer. A table of registers and their addresses is shown below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain UART registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

Register Address				
DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significent byte)
1	0	0	1	Divisor Latch (most significant byte)

• Master Reset (MR), Pin 35: When this input is high, it clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the UART. The States of various output signals (SOUT, INTR, $\overline{OUT1}$, $\overline{OUT2}$, $\overline{RTS}$, $\overline{DTR}$) are affected by an active MR input (Refer to above table.) This input is buffered with a TTL-compatible Schmitt Trigger with 0.5V typical hysteresis.

•Receiver Clock (RCLK), Pin 9: This input is the 16× baud rate clock for the receiver section of the chip.

PIN DESCRIPTIONS (continued)

• Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

• Clear to Send ($\overline{CTS}$), Pin 36: When low, this indicates that the MODEM or data set is ready to exchange data. The $\overline{CTS}$ signal is a MODEM status input whose conditions can be tested by the CPU reading bit 4 (CTS) of the MODEM Status Register. Bit 4 is the complement of the $\overline{CTS}$ signal. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{CTS}$ has no effect on the Transmitter.
Note: Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

• Data Set Ready ($\overline{DSR}$), Pin 37: When low, this indicates that the MODEM or data set is ready to establish the communications link with the UART. The $\overline{DSR}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 5 (DSR) of the MODEM Status Register. Bit 5 is the complement of the $\overline{DSR}$ Signal. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register.
Note: Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

• Data Carrier Detect ($\overline{DCD}$), Pin 38: When low, indicates that the data carrier has been detected by the MODEM or data set. The $\overline{DCD}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 7 (DCD) of the MODEM Status Register. Bit 7 is the complement of the $\overline{DCD}$ signal. Bit 3 (DDCD) of the MODEM Status Register indicates whether the $\overline{DCD}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{DCD}$ has no effect on the receiver.
Note: Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

• Ring Indicator ($\overline{RI}$), Pin 39: When low, this indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 6 (RI) of the MODEM Status Register. Bit 6 is the complement of the $\overline{RI}$ signal. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{RI}$ input signal has changed from a low to a high state since the previous reading of the MODEM Status Register.
Note: Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status interrupt is enabled.

• Vcc, Pin 40: +5V supply.

• Vss, Pin 20: Ground (OV) reference.

• • OUTPUT SIGNALS

• Data Terminal Ready ($\overline{DTR}$), Pin 33: When low, this informs the MODEM or data set that the UART is ready to establish a communications link. The $\overline{DTR}$ output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

• Request the Send ($\overline{RTS}$), Pin 32: When low, this informs the MODEM or data set that the UART is ready to exchange data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

• Output 1 ($\overline{OUT1}$), Pin 34: This user-designated output can be set to an active low by programming bit 2 (OUT1) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

• Output 2 ($\overline{OUT2}$), Pin 31: This user-designated output can be set to an active low by programming bit 3 (OUT2) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

PIN DESCRIPTIONS (continued)

• Chip Select Out (CSOUT), Pin 24: When high, it indicates that the chip has been selected by active, CS0, CS1, and CS2 inputs. No data transfer can be initiated until the CSOUT signal is a logic 1. CSOUT goes low when the UART is deselected.

• Driver Disable (DDIS), Pin 23: This goes low whenever the CPU is reading data from the UART. It can disable or control the direction of a data bus transceiver between the CPU and the UART.

• Baud Out (BAUDOUT), Pin 15: This is the 16 × clock signal from the transmitter section of the UART. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The BAUDOUT may also be used for the receiver section by tying this output to the RCLK input of the chip.

• Interrupt (INTR), Pin 30: This goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Line Status; Received data Available; Transmitter Holding Register Empty; and MODEM Status. The INTR signal is reset low upon the appropriate interrupt service or a Master Reset operation.

• Serial Output (SOUT), Pin 11: This is the composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation or when the transmitter is idle.

• • INPUT/OUTPUT SIGNALS

• Data (D7-D0) Bus, Pins 1-8: This bus is comprised of eight Three-State input/output lines. The bus provides bidirectional communications between the UART and the CPU. Data, control words, and status information are transferred via the D7-D0 Data Bus.

• External Clock Input/Output (XIN, XOUT), Pin 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the UART. When a crystal oscillator or a clock signal is provided, it drives the UART via XIN.

AC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5V ± 5%, Note 5

Symbol	Parameter	MX16C450		MX82C50A		MX82C50			Units	Conditions
		Min	Max	Min	Max	Min	Typ	Max		
tAW	Address Strobe Width	60		90		90			ns	
tAS	Address Setup Time	60		90		110			ns	
tAH	Address Hold Time	0		0		0			ns	
tCS	Chip Select Setup Time	60		90		110			ns	
tCH	Chip Select Hold Time	0		0		0			ns	
tCSS	Chip Select Output Delay From ADS							90	ns	
tDID	DISTR/DISTR Delay From ADS					0			ns	
tDIW	DISTR/DISTR Strobe Width	125		175		175			ns	
tRC	Ready Cycle Delay	175		500		1735			ns	
RC	Ready Cycle = tAR(1) + tDIW + tRC	360		755		2000			ns	
tDD	DISTR/DISTR to Driver Disable Delay		60		75			150	ns	100 pF load Note 4
tDDD	Delay from DISTR/DISTR to Data		125		175			250	ns	100 pF load
tHZ	DISTR/DISTR to Floating Data Delay	0	100	100		100			ns	100 pF load Note 4
tDOD	DOSTR/DOSTR delay from ADS					50			ns	
tDOW	DOSTR/DOSTR Strobe Width	100		175		175			ns	
tWC	Write Cycle Delay	200		500		1785			ns	
WC	Write Cycle = tAW* + tDOW + tWC	360		755		2100			ns	
tDS	Data Setup Time	40		90		175			ns	

AC CHARACTERISTICS (Cont.) TA = 0°C to +70°C, VCC = 5V ± 5%, Note 5

Symbol	Parameter	MX16C450		MX82C50A		MX82C50			Units	Conditions
		Min	Max	Min	Max	Min	Typ	Max		
tDH	Data Hold Time	40		60		60			ns	
tCSC*	Chip Select Output Delay from Select		100		125			200	ns	100 pF load
tRA*	Address Hold Time from $\overline{DISTR}$/DISTR	20		20		50			ns	Note 2
tRCS*	Chip Select Hold Time from $\overline{DISTR}$/DISTR	20		20		50			ns	Note 2
tAR*	$\overline{DISTR}$/DISTR Delay from Address	60		80		110			ns	Note 2
tCSR*	$\overline{DISTR}$/DISTR Delay From Chip Select	50		80		110			ns	Note 2
tWA*	Address Hold Time from $\overline{DSSTR}$/DSSTR	20		20		50			ns	Note 2
tWCS*	Chip Select Hold Time from $\overline{DOSTR}$/DOSTR	20		20		50			ns	Note 2
tAW*	$\overline{DOSTR}$/DOSTR Delay from Address	60		80		160			ns	Note 2
tCSW*	$\overline{DOSTR}$/DOSTR Delay from Select	50		80		160			ns	Note 2
tMRW	Master Reset Pulse Width	5		10		25			µs	
tXH	Duration of Clock HIGH Pulse	140		140		140			ns	
tXL	Duration of Clock LOW Pulse	140		140		140			ns	External Clock (3.1 MHz Max.)

AC CHARACTERISTICS (Cont.) TA = 0°C to +70°C, VCC = 5V ± 5%

Symbol	Parameter	MX16C450		MX82C50A		MX82C50			Units	Conditions
		Min	Max	Min	Max	Min	Typ	Max		
Transmitter										
tHR1	Delay from rising edge of $\overline{\text{DOSTR}}$ /DOSTR (WR THR) to Reset interrupt		175		1000			N/A	ns	100 pF load
tHR2	Delay from falling edge of $\overline{\text{DOSTR}}$ /DOSTR (WR THR) to Reset interrupt		n/a		n/a		1000		ns	100 pF load
tIRS	Delay from Initial INTR Reset to Transmit Start	8	24	8	24		16		RCLK cycles	Note 3
tSI	Delay from initial Write to interrupt	16	32	16	32		24		RCLK cycles	Note 3
tSS	Delay from Stop to Next Start						1000		ns	
tSTI	Delay from Stop to Interrupt (THRE)	8	8	8	8		8		RCLK cycles	Note 3
tIR	Delay from $\overline{\text{DISTR}}$/DISTR (RD IIR) to Reset Interrupt (THRE)		250		1000		1000		ns	100 pF load
Modem Control										
tMDO	Delay from $\overline{\text{DISTR}}$/DISTR (WR MCR) to Output		200		1000		1000		ns	100 pF load
tSIM	Delay to Set Interrupt from MODEM Input				1000		1000		ns	100 pF load
tRIM	Delay to Reset Interrupt from $\overline{\text{DISTR}}$/DISTR (RS MSR)		250		1000		1000		ns	100 pF load

Baud Generator

N	Baud Divisor	1	$2^{16}-1$	1	$2^{16}-1$	1	$2^{16}-1$			
tBLD	Baud Output Negative Edge Delay		125		250		250		ns	100 pF load
tBHD	Baud Output Positive Edge Delay		125		250		250		ns	100 pF load
tLW	Baud Output Down Time	425		425			425		ns	Refer *
tHW	Baud Output Up Time	330		330			330		ns	Refer **

* – fx = 2 MHz, divided by 2, 100 pF load
** – fx = 3 MHz, divided by 3, 100 pF load

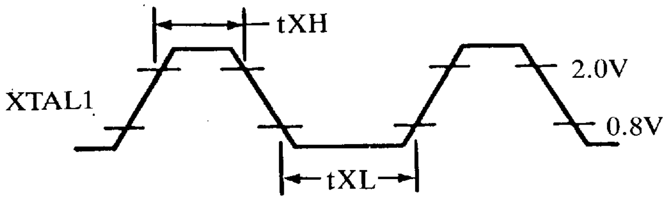
Receiver

tSCD	Delay from RCLK to Sample Time		2		2		2		μs	
tSINT	Delay from Stop to Set Interrupt	1	1	1	1		2		RCLK cycles	Note 3
tRINT	Delay from $\overline{DISTR}$/DISTR (RD RBR/RDLSR) to Reset Interrupt		1		1		1		μs	100 pF load

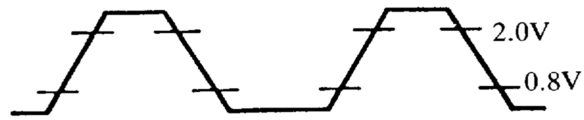
Notes:
1. Does not apply to XTAL2.
2. Applicable only when ADS is tied LOW.
3. RCLK = tXH and tXL
4. Charge and discharge time is determined by VOL, VOH and the external loading.
5. All timings are referenced to valid 0 and valid 1 (see AC TEST POINTS).

AC TESTING INPUT/OUTPUT WAVE FORM

EXTERNAL CLOCK INPUT (3.1 MHz MAXIMUM)

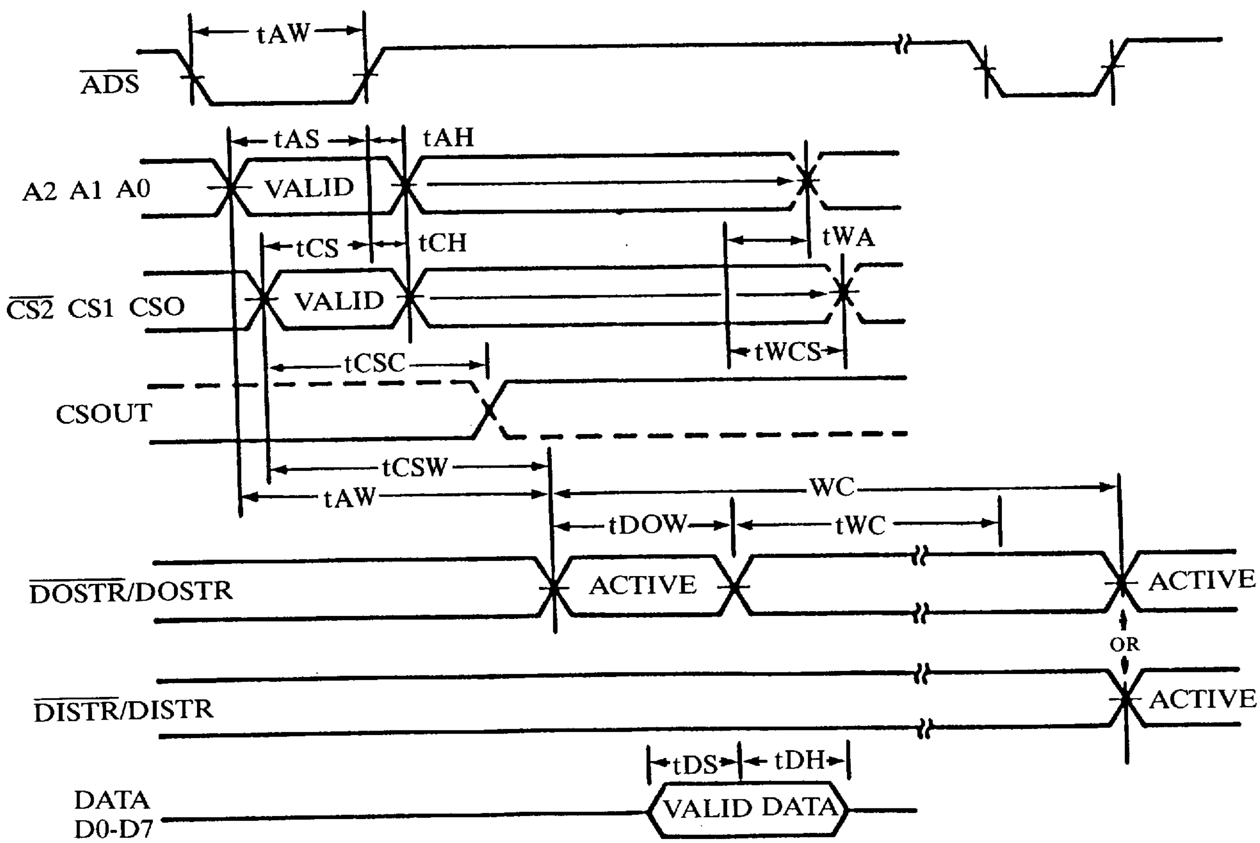


AC TEST POINTS



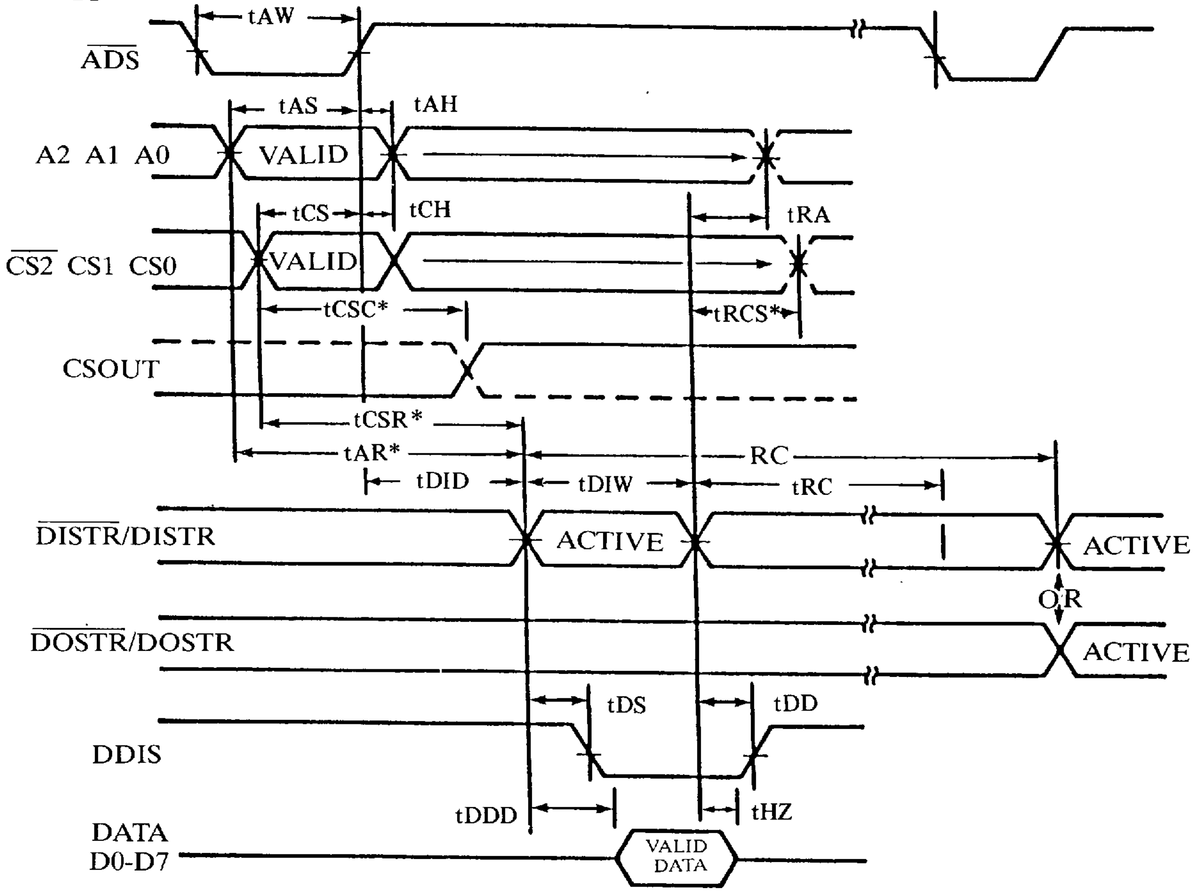
TIMING DIAGRAM

WRITE CYCLE

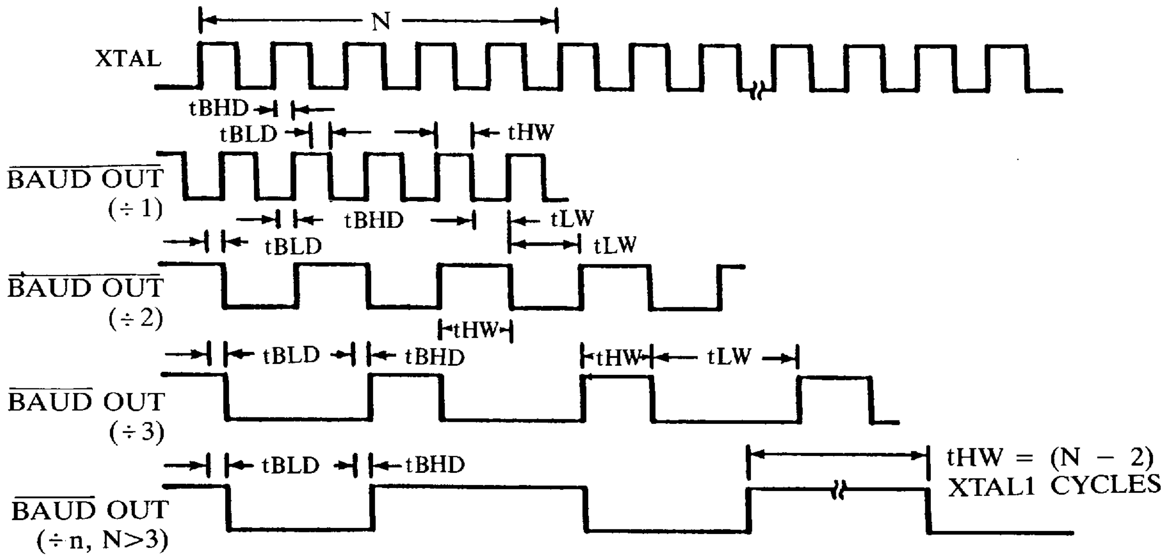


TIMING DIAGRAMS

READ CYCLE

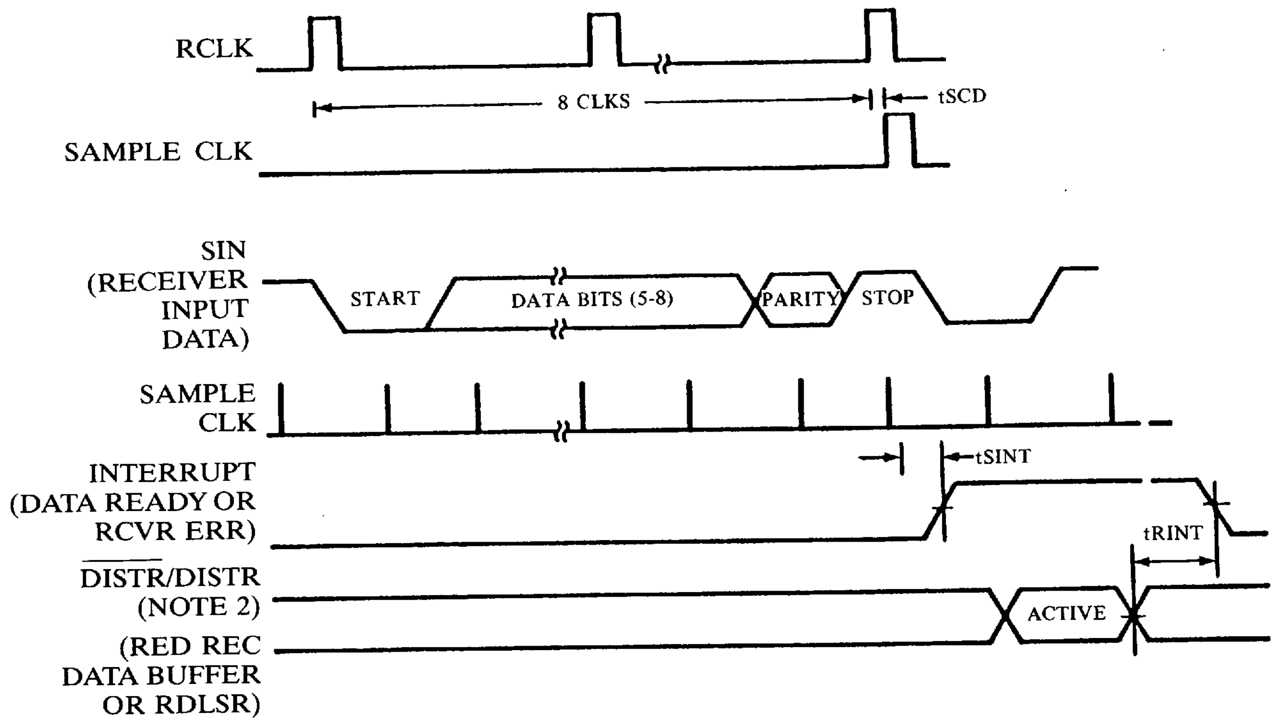


BAUDOUT

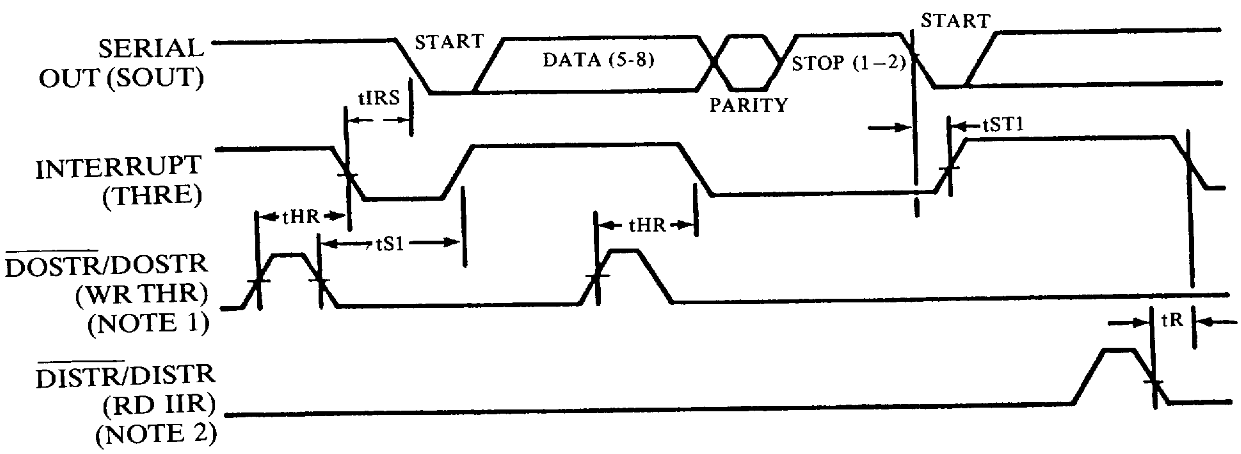


TIMING DIAGRAMS

RECEIVER

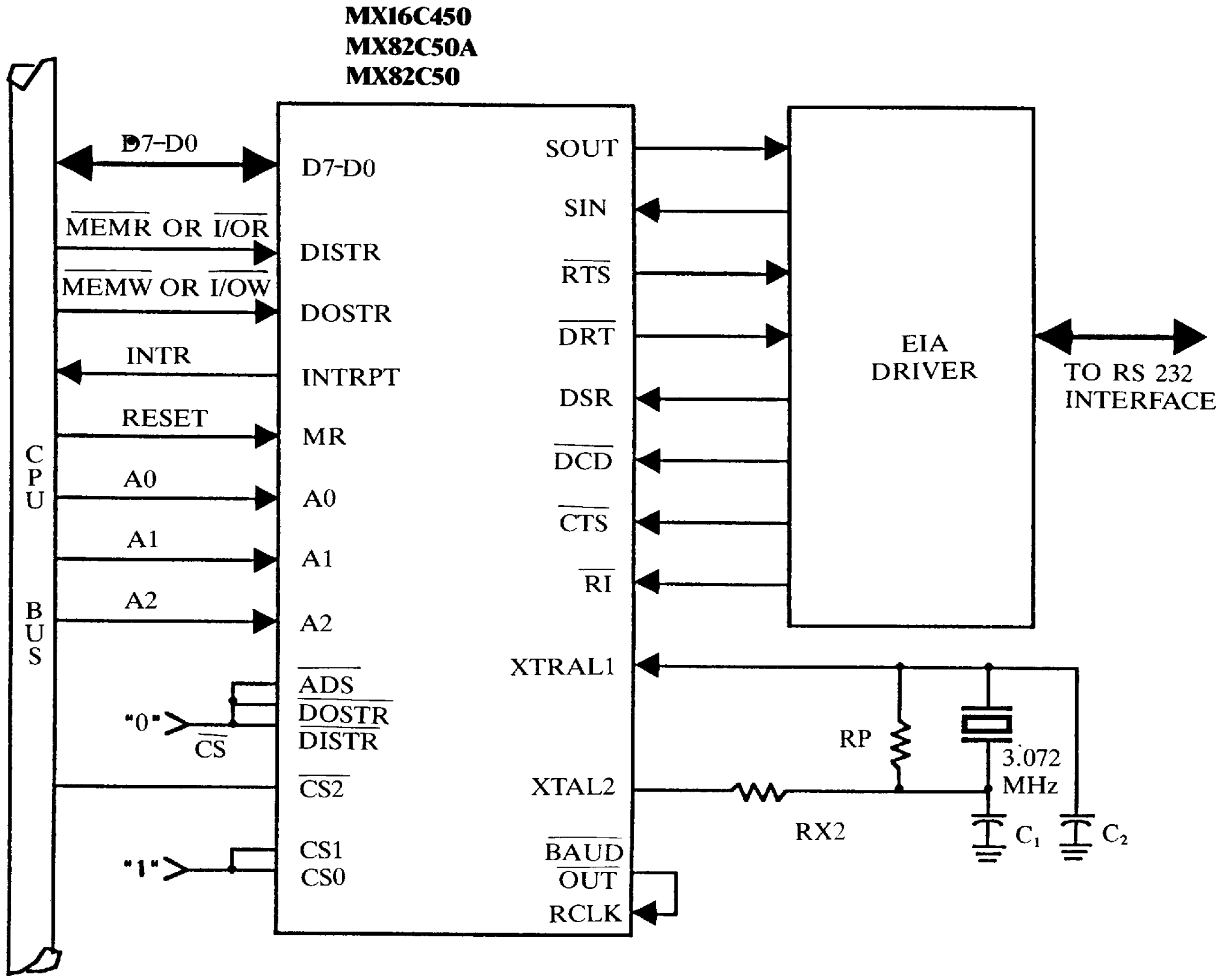


TRANSMITTER



NOTES:
1. SEE WRITE CYCLE TIMING
2. SEE READ CYCLE TIMING

BASIC CONFIGURATION
MX16C450, MX82C50A, MX82C50

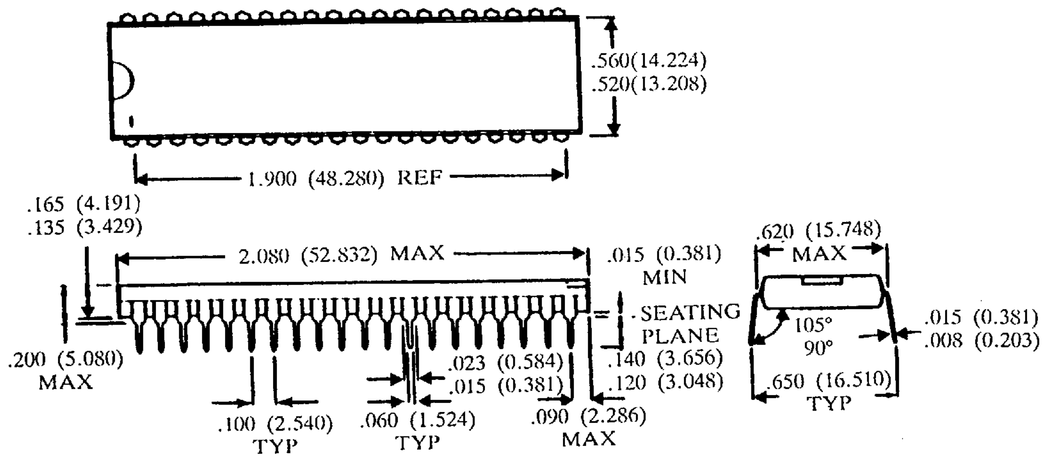


TYPICAL COMPONENT VALVES

Crystal	RP	RX2	C1	C2
3.072 MHz	1MΩ	1.5Ω	10 . 30 pF	40 . 90 pF

PACKAGE OUTLINES

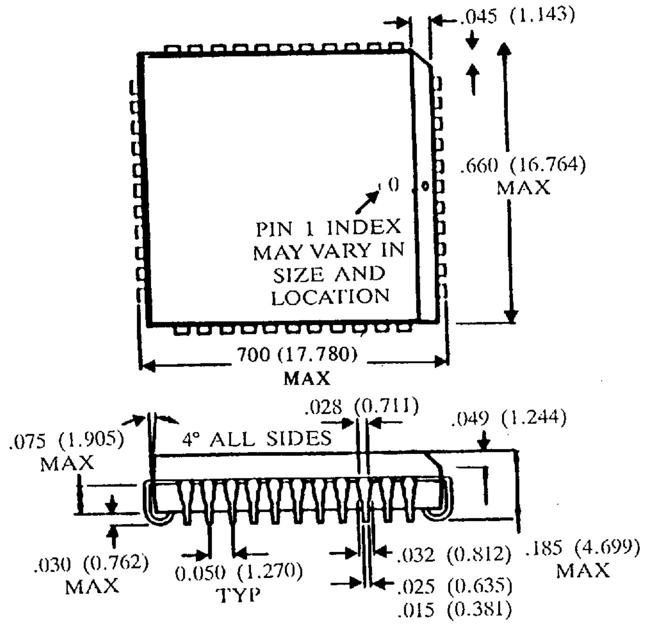
40-PIN PLASTIC DUAL IN-LINE PACKAGE



NOTES: UNLESS OTHERWISE SPECIFIED.
1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
2. LEAD MATERIAL: ALLOY 42 OR COPPER.
3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR WHICH IS .010 (0.254) MAX. AT EACH END.
4. TOLERANCE TO BE +/– .005 (0.127) UNLESS OTHERWISE NOTED.
5. ALL METRIC DIMENSIONS ARE IN PARENTHESES ( ).
6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

PACKAGE OUTLINES

44-PIN PLASTIC LEADED CHIP CARRIER



NOTES:
1. TOLERANCE TO BE +/– .005 (0.127) INCH.
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR WHICH IS .010 (0.254) INCH MAX. ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES ( ).

1348 Ridder Park Drive San Jose, CA 95131 (408)453-8088