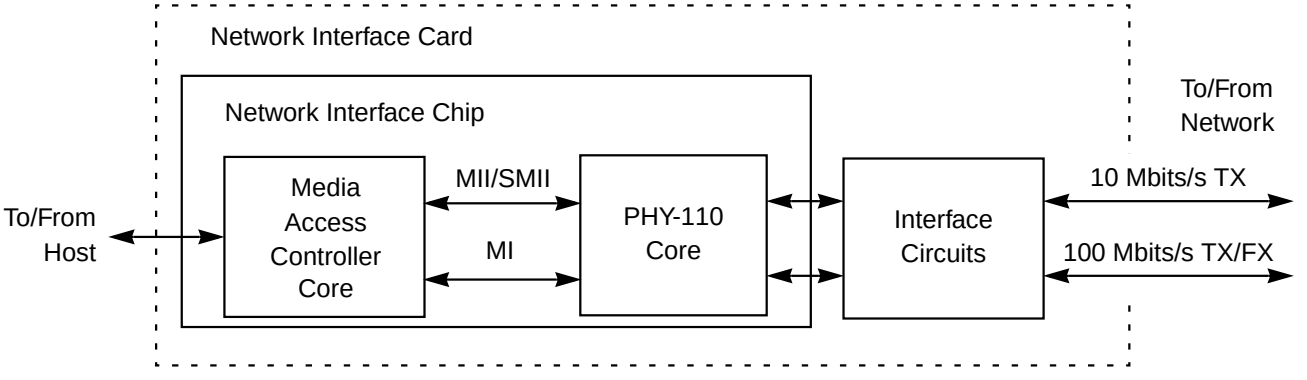
Ethernet PHY-110 Core

Preliminary Datasheet

The LSI Logic PHY-110 core is a complete physical layer solution for 10 and 100 Mbits/s Ethernet connections. Figure 1 shows a typical application of the PHY-110. When combined with a 10/100 Mbits/s Media Access Controller (MAC), the PHY-100 and MAC become a complete Network Interface chip, reducing the component system and assembly costs of a network connection.

The PHY-110 has also been designed for cost-effective, multiple-channel applications by breaking out the common channel circuits, such as the clock generator, in a separate hardmac that need not be repeated for each channel.

Figure 1 A Typical PHY-110 Application



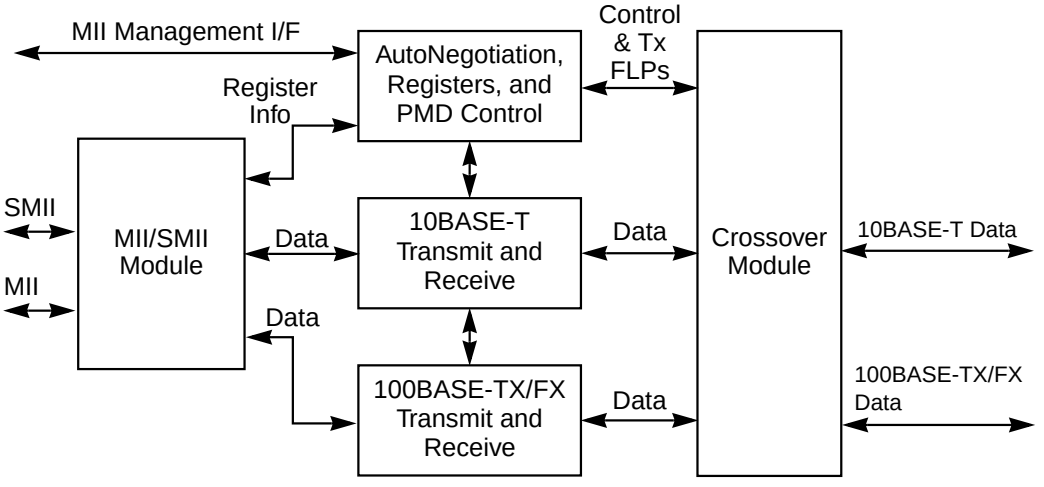
PHY-110 Overview

As shown in Figure 2, the PHY-110 Core is actually three PHYs in one, 10BASE-T, 100BASE-TX, and 100BASE-FX. The PHY operates in the 100BASE-TX or 100BASE-FX mode at 100 Mbits/s, or in the 10BASE-T mode at 10 Mbits/s. The 100 Mbits/s mode and the 10 Mbits/s mode differ in data rate, signaling protocol, and cabling as follows:

- 100BASE-TX mode uses two pairs of category 5 or better UTP or STP twisted-pair cable with 4B5B encoded, scrambled, MLT3 coded, 125 MHz data to achieve a throughput of 100 Mbits/s.

- 10BASE-T mode uses two pairs of category 3 or better UTP or STP twisted-pair cable with Manchester encoded, 10 MHz data to achieve a 10 Mbits/s throughput.
- 100BASE-FX mode uses two fibers with 4B5B encoded, NRZI, 125 MHz data through an ECL driver to achieve a throughput of 100 Mbits/s.

Figure 2 Top Level Block Diagram



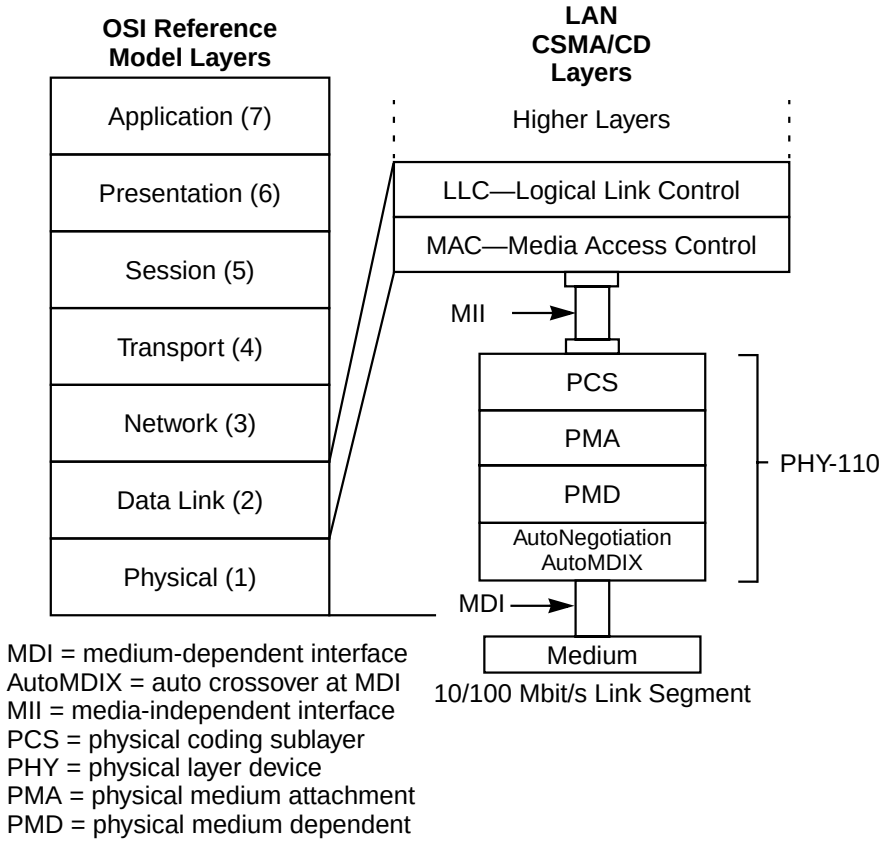
There is a transmit data path and a receive data path associated with each PHY mode. The transmit data path is from the MII/SMII Module input to the twisted-pair or fiber output of the Crossover (AutoMDIX) Module. The receive data path is from the twisted-pair or fiber input of the Crossover module to the MII/SMII Module output. The MII Management Interface provides host access to control and status registers in the core.

PHY Core and the OSI Model

Figure 3 shows how the PHY core fits into the ISO Open Systems Interconnection (OSI) Reference model. The OSI model defines a data communications protocol consisting of seven distinct layers.

See the *CSMA/CD Access Method and Physical Layer Specifications, 1998 Edition* ANSI/IEEE Standard 802.3 for detailed descriptions of the functions of a PHY.

Figure 3 PHY Core Relationship to the OSI Model



Features

The main features of the PHY core are:

- Single-channel PHY configurable for 10BASE-T, 100BASE-TX, or 100BASE-FX operation
- Meets all applicable IEEE 802.3, 10BASE-T, 100BASE-TX, and 100BASE-FX specifications
- AutoMDIX or manual crossover for transmit and receive twisted-pair input/outputs
- 1.8 Vdc required
- Low power (< 280 mW) for high port-count integration
- Half-duplex or full-duplex operation
- MII or Serial MII (SMII) interface to Ethernet MAC

- Management Interface (MI) for access to configuration and status registers
- AutoNegotiation for 10/100 Mbits/s, full/half duplex operation
- In-core wave shaping (no external filters required)
- Adaptive equalizer for 100BASE-TX operation
- Baseline wander correction
- Strap options for configuring core (without using the management interface)
- Far-End Fault (FEF) handling
- Supports up to four parallel LED outputs or a serial LED output programmable to reflect any one of 16 events
- Scan support in the digital logic
- Pattern generators and checkers for ATE tests, characterization and diagnostics

Deliverables

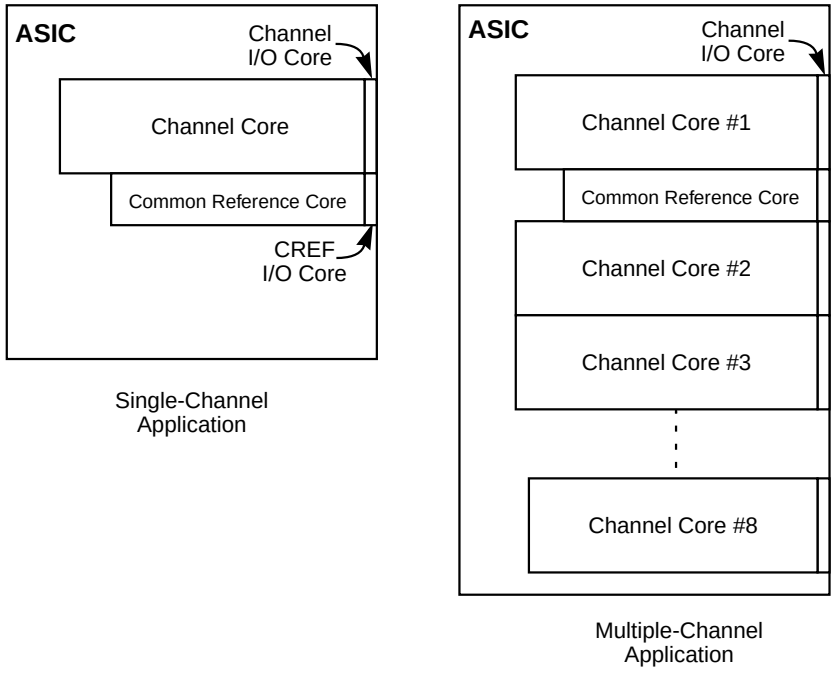
The primary deliverables are four hardmacros:

- Channel Core
- Channel I/O Core
- Common Reference (CREF) Core
- CREF I/O Core
- Encrypted RTL simulation models and/or behavioral models
- Gate netlist and wrappers
- A System Verification Environment (SVE)
- Synthesis and timing models
- Complete documentation
- LSI Logic FlexStream® software support

Core Layouts

Figure 4 shows floorplans of ASICs with a single-channel PHY and a multiple-channel PHY. In all designs, the PHY cores must be arranged similar to that shown. That is, the Reference Core must be adjacent to a Channel Core, and the I/O cores must be between the Channel and Reference Cores and the edge of the ASIC. One Common Reference Core can support up to eight Channel Cores.

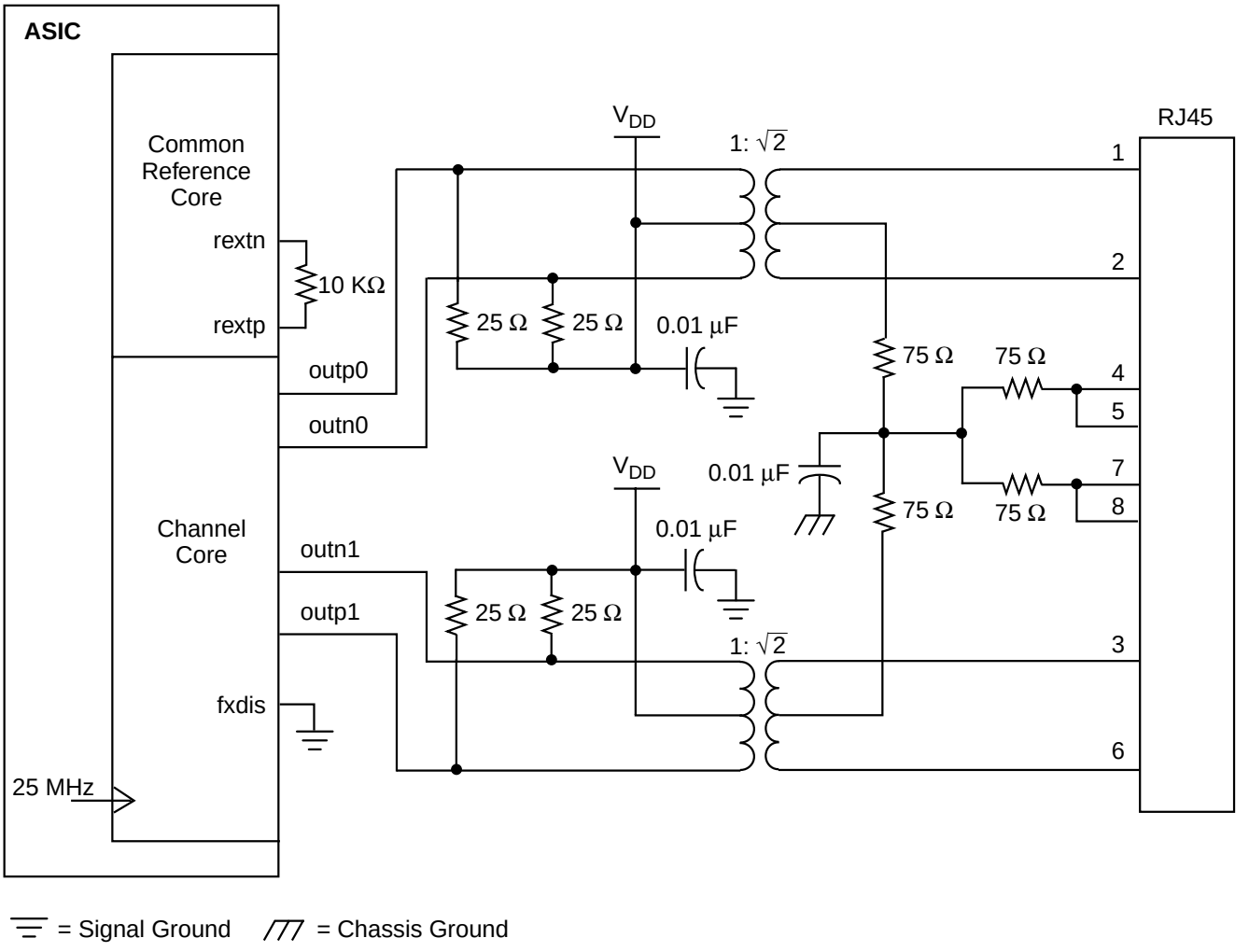
Figure 4 PHY-110 Layout Configurations



External TX Connections

Figure 5 shows the external components and wiring for the Common Reference and Channel cores for connection to twisted-pair cable. The differential, twisted-pair outputs of the Channel core are outp0 and outn0 and the inputs are outp1 and outn1. The transformers have a 1: $\sqrt{2}$ turns ratio and are available from Pulse, Bel Fuse Inc., and HALO Electronics Inc. The terminating resistors shown are for 50 Ω, UTP cable.

Figure 5 Front-End Schematic



Test Features

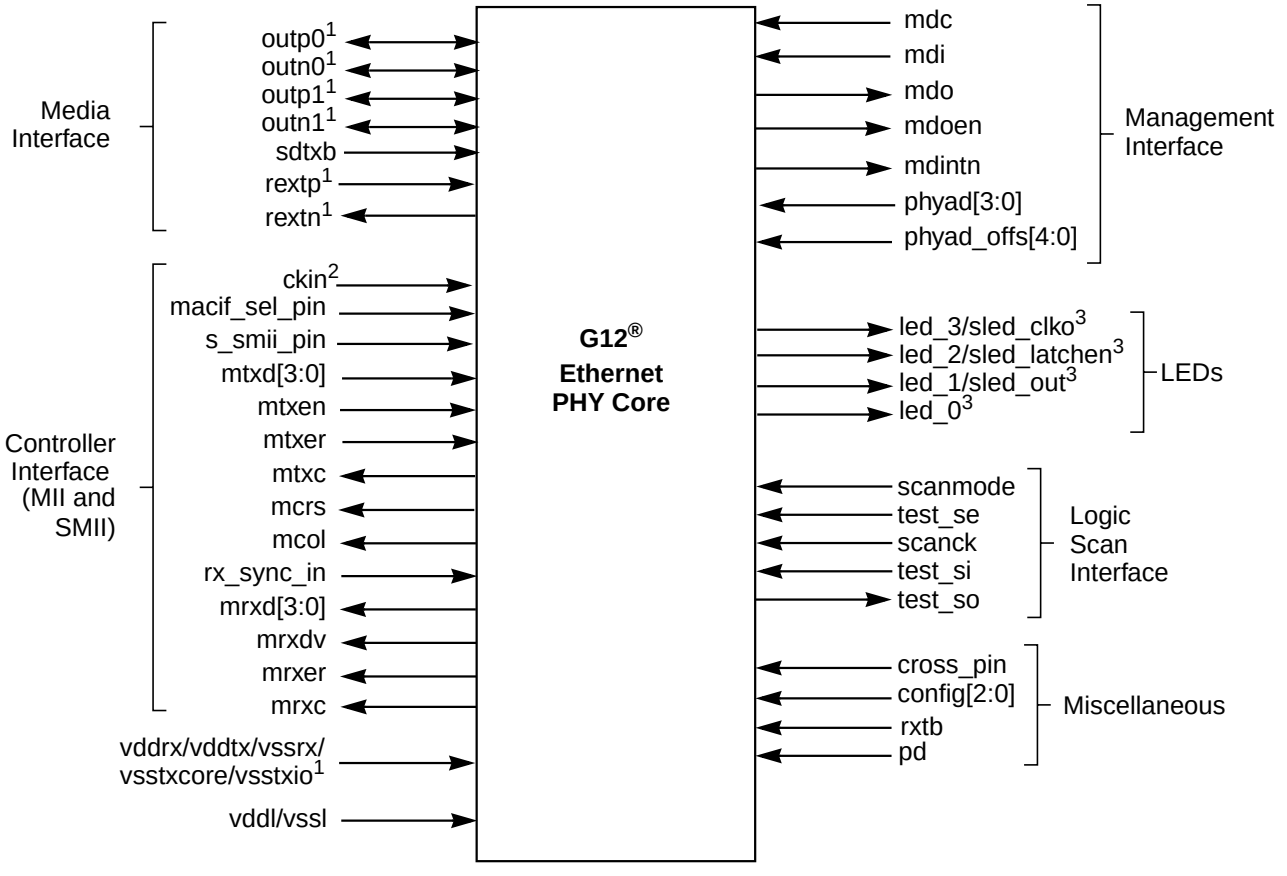
The PHY-110 has several built-in features that can be used for ATE testing and diagnostics. It contains pattern generators that can be used for various twisted-pair measurements such as, the Transmit Output Voltage (TOV), Total Harmonic Distortion (THD), Template match, Rise/Fall time, Overshoot, Duty Cycle Distortion, and Waveform symmetry.

A pattern generator on the transmit side, a loopback feature at the twisted-pair output, and a CRC checker on the receive side allows most of the PHY-110 circuits to be easily tested.

I/O Signals

Figure 6 shows the I/O signals of the PHY-110 organized by interface. The sections following list the signals in the order of the figure and describe them. Unless otherwise noted in the descriptions, the signals are active HIGH.

Figure 6 I/O Signals



[1] Pin must be external to ASIC.
[2] Can be provided externally or from an ASIC internal clock.
[3] Optional external pins.

Media Interface Signals

outp0 **Twisted-Pair Transmit Output (Positive), or FX Receive Input (Negative)** **O/I**

The sdtxb input controls the configuration of the outp0/outn0 signals. The outp0/outn0 signals function as twisted-pair outputs or fiber optic inputs, based on the

signal level of the corresponding sdtxb input. For more details, see the sdtxb signal description in this section.

outn0 **Twisted-Pair Transmit Output (Negative), or FX Receive Input (Positive)** **O/I**

The sdtxb input controls the configuration of the outp0/outn0 signals. The outp0/outn0 signals function as twisted-pair outputs or fiber optic inputs, based on the signal level of the corresponding sdtxb input. For more details, see the sdtxb signal description in this section.

outp1 **Twisted-Pair Receive Input (Positive), or FX Transmit Output (Positive)** **I/O**

The sdtxb input controls the configuration of the outp1/outn1 signals. The outp1/outn1 signals function as twisted-pair outputs or fiber optic inputs, based on the signal level of the corresponding sdtxb input. For more details, see the sdtxb signal description in this section.

outn1 **Twisted-Pair Receive Input (Negative), or FX Transmit Output (Negative)** **I/O**

The sdtxb input controls the configuration of the outp1/outn1 signals. The outp1/outn1 signals function as twisted-pair outputs or fiber optic inputs, based on the signal level of the corresponding sdtxb input. For more details, see the sdtxb signal description in this section.

sdtxb **FX Signal Detect Input/FX Interface Disable** **I**

When this line is not tied to GND, the FX interface is enabled and this line becomes an ECL signal detect input. When this line is tied to GND, the FX interface is disabled and the TP interface is enabled.

rextp, rextn **Transmit Current Set** **I**

An external resistor connected between the rextp and rextn inputs sets the peak output current for the TP and FX transmit outputs according to the following formula:

$$R_{EXT} = \frac{10K}{I_{OUT}} \times I_{REF}$$

where: R_{EXT} is the value of the external resistor
I_{OUT} is the peak output current
I_{REF} = 40.0 x $\sqrt{2}$ mA (100 Mbits/s, UTP)
32.6 x $\sqrt{2}$ mA (100 Mbits/s, STP)
100.0 x $\sqrt{2}$ mA (10 Mbits/s, UTP)
81.6 x $\sqrt{2}$ mA (10 Mbits/s, STP)

Controller Interface Signals (MII and SMII)

ckin — **Global Clock In** — **I**

This clock input generates all the device's internal clocks. Controller interface data for all channels is latched in and out of the device on the rising edges of ckin. In MII mode, ckin must run at 25 MHz; in SMII mode, it must run at 125 MHz.

macif_sel_pin — **Controller Interface Select** — **Pullup I**

This input is tied HIGH to select MII mode and tied LOW to select SMII mode.

s_smii_pin — **SMII Source Synchronous Mode Select** — **I**

This pin is tied HIGH for SMII source synchronous mode and tied LOW for source non-synchronous mode.

mtxd[3:0] — **Transmit Data Input** — **I**

Transmit, 4-bit parallel data in for processing and transmission over the TP or FX outputs. The data is clocked in on the rising edge of ckin in MII and SMII modes.

mtxen — **Transmit Enable Input** — **I**

In MII mode, the mtxen input from the controller interface is asserted to indicate valid data on mtxd and mtxer. These inputs are clocked in on the rising edges of ckin. In SMII mode, this signal is not used.

mtxer — **Transmit Error** — **I**

When asserted, this signal indicates that an error was detected in the connecting MAC. When mtxer is asserted for one or more clock periods while mtxen is asserted, the PHY-110 transmits one or more symbols in the current frame which are not part of the valid data or delimiter set. The PHY-110 ignores mtxer when mtxen is deasserted.

mtxc — **Transmit Clock** — **O**

Timing signal for all transmit nibble operations. It is 25 MHz in 100 Mbits/s operation and 2.5 MHz in 10 Mbits/s operation.

mcrs	**Carrier Sense** In MII mode, this output is asserted when valid data is detected on the receive TP or FX inputs. The output toggles at 12.5 MHz when no more valid data is detected but data is still being output on the mrxd[3:0] pins. mcrs is deasserted on the rising edge of ckin when data output on mrxd[3:0] has been completed. mcrs is not used in SMII mode.	**O**
mcol	**Collision** This signal is asserted when the PHY-110 detects simultaneous transmit and receive activity in half-duplex mode.	**O**
rx_sync_in	**Global SMII Synchronization** In SMII mode, the rx_sync_in input is asserted once every ten mtxd/mrxd bits to indicate the beginning of each 10-bit data segment on mtxd/mrxd. rx_sync_in is clocked into the core on the rising edge of ckin. In MII mode, rx_sync_in is not used.	**I**
mrxd[3:0]	**Receive Data Out** These signals connect to the controller interface. They contain data from the receive TP or FX inputs and are clocked out on the rising edge of ckin in MII and SMII modes.	**O**
mrxdv	**Receive Data Valid** The PHY-110 asserts this signal when it is presenting valid data on the mrxd[3:0] lines. The mrxdv signal remains asserted for the entire duration of the frame and is deasserted prior to the first rising edge following the end of the frame.	**O**
mrxer	**Receive Error** This controller interface output is asserted when coding or other specified errors are detected on the TP or FX inputs. It is clocked out on the rising edge of mtxc in MII mode. In SMII mode, mrxer is not used.	**O**
mrxc	**Receive Clock** Timing signal for all receive nibble operations. It is 25 MHz in 100 Mbits/s operation and 2.5 MHz in 10 Mbits/s operation.	**O**

Management Interface (MI) Signals

mdc **MI Clock** **I**

The mdc clock shifts serial data for the internal registers into and out of the mdio line on its rising edge.

mdi **MI Input Data** **I**

This line carries serial data to the internal registers. The data is clocked in the core on the rising edge of mdc.

mdo **MI Output Data** **O**

This line carries serial data from the internal registers. The data is clocked out of the core on the rising edge of mdc.

mdoen **Management Data Output Enable** **O**

This signal is asserted when valid data is placed on mdo and can be used as a data strobe by the connecting device.

mdintn **MI Interrupt** **O.D. Pullup O**

The mdintn signal is an active LOW interrupt output. It is asserted when there is a change in certain internal register bits and deasserted after all changed bits have been read.

phyad[3:0] **MI Physical Address** **I**

This is the 4-bit address provided to the PHY-110. It is a unique address and distinguishes this PHY-110 from any other PHY present in the system. The PHY-110 only responds to transactions if the address in the management frame matches the address on these pins.

phyad_offs[4:0]

Physical Address Offset **I**

These signals are only relevant when this PHY-110 is used for multi-port designs. In multi-port designs the 5-bit offset helps determine the unique 5-bit address of a port, since the device will only have a 5-bit address input. For example, in a two-port design, the offset of the first port is zero and the offset of the second port is one. When the offset is added to phyad[4:0], the port gets its unique address. The address offset is a 5-bit input since the absolute maximum number of PHYs that can be controlled by an STA is 32.

LED Signals

led0–3 **Parallel LED Outputs 0–3** **O**

These outputs can each be programmed though the MI serial port to indicate any one of 16 events when they are asserted. The following table lists the events and indicates the default for each output.

Events	Defaults
FEF (Far End Failure)	
Blink	
HI Z	
OFF	
ON	
10/100	led0
HDX/FDX	led1
COL	
ACT	led2
XMTACT	
RCVACT	
LINK + ANEG	
LINK + ACT	
LINK100	
LINK10	
LINK DETECT	led3

These outputs can drive an LED from either V_{DD} or GND.

sled_out (led_1 pin)

Serial LED Out **O**

LED data output line in serial LED mode.

sled_latchen (led_2 pin)

Serial LED Latch Enable **O**

The latch signal is a one-clock wide pulse indicating the end of a frame.

sled_clko (led_3 pin)

Serial LED Clock **O**

This signal clocks the data out on sled_out at 1 MHz.

Logic Scan Interface Signals

scanmode	**Scan Mode Select** This input is asserted to select the logic scan mode and deasserted (default) for normal operation.	**I**
test_se	**Scan Chain Enable** This input is asserted to enable the scan and put all the logic in the scan chain into scan mode.	**I**
scanck	**Scan Clock** The scan clock is connected to all flops during scan mode.	**I**
test_si	**Scan Data In** This is the input of the core scan chain during scan mode. Scan patterns will be loaded to this input pin.	**I**
test_so	**Scan Data Out** This is the output of the scan chain to carry the scan patterns out of the core during scan mode.	**O**

Miscellaneous Signals

cross_pin	**Crossover Enable** Asserting the cross input causes a manual crossover of the TP outputs and inputs whether or not autocrossover is enabled (see config[2:0] following).	**I**
config[2:0]	**Core Configurations** The config[2:0] inputs are read at reset and their coding is used to set the default condition of the register configuration bits as shown in Table 1. For example, a config setting of 0b010 turns off AutoNegotiation, sets operation to 10 Mbits/s half duplex, and turns off autocrossover.	**I**

Table 1 PHY-110 Configurations

config[2:0]	Internal Register Bits			
	AUTO	SPDSEL	DPLX	AUTOXEN
0b000	0b1 = ON	X	X	0b1 = ON
0b001	0b1 = ON	X	X	0b0 = OFF
0b010	0b0 = OFF	0b0 = 10 Mbits/s	0b0 = Half	0b0 = OFF
0b011	0b0 = OFF	0b0 = 10 Mbits/s	0b1 = Full	0b0 = OFF
0b100	0b0 = OFF	0b1 = 100 Mbits/s	0b0 = Half	0b0 = OFF
0b101	0b0 = OFF	0b1 = 100 Mbits/s	0b1 = Full	0b0 = OFF
0b110	0b0 = OFF	0b0 = 10 Mbits/s	0b0 = Half	0b1 = ON
0b111	0b0 = OFF	0b1 = 100 Mbits/s	0b0 = Half	0b0 = OFF

rxtb **Hardware Reset** **Pullup I**
This input is asserted and then deasserted to reset the core. The core completes reset 100 ms after this signal is deasserted.

pd **Power Down** **I**
When asserted, pd powers down all of the Common Reference circuits except those that generate the frck25m clock signal.

Power Supplies

vddrx, vddtx, vssrx, vsstxcore, vsstxio **I**
1.8 V analog supplies and grounds.

vddl, vssl **I**
1.8 V digital supply and ground for digital core circuits.

Notes

Notes

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