AN-682

Fairchild Semiconductor
Application Note
July 1992
Revised November 2001

FAIRCHILD SEMICONDUCTOR™

Terminating F100K ECL Inputs

Introduction

Many F100K designs require that certain inputs be presented with a HIGH or LOW level. Because of the construction of the F100K input circuitry, a LOW can be realized by simply leaving the input OPEN. However, a HIGH must be terminated in a special way. Simply tying the input to V_{CC}/V_{CCA} is unacceptable.

Design Considerations

The ranges of V_{IH} and V_{IL} across V_{EE} (–4.2V to –5.7V for F100K ECL 300 Series) are –870 mV to –1165 mV and –1475 mV to –1830 mV respectively. By staying within these ranges, proper input conditions are assured. Figure 1 shows the voltage versus current for the F100K input transistor. If the input is tied to V_{CC}/V_{CCA} the input transistor saturates (Point D) which can damage internal circuitry. The best V_{IH} to realize a HIGH is a voltage drop of 0.9V below V_{CC}/V_{CCA}. As can be seen from the graph, this locates the quiescent point on the flat part of the curve (Point C) midway within the acceptable range of V_{IH}. Figure 2 shows three ways in which a HIGH can be realized on the input. These circuits allow the user to maintain constant input signals at optimum levels of V_{EE} and temperature. Each circuit can handle multiple fanouts, the number will depend upon the maximum current capability of the circuit. The designer should be aware that although Figure 2A, Figure 2B, and Figure 2C supply ECL compatible signals levels, they differ in power consumption and susceptibility to changes in temperature and V_{EE}.

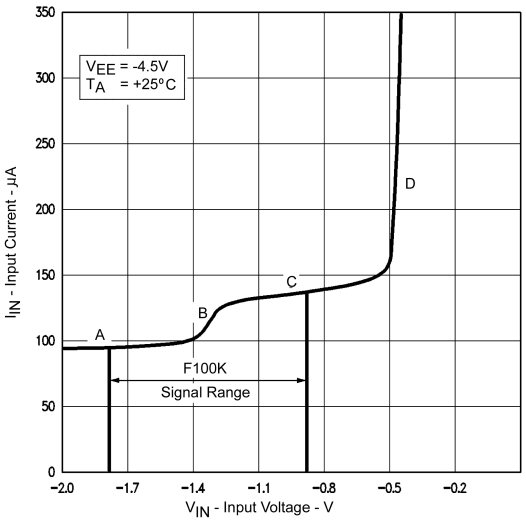
For designs where there are multiple unused inputs and extra logic gates available, fanout from the unused gates is possible. As an example, one gate of the 100302 is capable of driving ten quiescent inputs at voltage and current levels typical of F100K as shown in Figure 3.

Figure 4 shows in detail the F100K pull-up scheme and the input circuitry. Although the circuits of Figure 2 are good examples, a detailed circuit analysis must include the 50 kΩ input resistor. In Figure 4A, the resistor (R_D) which sets the diode biasing current is in parallel with the 50 kΩ input resistor. Similarly, the circuit of Figure 4B shows that R_2 is in parallel with the input resistor.

The point to emphasize is never tie an F100K input to V_{CC}/V_{CCA} in order to realize a HIGH preset. Instead, the following is recommended:

- For a LOW level — leave input open or tie to V_{EE}.
- For a HIGH level — tie input to a diode drop or 0.9V below V_{CC}/V_{CCA}.

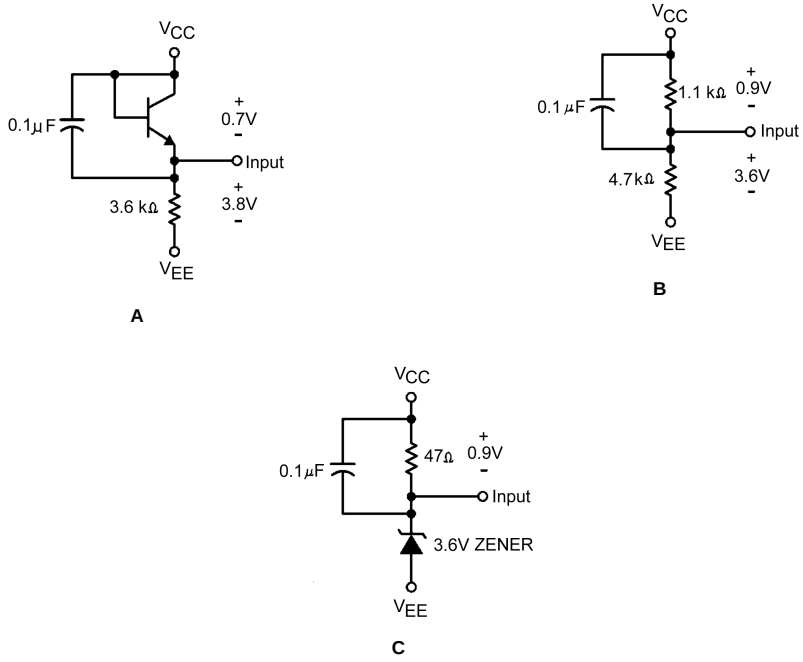
Remember also that the 50 kΩ input resistor must be considered in the circuit parameter calculations.



A = 50 KΩ Pull-Down Current
B = Transition (Switching) Region
C = Base Current plus 50 kΩ
D = Input Transistor Saturation

FIGURE 1. Input Characteristics

Design Considerations (Continued)



Note: Nominal values are shown.

FIGURE 2. Equivalent Circuits for HIGH Termination

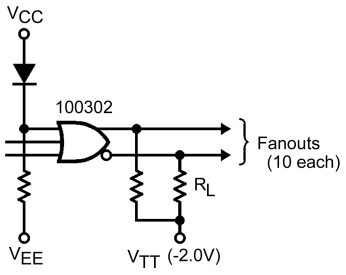


FIGURE 3. Utilizing Unused Gates to Terminate Multiple HIGHs and LOWs

Design Considerations (Continued)

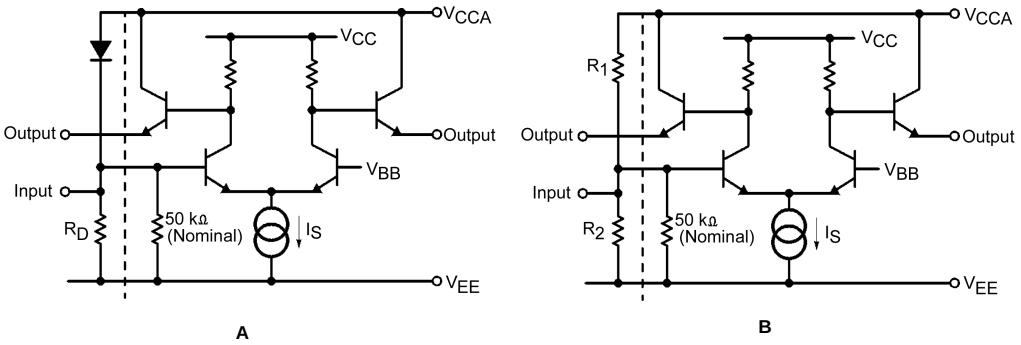


FIGURE 4. Pull-Up Circuit Examples